IT81202E-000/IT81202VG-000
IT81202E-256/IT81202VG-256
IT81202E-512/IT81202VG-512
IT81202E-1024/IT81202VG-1024

Embedded Controller

Preliminary Specification V0.3.2

(For B Version)

ITE TECH. INC.

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Revision History

Section	Revision	Page No.
-	Initial release For B version	-

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FIGURES

TABLES

1. Features

- **32-bit RISC-V Micro-controller**
  - 5-stage pipeline
  - 4KB instruction cache
  - RISC-V RV32IMAFC instruction set
  - "M" standard extension for integer multiplication and division
  - "A" standard extension for atomic instructions
  - "F" standard extension for single-precision floating-point
  - "C" standard extension for compressed instructions
  - Variable frequency range to gain maximum performance, up to 96MHz core clock

- **Smart Cache Controller**
  - Total 60KB SRAM
  - Configurable instruction-local-memory (ILM) size from 0KB~60KB
  - Configurable data-local-memory (DLM) size from 0KB~60KB

- **eSPI Interface**
  - Compatible with the eSPI specification v1.0
  - Supports Peripheral Channel
  - Supports VW IRQ/System Event
  - Supports 20MHz to 66MHz

- **LPC Bus Interface**
  - Compatible with LPC specification v1.1
  - Supports I/O read/write
  - Supports Memory read/write
  - Supports FWH read/write
  - Serial IRQ
  - Supports LPC 19.2MHz to 33MHz
  - Supports 3.3V/1.8V level

- **SPI Slave Interface**
  - Supports 4-wire serial interface

- **Embedded Flash**
  - 0K/256K/512K/1024K-byte e-flash
  - Over 100,000 erase/program cycles

- **Flash Interface**
  - FSPI Supports 3.3V/1.8V level

- **Crystal-Free**
  - Built-in 32.768 kHz clock generator
  - External crystal oscillator not required

- **SMBus Controller**
  - SMBus spec. 2.0
  - 6 SMBus channels, with 3 DMA controllers
  - Up to 6 SMBus masters or 5 slaves
  - Compatible with I2C standard mode (100Kbps) / fast-mode (400Kbps) / fast-mode plus (1Mbps)

- **System Wake Up Control**
  - Modem RI# wake up
  - Telephone RING# wake up
  - IRQ/SMI# routing

- **EC Wake Up Control**
  - 100 external/internal wake-up events
  - 86 WUI pins

- **Interrupt Controller**
  - 145 interrupt events to EC
  - Fixed priority

- **Timer / Watch Dog Timer**
  - 1 external 16-bit timer
  - 4 external 24-bit timers
  - 3 external 32-bit timers
  - The 16-bit timer can act as a watch dog timer, based on 32.768 k clock source
  - Can be used as RTOS tick-timer

- **UART**
  - 2 standard serial ports (legacy 16C550 COM1/COM2)
    Baud rate up to 460800
  - Receiver/Transmitter can be enabled separately
  - Hardware flow control

- **ACPI Power Management Channel**
  - 5 power management channels
  - Compatible and enhanced mode

- **Battery-backed SRAM (BRAM)**
  - 192-byte battery-backed memory space

- **GPIO**
  - Supports 86-port GPIO
  - Programmable pull up/pull down
  - Schmitt trigger for input
  - Supports 33-port 1.8V input level

- **KBC Interface**
  - 8042 style KBC interface
  - Legacy IRQ1 and IRQ12
  - Fast A20G and KB reset

- **ADC**
  - 11 ADC channels (8 external)
  - 10-bit resolution (+/- 4LSB)
  - Digital filter for noise reduction
  - 6 voltage comparators
- **PWM**
  - 8 PWM channels
  - 32.768 kHz of base clock frequency
  - 8 duty cycles of resolution
  - 8/16-bit common input clock prescaler
  - 4 prescalers for 8 PWM output used for devices with different frequencies
  - Supports PWM open-drain output
  - Supports two sets of tachometers; each can be switched from two external pins.
  - 1 tachometer for color sensor
- **PECI Host**
  - PECI spec. 2.0/3.0/3.1
  - Supports 16-byte write/read length
  - Supports FCS checking mechanism
  - Supports AW_FCS hardwired mechanism
  - Supports adjustable V_{TT} level
- **KB Matrix Scan**
  - Hardware keyboard scan
  - 18x8 keyboard matrix scan
- **SPI Master (SSPI)**
  - 2-channel SPI master, frequency up to (FreqPLL / 2) MHz
  - 4-wire or 3-wire (bi-directional data) I/F
  - Supports n-bit transmission (n = 1 ~ 8)
  - SPI Mode 0, 1, 2, 3
  - Support DMA transfer
- **USB Type-C CC Logic**
  - Supports 2 sets of USB Type-C (R1.3) ports
  - DRP/DFP/UFP (including dead battery condition) mode
  - Audio adaptor accessory mode
  - Debug accessory mode
- **USB Power Delivery (USBPD)**
  - Supports 2 sets of USB PD (R3.0 V1.2) ports
  - BMC PHY
  - Dual role (provider & consumer)
  - Policy manager
  - Supports Fast Role Swap detection
- **In-System Programming**
  - ISP via parallel port interface on existing KBS connector
  - Fast flash programming with software provided by ITE
- **In-System Debugging**
  - ISD via parallel port / SMB / JTAG interface on existing KBS connector
  - ISD via SMB / JTAG interface on 2-wire USB connector
  - Supports EC memory snoop
  - Supports up to 8 breakpoint sets of CPU
- **Power Consumption**
  - Standby with Sleep mode current: TBD µA
- **CEC**
  - Suitable for HDMI 1.4a standard
- **Package**
  - LQFP 128 / VFBGA 128

2. General Description

The IT81202 is a highly integrated embedded controller with system functions suitable for mobile system applications. The IT81202 directly interfaces to the eSPI/LPC bus and provides ACPI embedded controller function, an SPI slave interface, keyboard controller (KBC) and matrix scan, PWM and ADC for hardware monitor, BRAM and system wake-up functions for system power management. The IT81202 also provides the solution for USB Type-C and USB Power Delivery port control.

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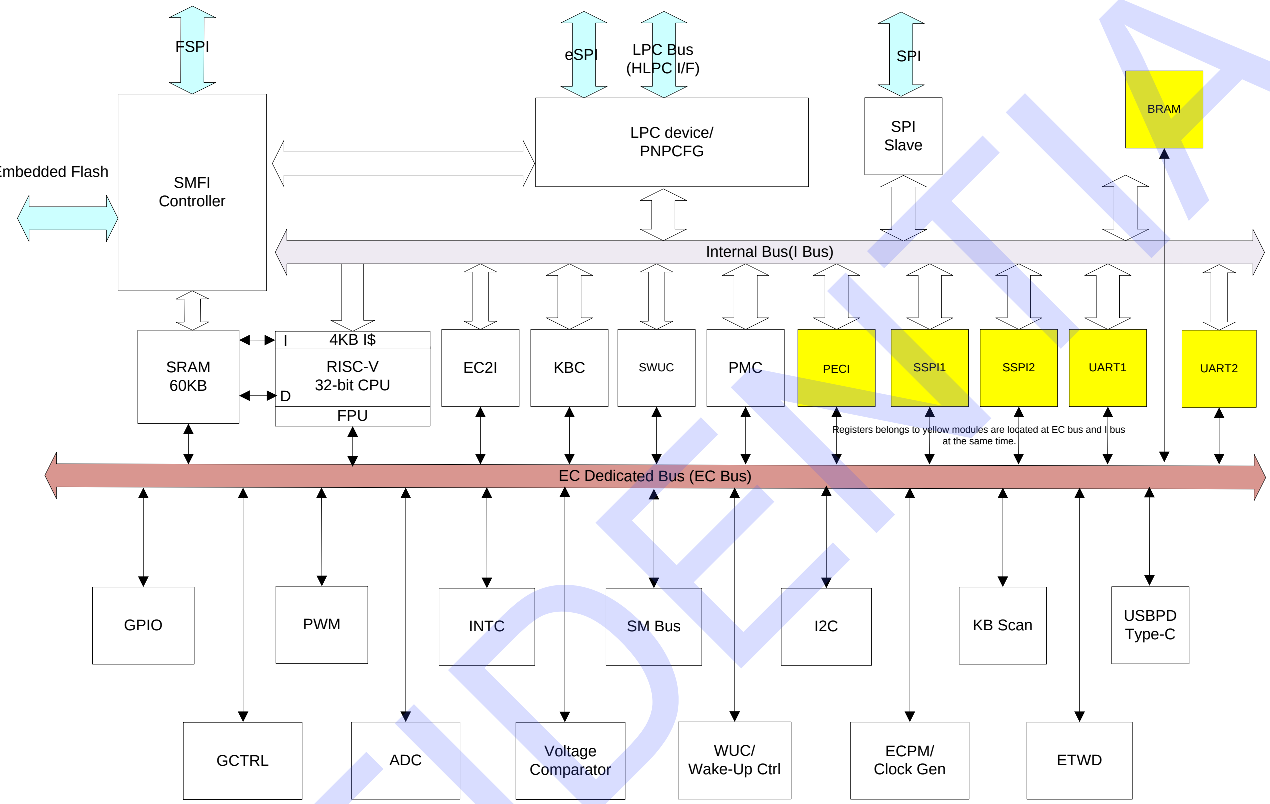
3. System Block Diagram

3.1 Block Diagram

- **IT81202:**



- **Host Domain:**
  LPC, eSPI, PNPCFG, host parts of SMFI/SWUC/KBC/PMC logical devices and host parts of EC2I.

- **EC Domain:**
  JTAG, INTC, WUC KB Scan, GPIO, ECPM, SMB, ADC, PWM, ETWD, EC2I, GCTRL, BRAM, DBGR, USBPD, EC parts of SMFI/SWUC/KBC/PMC and EC parts of EC2I.

- **Double-mapping Module:**
  BRAM, SSPI, PECI, UART1 and UART2.

Note: The SPI master (abbreviated as SSPI) is connected to the slow (contrast to SPI flash) SPI slave(s). The SPI slave (abbreviated as SPI) is connected to a host CPU or an application processor.

3.2 EC Mapped Memory Space

Figure 3-1. EC Memory Map

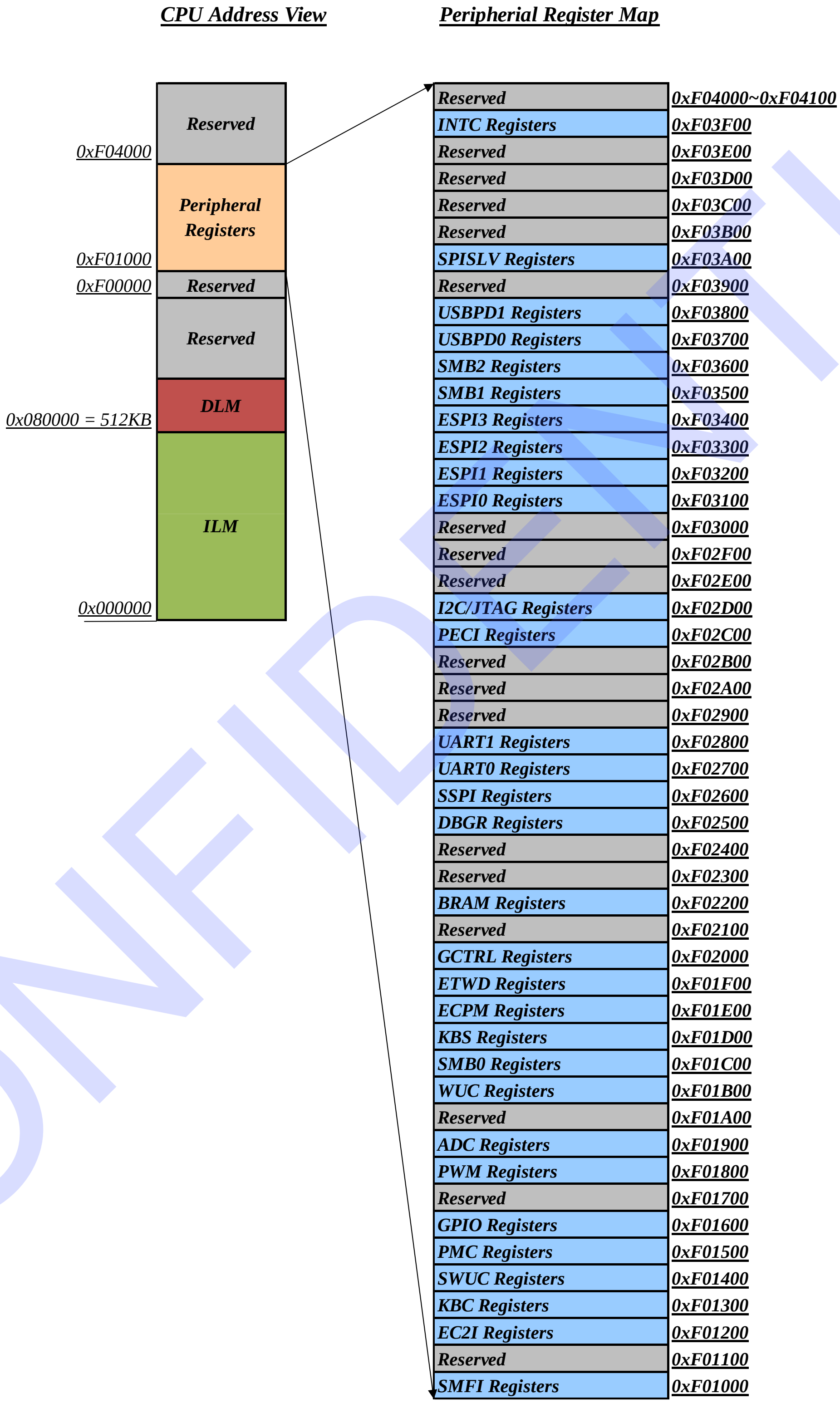


Figure 3-2. EC Code Memory Map

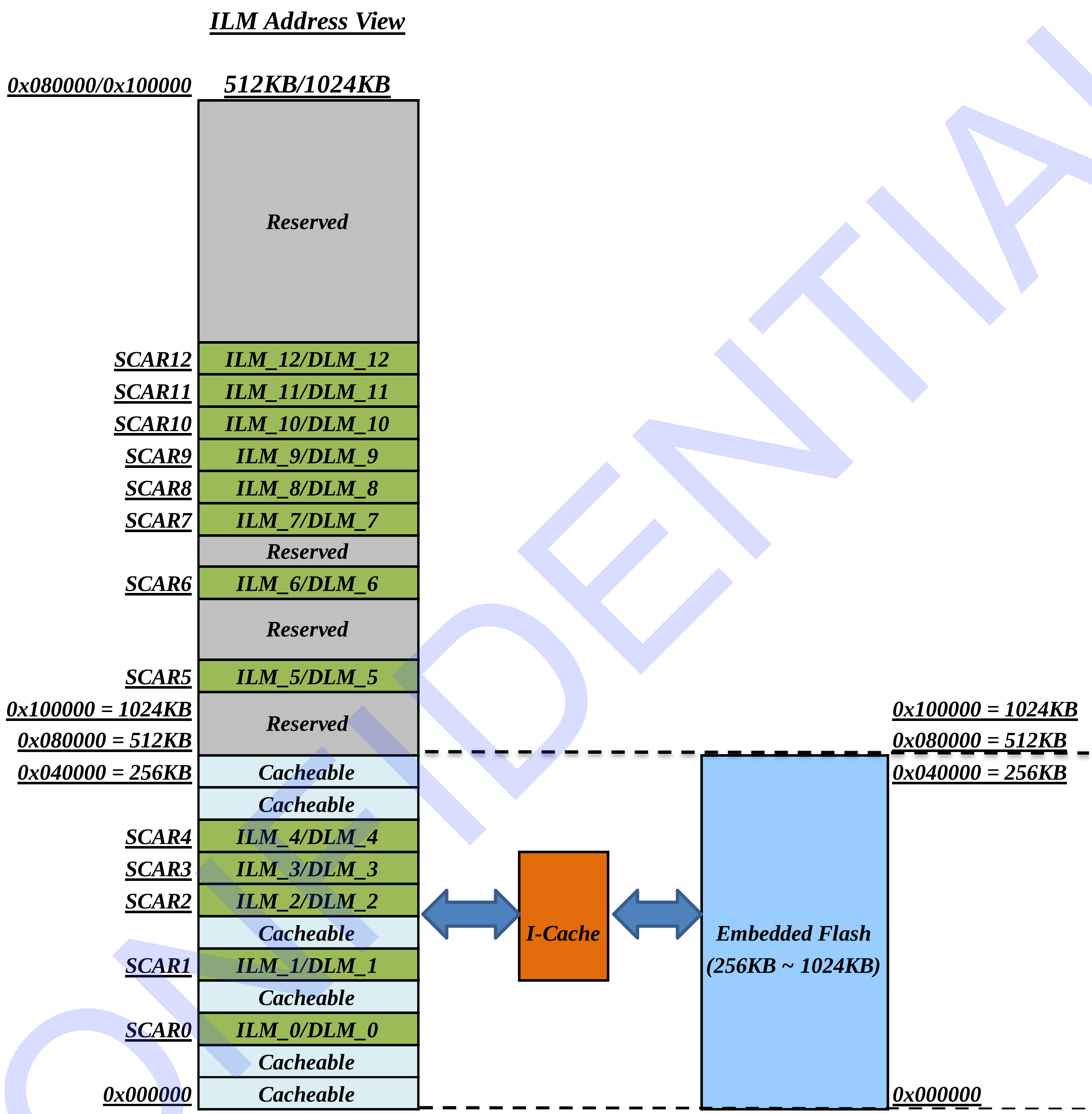
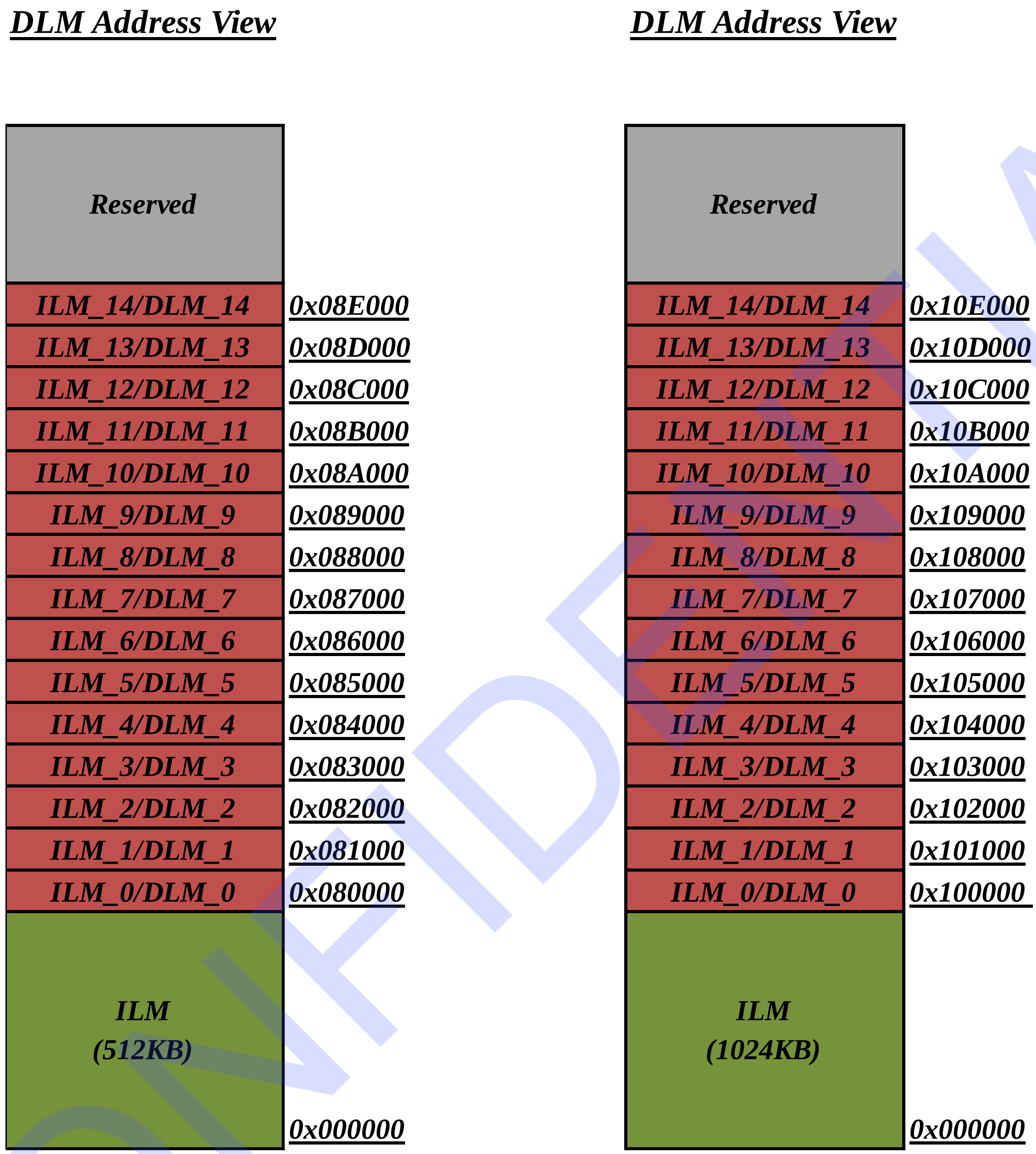


Figure 3-3. EC Data Memory Map



3.3 Register Abbreviation

The register abbreviations and access rules are listed below:

R	**READ ONLY**.	If a register is read only, writing to this register has no effect.
W	**WRITE ONLY**.	If a register is write only, reading to this register returns all zero.
R/W	**READ/WRITE**.	A register with this attribute can be read and written.
RC	**READ CLEAR**.	If a register is read clear, reading to this register clears the register to '0'.
R/WC	**READ/WRITE CLEAR**.	A register bit with this attribute can be read and written. However, writing 1 clears the corresponding bit and writing 0 has no effect.

BFNAME@REGNAME This abbreviation may be shown in figures to represent one bit in a register or one field in a register.

The used radix indicator suffixes in this specification are listed below:
Decimal number: "d" suffix or no suffix
Binary number: "b" suffix
Hexadecimal number: "h" suffix

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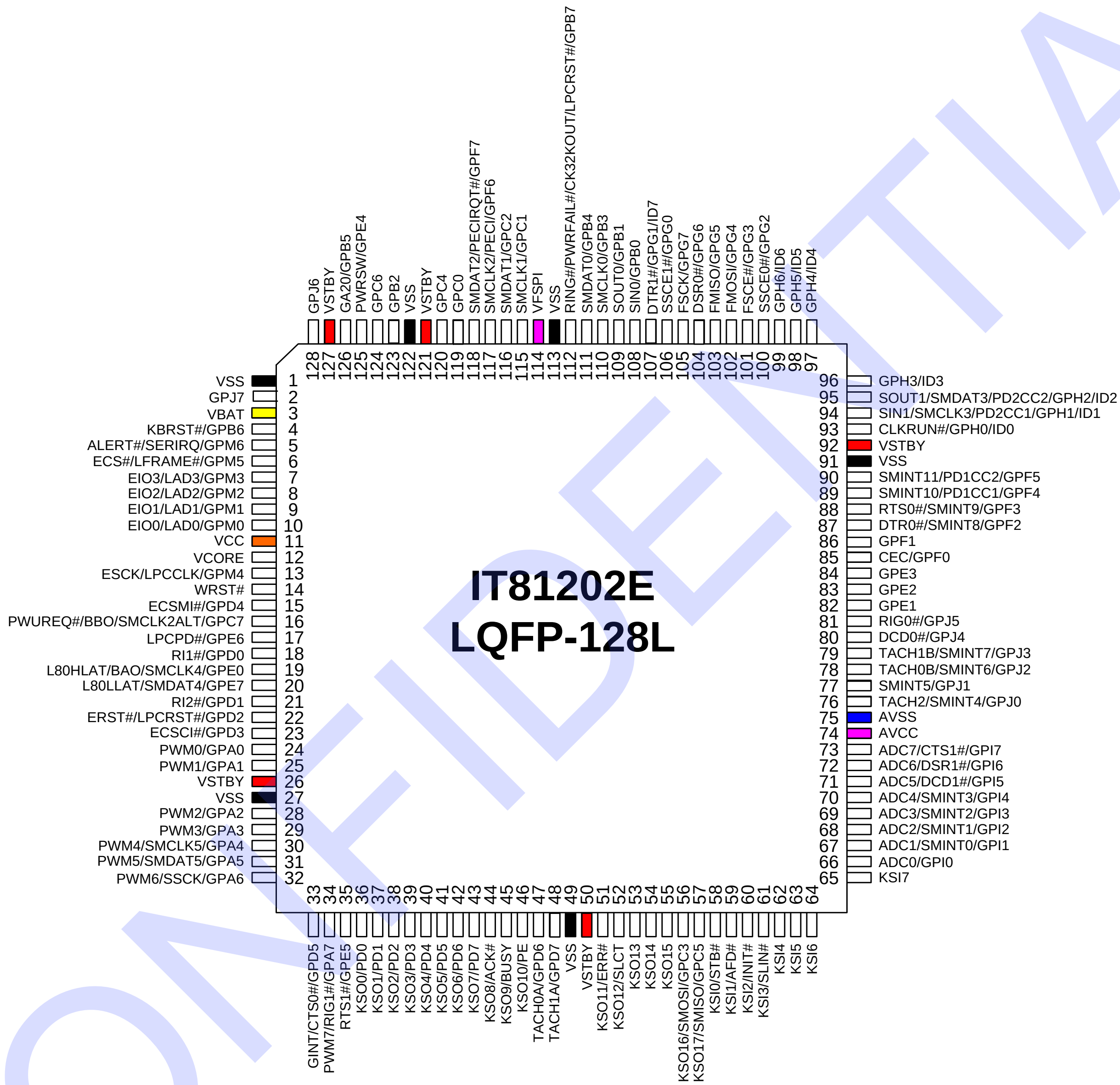
4. Pin Configuration

4.1 Top View

IT81202E Top View



IT81202VG Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7	SMDAT0/GPB4	SOUT0/GPB1	SIN0/GPB0	DTR1#/GPG1/ID7	FMISO/GPG5	FSCE#/GPG3	GPH5/ID5	GPH3/ID3	DTR0#/SMINT8/GPF2	CEC/GPF0	GPE2	GPE1	A
B	SMCLK2/PECI/GPF6	SMDAT1/GPC2	SMCLK1/GPC1	SMCLK0/GPB3	FSCK/GPG7	FMOSI/GPG4	GPH6/ID6	GPH4/ID4	SMINT11/PD1CC2/GPF5	RTS0#/SMINT9/GPF3	GPF1	GPE3	DCD0#/GPJ4	B
C	SMDAT2/PECIRQT#/GPF7	GPC4										RIG0#/GPJ5	TACH1B/SMINT7/GPJ3	C
D	GPC0	GPB2		VSTBY	VFSPI	DSR0#/GPG6	SOUT1/SMDAT3/PD2CC2/GPH2/ID2	CLKRUN#/GPH0/ID0	SMINT10/PD1CC1/GPF4	VSTBY		TACH0B/SMINT6/GPJ2	SMINT5/GPJ1	D
E	GPC6	PWRSW/GPE4		VSTBY	VSS	SSCE1#/GPG0	SSCE0#/GPG2	SIN1/SMCLK3/PD2CC1/GPH1/ID1	AVCC	AVSS		TACH2/SMINT4/GPJ0	ADC7/CTS1#/GPI7	E
F	GA20/GPB5	GPJ6		VSS	VSS				ADC3/SMINT2/GPI3	ADC5/DCD1#/GPI5		ADC6/DSR1#/GPI6	ADC4/SMINT3/GPI4	F
G	GPJ7	ALERT#/SERIRQ/GPM6		VSS	VSS				KSI7	ADC0/GPI0		ADC2/SMINT1/GPI2	ADC1/SMINT0/GPI1	G
H	ECS#/LFRAME#/GPM5	EIO3/LAD3/GPM3		KBRST#/GPB6	VSS				KSI4	KSI5		KSI3/SLIN#	KSI6	H
J	EIO2/LAD2/GPM2	EIO1/LAD1/GPM1		VBAT	VCC	PWM5/SMDAT5/GPA5	KSO1/PD1	KSO5/PD5	KSI2/INIT#	KSO17/SMISO/GPC5		KSI0/STB#	KSI1/AFD#	J
K	EIO0/LAD0/GPM0	ESCK/LPCCLK/GPM4		VSTBY	VCORE	PWM4/SMCLK5/GPA4	PWM7/RIG1#/GPA7	KSO4/PD4	KSO9/BUSY	VSTBY		KSO15	KSO16/SMOSI/GPC3	K
L	WRST#	ECSMI#/GPD4										KSO13	KSO14	L
M	LPCPD#/GPE6	PWUREQ#/BBO/SMCLK2ALT/GPC7	L80LLAT/SMDAT4/GPE7	ERST#/LPCRST#/GPD2	PWM0/GPA0	PWM2/GPA2	PWM6/SSCK/GPA6	KSO0/PD0	KSO3/PD3	KSO7/PD7	TACH0A/GPD6	TACH1A/GPD7	KSO12/SLCT	M
N	RI1#/GPD0	L80HLAT/BAO/SMCLK4/GPE0	RI2#/GPD1	ECSCI#/GPD3	PWM1/GPA1	PWM3/GPA3	GINT/CTS0#/GPD5	RTS1#/GPE5	KSO2/PD2	KSO6/PD6	KSO8/ACK#	KSO10/PE	KSO11/ERR#	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Table 4-1. Pins Listed in Numeric Order (128-pin LQFP)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS	33	GINT/CTS0#/GPD5	65	KSI7	97	GPH4/ID4
2	GPJ7	34	PWM7/RIG1#/GPA7	66	ADC0/GPI0	98	GPH5/ID5
3	VBAT	35	RTS1#/GPE5	67	ADC1/SMINT0/GPI1	99	GPH6/ID6
4	KBRST#/GPB6	36	KSO0/PD0	68	ADC2/SMINT1/GPI2	100	SSCE0#/GPG2
5	ALERT#/SERIRQ/GPM6	37	KSO1/PD1	69	ADC3/SMINT2/GPI3	101	FSCE#/GPG3
6	ECS#/LFRAME#/GPM5	38	KSO2/PD2	70	ADC4/SMINT3/GPI4	102	FMOSI/GPG4
7	EIO3/LAD3/GPM3	39	KSO3/PD3	71	ADC5/DCD1#/GPI5	103	FMISO/GPG5
8	EIO2/LAD2/GPM2	40	KSO4/PD4	72	ADC6/DSR1#/GPI6	104	DSR0#/GPG6
9	EIO1/LAD1/GPM1	41	KSO5/PD5	73	ADC7/CTS1#/GPI7	105	FSCK/GPG7
10	EIO0/LAD0/GPM0	42	KSO6/PD6	74	AVCC	106	SSCE1#/GPG0
11	VCC	43	KSO7/PD7	75	AVSS	107	DTR1#/GPG1/ID7
12	VCORE	44	KSO8/ACK#	76	TACH2/SMINT4/GPJ0	108	SIN0/GPB0
13	ESCK/LPCCLK/GPM4	45	KSO9/BUSY	77	SMINT5/GPJ1	109	SOUT0/GPB1
14	WRST#	46	KSO10/PE	78	TACH0B/SMINT6/GPJ2	110	SMCLK0/GPB3
15	ECSMI#/GPD4	47	TACH0A/GPD6	79	TACH1B/SMINT7/GPJ3	111	SMDAT0/GPB4
16	PWUREQ#/BBO/SMCLK2ALT/GPC7	48	TACH1A/GPD7	80	DCD0#/GPJ4	112	RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7
17	LPCPD#/GPE6	49	VSS	81	RIG0#/GPJ5	113	VSS
18	RI1#/GPD0	50	VSTBY	82	GPE1	114	VFSPI
19	L80HLAT/BAO/SMCLK4/GPE0	51	KSO11/ERR#	83	GPE2	115	SMCLK1/GPC1
20	L80LLAT/SMDAT4/GPE7	52	KSO12/SLCT	84	GPE3	116	SMDAT1/GPC2
21	RI2#/GPD1	53	KSO13	85	CEC/GPF0	117	SMCLK2/PECI/GPF6
22	ERST#/LPCRST#/GPD2	54	KSO14	86	GPF1	118	SMDAT2/PECIRQT#/GPF7
23	ECSCI#/GPD3	55	KSO15	87	DTR0#/SMINT8/GPF2	119	GPC0
24	PWM0/GPA0	56	KSO16/SMOSI/GPC3	88	RTS0#/SMINT9/GPF3	120	GPC4
25	PWM1/GPA1	57	KSO17/SMISO/GPC5	89	SMINT10/PD1CC1/GPF4	121	VSTBY
26	VSTBY	58	KSI0/STB#	90	SMINT11/PD1CC2/GPF5	122	VSS
27	VSS	59	KSI1/AFD#	91	VSS	123	GPB2
28	PWM2/GPA2	60	KSI2/INIT#	92	VSTBY	124	GPC6
29	PWM3/GPA3	61	KSI3/SLIN#	93	CLKRUN#/GPH0/ID0	125	PWRSW/GPE4
30	PWM4/SMCLK5/GPA4	62	KSI4	94	SIN1/SMCLK3/PD2CC1/GPH1/ID1	126	GA20/GPB5
31	PWM5/SMDAT5/GPA5	63	KSI5	95	SOUT1/SMDAT3/PD2CC2/GPH2/ID2	127	VSTBY
32	PWM6/SSCK/GPA6	64	KSI6	96	GPH3/ID3	128	GPJ6

Table 4-2. Pins Listed in Numeric Order (128-pin VFBGA)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7	D4	VSTBY	G9	KSI7	K12	KSO15
A2	SMDAT0/GPB4	D5	VFSPI	G10	ADC0/GPI0	K13	KSO16/SMOSI/GPC3
A3	SOUT0/GPB1	D6	DSR0#/GPG6	G12	ADC2/SMINT1/GPI2	L1	WRST#
A4	SIN0/GPB0	D7	SOUT1/SMDAT3/PD2CC2/GPH2/ID2	G13	ADC1/SMINT0/GPI1	L2	ECSMI#/GPD4
A5	DTR1#/GPG1/ID7	D8	CLKRUN#/GPH0/ID0	H1	ECS#/LFRAME#/GPM5	L12	KSO13
A6	FMISO/GPG5	D9	SMINT10/PD1CC1/GPF4	H2	EIO3/LAD3/GPM3	L13	KSO14
A7	FSCE#/GPG3	D10	VSTBY	H4	KBRST#/GPB6	M1	LPCPD#/GPE6
A8	GPH5/ID5	D12	TACH0B/SMINT6/GPJ2	H5	VSS	M2	PWUREQ#/BBO/SMCLK2ALT/GPC7
A9	GPH3/ID3	D13	SMINT5/GPJ1	H9	KSI4	M3	L80LLAT/SMDAT4/GPE7
A10	DTR0#/SMINT8/GPF2	E1	GPC6	H10	KSI5	M4	ERST#/LPCRST#/GPD2
A11	CEC/GPF0	E2	PWRSW/GPE4	H12	KSI3/SLIN#	M5	PWM0/GPA0
A12	GPE2	E4	VSTBY	H13	KSI6	M6	PWM2/GPA2
A13	GPE1	E5	VSS	J1	EIO2/LAD2/GPM2	M7	PWM6/SSCK/GPA6
B1	SMCLK2/PECI/GPF6	E6	SSCE1#/GPG0	J2	EIO1/LAD1/GPM1	M8	KSO0/PD0
B2	SMDAT1/GPC2	E7	SSCE0#/GPG2	J4	VBAT	M9	KSO3/PD3
B3	SMCLK1/GPC1	E8	SIN1/SMCLK3/PD2CC1/GPH1/ID1	J5	VCC	M10	KSO7/PD7
B4	SMCLK0/GPB3	E9	AVCC	J6	PWM5/SMDAT5/GPA5	M11	TACH0A/GPD6
B5	FSCK/GPG7	E10	AVSS	J7	KSO1/PD1	M12	TACH1A/GPD7
B6	FMOSI/GPG4	E12	TACH2/SMINT4/GPJ0	J8	KSO5/PD5	M13	KSO12/SLCT
B7	GPH6/ID6	E13	ADC7/CTS1#/GPI7	J9	KSI2/INIT#	N1	RI1#/GPD0
B8	GPH4/ID4	F1	GA20/GPB5	J10	KSO17/SMISO/GPC5	N2	L80HLAT/BAO/SMCLK4/GPE0
B9	SMINT11/PD1CC2/GPF5	F2	GPJ6	J12	KSI0/STB#	N3	RI2#/GPD1
B10	RTS0#/SMINT9/GPF3	F4	VSS	J13	KSI1/AFD#	N4	ECSCI#/GPD3
B11	GPF1	F5	VSS	K1	EIO0/LAD0/GPM0	N5	PWM1/GPA1
B12	GPE3	F9	ADC3/SMINT2/GPI3	K2	ESCK/LPCCLK/GPM4	N6	PWM3/GPA3
B13	DCD0#/GPJ4	F10	ADC5/DCD1#/GPI5	K4	VSTBY	N7	GINT/CTS0#/GPD5
C1	SMDAT2/PECIRQT#/GPF7	F12	ADC6/DSR1#/GPI6	K5	VCORE	N8	RTS1#/GPE5
C2	GPC4	F13	ADC4/SMINT3/GPI4	K6	PWM4/SMCLK5/GPA4	N9	KSO2/PD2
C12	RIG0#/GPJ5	G1	GPJ7	K7	PWM7/RIG1#/GPA7	N10	KSO6/PD6
C13	TACH1B/SMINT7/GPJ3	G2	ALERT#/SERIRQ/GPM6	K8	KSO4/PD4	N11	KSO8/ACK#
D1	GPC0	G4	VSS	K9	KSO9/BUSY	N12	KSO10/PE
D2	GPB2	G5	VSS	K10	VSTBY	N13	KSO11/ERR#

5. Pin Descriptions

5.1 Pin Descriptions

Table 5-1. Pin Descriptions of 3.3V/1.8V LPC Bus Interface

Pin(s) No.	Signal	Attribute	Description
LPC Bus Interface (3.3V/1.8V CMOS I/F) (Supplied by VCC)			
13	**LPCCLK**	PI	***LPC Clock*** 19.2MHz to 33MHz clock for LPC domain functions
7-10	**LAD[3:0]**	PIO	***LPC Address Data***
6	**LFRAME#**	PI	***LPC LFRAME# Signal***
5	**SERIRQ**	PIO	***SERIRQ Signal*** This pin is supplied by VCC.

Table 5-2. Pin Descriptions of eSPI Bus Interface

Pin(s) No.	Signal	Attribute	Description
eSPI Bus Interface (1.8V CMOS I/F) (Supplied by VCC)			
13	**ESCK**	IK	***eSPI Clock*** 20MHz to 66MHz for eSPI domain functions.
7-10	**EIO[3:0]**	EIO	***eSPI Bi-directional Data***
6	**ECS#**	IK	***eSPI Chip Select***
5	**ALERT#**	EIO	***Alert***

Table 5-3. Pin Descriptions of eSPI Bus Interface

Pin(s) No.	Signal	Attribute	Description
eSPI Bus Interface (1.8V CMOS I/F)			
22	**ERST#**	IK	***eSPI Reset*** Note this pin takes effect after setting 'Input Voltage Selection' to 1.8V.

Table 5-4. Pin Descriptions of LPC Bus Interface

Pin(s) No.	Signal	Attribute	Description
LPC Bus Interface (3.3V CMOS I/F)			
22	**LPCRST#**	IK	***LPC Hardware Reset*** LPC hardware reset will reset LPC interface and host side modules. The source is determined by EC side register bit LPCRSTEN. This pin can be omitted if external LPC reset is not required.
17	**LPCPD#**	IO2	***LPC LPCPD# Signal***
93	**CLKRUN#**	IO16	***LPC CLKRUN# Signal***
15	**ECSMI#**	O8	***EC SMI# Signal*** This is SMI# signal driven by SWUC module.
23	**ECSCI#**	O8	***EC SCI# Signal*** This is SCI# signal driven by PMC module.
126	**GA20**	IO2	***Gate A20 Signal*** This is GA20 signal driven by SWUC module.
4	**KBRST#**	IO2	***KB Reset Signal*** This is KBRST# signal driven by SWUC module.
14	**WRST#**	IK	***Warm Reset*** For EC domain function, reset after power up.
16	**PWUREQ#**	O16	***System Power On Request*** This is PWUREQ# signal driven by SWUC module.
19	**L80HLAT**	O16	***LPC I/O Port 80, High-nibble LAD Latch*** An active high signal to latch Port 80 high-nibble for the debug purpose.
20	**L80LLAT**	O16	***LPC I/O Port 80, Low-nibble LAD Latch*** An active high signal to latch Port 80 low-nibble for the debug purpose.

Table 5-5. Pin Descriptions of SPI Slave Interface

Pin(s) No.	Signal	Attribute	Description
SPI Slave Interface (3.3V/1.8V CMOS I/F) (Supplied by VCC)			
13	**ESCK**	IK	***SPI Clock*** 20MHz to 66MHz for eSPI domain functions.
9	**EIO[1]**	O8	***SPI Data Out*** Connected to SI of SPI host
10	**EIO[0]**	IOK8	***SPI Data In*** Connected to SO of SPI host
6	**ECS#**	IK	***SPI Chip Select***
5	**ALERT#**	PIO	***Alert***

Table 5-6. Pin Descriptions of 3.3V/1.8V External Serial Flash Interface (FSPI)

Pin(s) No.	Signal	Attribute	Description
External Serial Flash Interface (3.3V/1.8V CMOS I/F) (Supplied by VFSPI)			
105	**FSCK**	O8	***Serial Flash Clock*** Clock to external serial flash.
101	**FSCE#**	O8	***Serial Flash Chip Enable*** Connected to CE# of serial flash.
102	**FMOSI**	IOK8	***Serial Flash In*** Connected to SI of serial flash.
103	**FMISO**	IOK8	***Serial Flash Out*** Connected to SO of serial flash.

Note: Please do not place any pull-up resistor on these FSPI pins to reduce power consumption.

Table 5-7. Pin Descriptions of Serial Master Interface (SSPI)

Pin(s) No.	Signal	Attribute	Description
Serial Peripheral Interface (3.3V CMOS I/F)			
32	**SSCK**	O8	***SSPI Clock*** Clock to external device.
106,100	**SSCE1#, SSCE0#**	O8, O4	***SSPI Chip Enable*** Connected to SSCE# of SPI device.
56	**SMOSI**	O8	**SSPI Master Out/Slave In** Connected to SI of 4-wire SPI device.
57	**SMISO**	IOK8	**SSPI Master In/Slave Out** Connected to SO of 4-wire SPI device or connected to SIO of 3-wire SPI device.

Table 5-8. Pin Descriptions of Keyboard Matrix Scan Interface

Pin(s) No.	Signal	Attribute	Description
KB Matrix Interface (3.3V CMOS I/F)			
57-51, 46-36	**KSO[17:0]**	O8	***Keyboard Scan Output*** Keyboard matrix scan output.
65-58	**KSI[7:0]**	IK	***Keyboard Scan Input*** Keyboard matrix scan input for switch based keyboard.

Table 5-9. Pin Descriptions of 3.3V/1.8V SMBus Interface

Pin(s) No.	Signal	Attribute	Description
SMBus Interface (3.3V/1.8V CMOS I/F)			
110, 115, 117, 16, 94, 19, 30	**SMCLK0, SMCLK1, SMCLK2, SMCLK2ALT SMCLK3, SMCLK4, SMCLK5**	IOK4, IOK4, IOK4, IOK16, IOK16, IOK16, IOK8	***SMBus CLK*** 6 SMBus interface provided.

Pin(s) No.	Signal	Attribute	Description
111, 116, 118, 95 20, 31	**SMDAT0, SMDAT1, SMDAT2, SMDAT3, SMDAT4, SMDAT5**	IOK4, IOK4, IOK4, IOK16, IOK16, IOK8	***SMBus Data*** 6 SMBus interface provided.

Table 5-10. Pin Descriptions of PWM Interface

Signal	Pin(s) No.	Attribute	Description
PWM Interface (3.3V CMOS I/F)			
34, 32-28, 25-24	**PWM[7:4], PWM[3:0]**	O8, O16	***Pulse Width Modulation Output*** These are general-purpose PWM signals. PWM0-7 correspond to channel 0-7 respectively.
76, 48, 79, 47, 78	**TACH2 TACH1A TACH1B TACH0A TACH0B**	IK	***Tachometer Input*** These are tachometer inputs from external fans. They are used for measuring the external fan speed. TACH2 is for color sensor.

Table 5-11. Pin Descriptions of Wake Up Control Interface

Pin(s) No.	Signal	Attribute	Description
Wake Up Control Interface (3.3V CMOS I/F)			
Refer to Table 7-4. WUC Input Assignme nts	**WUI[86:80] WUI[74:32] WUI[31:16] WUI[15:0]**	IK	***EC Wake Up Input*** Supplied by VSTBY, used for EC wake up.
125	**PWRSW**	IK	***Power Switch Input*** Supplied by VSTBY, used to indicate the status of power switch.
21,18	**RI[2:1]#**	IK	***Ring Indicator Input*** Supplied by VSTBY, used for system wake up.
112	**RING#**	IK	***Telephone Line Ring Input*** Supplied by VSTBY, used for system wake up.
112	**PWRFAIL#**	IK	***Power Fail Input***

Table 5-12. Pin Descriptions of Serial Port (UART) Interface

Pin(s) No.	Signal	Attribute	Description
Serial Port Interface (3.3V CMOS I/F)			
94,108	**SIN[1:0]**	IOK16	***Serial Data Input*** This input receives serial data from the communications link.
95,109	**SOUT[1:0]**	IOK16	***Serial Data Output*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
72,104	**DSR[1:0]#**	AI / IK	***Data Set Ready*** When the signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
35,88	**RTS[1:0]#**	O2	***Request to Send*** When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state.
73,33	**CTS[1:0]#**	AI / IK	***Clear to Send*** When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Pin(s) No.	Signal	Attribute	Description
34,81	**RIG[1:0]#**	IK	***Ring Indicator*** When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
71,80	**DCD[1:0]#**	AI / IK	***Data Carrier Detect*** When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
107,87	**DTR[1:0]#**	O16	***Data Terminal Ready*** DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state.

Table 5-13. Pin Descriptions of Platform Environment Control Interface (PECI)

Pin(s) No.	Signal	Attribute	Description
Platform Environment Control Interface Interface (3.3V CMOS I/F)			
117	**PECI**	PECI	***PECI*** This bi-directional pin provides data communication between the PECI host and devices.
118	**PECIRQT#**	O4	***PECI Request*** The PECI request is output to PECI devices. When this pin goes low, it requests the system to make the PECI bus available.

Table 5-14. Pin Descriptions of Hardware Bypass (HWBP)

Pin(s) No.	Signal	Attribute	Description
Hardware Bypass (HWBP) Interface (3.3V CMOS I/F)			
19	**BAO**	O16	***Buffer A Output*** Hardware bypass path from GPI6 to BAO.
16	**BBO**	O16	***Buffer B Output*** Hardware bypass path from GPI7 to BBO.

Table 5-15. Pin Descriptions of Parallel Port Interface

Pin(s) No.	Signal	Attribute	Description
Parallel Port Interface (3.3V CMOS I/F)			
52	**SLCT**	O8	***Printer Select***
46	**PE**	O8	***Printer Paper End***
45	**BUSY**	O8	***Printer Busy***
44	**ACK#**	O8	***Printer Acknowledge***
61	**SLIN#**	IK	***Printer Select Input***
60	**INIT#**	IK	***Printer Initialize***
51	**ERR#**	O8	***Printer Error***
59	**AFD#**	IK	***Printer Auto Line Feed***
58	**STB#**	IK	***Printer Strobe***
43-36	**PD[7:0]**	O8	***Parallel Port Data[7:0]***

*: The interface can be connected to parallel port of computer through ITE-specified cable. The programmer can directly read/write flash through this interface.

Table 5-16. Pin Descriptions of GPIO Interface

Pin(s) No.	Signal	Attribute	Description
GPIO Interface (3.3V CMOS I/F)			
Refer to Pins List Table	**GPA[7:0], GPB[7:0], GPC[7:0], GPD[7:0], GPE[7:0], GPF[7:0], GPG[7:0], GPH[6:0], GPI[7:0], GPJ[7:0], GPM[6:0]**	IOK	***GPIO Signals*** The GPIO pins are divided into groups. Some GPIO pins have alternative function. **PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPG[7, 5:3]. GPG6 must be pulled up. (Reserved hardware strapping)**. GPG2 is pulled up if FSPI I/F is used, and pulled down if otherwise.
33	**GINT**	IK	***General Purpose Interrupt*** General Purpose Interrupt directly input to INT28 of INTC.

Table 5-17. Pin Descriptions of Hardware Strap

Pin(s) No.	Signal	Attribute	Description
Hardware Strap (3.3V CMOS I/F)			
107, 99-93	**ID[7:0]**	IK	***Identify Input*** These hardware straps are used to identify the version for firmware usage. These input signals will be latched when the VSTBY powers up. Note that these hardware straps are only available if these pins are not driven by other components on PCB. The default is without the pull-up or down resistor.
63, 62, 60, 59	**KSI[5, 4, 2, 1]**	IK	The 0011b is the entry of DBGR/EPP.
105, 119, 103, 102, 101, 100	**GPG[7:2]**	IK	These pins are the entry of the test mode. The 010000b is the normal mode.
125	**GPG0**	IK	Voltage Comparator Enable This hardware strap is enabled if there is an external pull-up resistor, while disabled if pull-down resistor. **Note:** Only for voltage comparator 0

*: The strapped pin will be strapped 1b if it is pulled up. The strapped pin will be strapped 0b if it is pulled down or not pulled. The strapped pin will be strapped an unknown value if it is driven.

Table 5-18. Pin Descriptions of ADC Input Interface

Pin(s) No.	Signal	Attribute	Description
ADC Interface			
73-66	**ADC[7:0]**	AI	**ADC Input/Alternate GPIO** These 8 ADC inputs can be used as GPIO ports depending on the ADC channels required.

Table 5-19. Pin Descriptions of 3.3V/1.8V SMB/I2C Interrupt Input

Pin(s) No.	Signal	Attribute	Description
SMB/I2C Interrupt (3.3V/1.8V CMOS I/F)			
90-87, 79-76, 70-67	**SMINT[11:0]**	IK	***SMB/I2C Interrupt Input*** These interrupt input pins can be used to trigger the I2C controller hardware in auto-mode.

Table 5-20. Pin Descriptions of Clock

Pin(s) No.	Signal	Attribute	Description
Clock Interface (3.3V CMOS I/F)			
112	**CK32KOUT**	O16	**32.768 kHz Oscillator Output** 32.768 kHz clock output.

Table 5-21. Pin Descriptions of USBPD

Pin(s) No.	Signal	Attribute	Description
USBPD Interface			
89	**PD1CC1**	AIO	***Configuration Channel 1 of Port 1***
90	**PD1CC2**	AIO	***Configuration Channel 2 of Port 1***
94	**PD2CC1**	AIO	***Configuration Channel 1 of Port 2***
95	**PD2CC2**	AIO	***Configuration Channel 2 of Port 2***

Table 5-22. Pin Descriptions of Power/Ground Signals

Pin(s) No.	Signal	Attribute	Description
Power Ground Signals			
1, 27, 49, 91,113, 122	**VSS**	I	***Ground*** Digital ground.
11	**VCC**	I	***LPC Bus Power Supply of 3.3V/1.8V*** The power supply of LPC/eSPI and related functions, which is the main power of system.
26, 50, 92, 121, 127	**VSTBY**	I	***Standby Power Supply of 3.3V*** The power supply of EC domain functions, which is the standby power of system.
114	**VFSPI**	I	***Standby Power Supply of 3.3V/1.8V*** This pin supplies the I/O power of FSCK/FSCE#/FMOSI/FMISO/SERIRQ. If the external SPI flash is used, the power level of the flash must be the same as that of the VFSPI pin. The power pin must be supplied as well if VCC is supplied. It's allowed to let {VSTBY,VFSPI}={on,off} and the FSPI I/F must be disabled by the setting in 16B-signature if the configuration of EC power-on is {VSTBY,VFSPI}={on,off},
12	**VCORE**	I/O	***Core Power Bypass*** Internal core power output. The external capacitor is required to be connected between this pin and VSS and physically close to this pin. The capacitor type must be low-ESR and MLCC is required.
3	**VBAT**	I	***Battery Power Supply of 3.3V*** The power supply for BRAM.
75	**AVSS**	I	***Analog Ground for Analog Component***
74	**AVCC**	I	***Analog VCC for Analog Component***

Note: I/O cell types are described below:

I:	Input PAD.
AI:	Analog Input PAD.
IK:	Schmitt Trigger Input PAD.
IKD:	Schmitt Trigger Input PAD (integrated one pull-down resistor).
PI:	PCI Bus Specified Input PAD.
PIO:	PCI Bus Specified Input/Output PAD.
EIO:	eSPI Bus Specified Input/Output PAD.
OSCI:	Oscillator Input PAD.
AO:	Analog Output PAD.
O2:	2 mA Output PAD.
O4:	4 mA Output PAD.
O6:	6 mA Output PAD.
O8:	8 mA Output PAD.
AIO2:	2 mA Bidirectional PAD with Analog Input PAD.
IOK2:	2 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK4:	4 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK6:	6 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK8:	8 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK16:	16 mA Bidirectional PAD with Schmitt Trigger Input PAD.
PECI:	Special design for PECI interface.

All input pins aren't 5V tolerant, except those with the "5VT" field checked in the table "GPIO Alternate Function" of specification v3.0 or above.

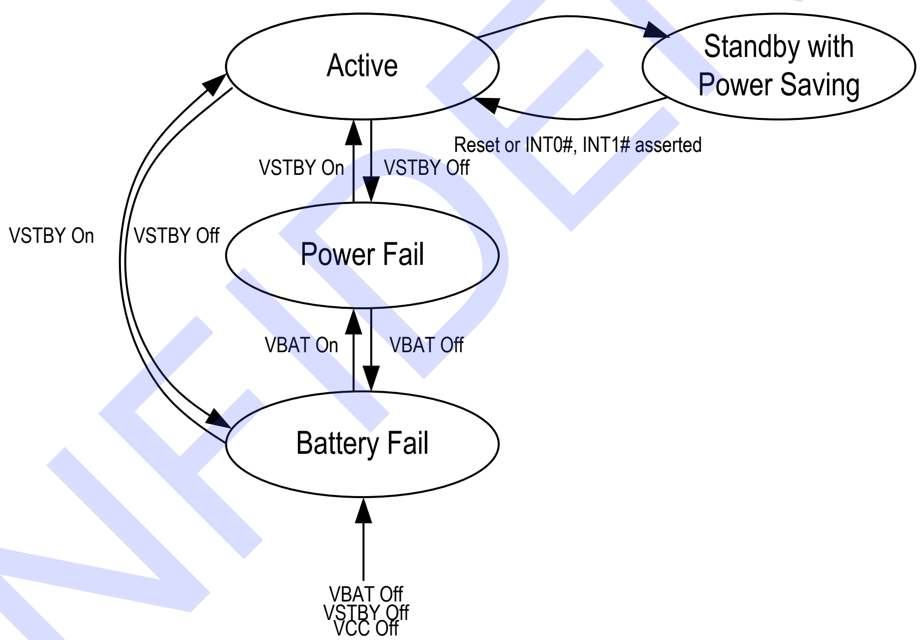
5.2 Chip Power Planes and Power States

Table 5-23. Power States

Power State	VSTBY/AVCC pin	VBAT pin
Active	Supplied	Supplied or Not
Active with Power Saving	Supplied EC is in Doze or Sleep Mode	Supplied or Not
Standby	Supplied	Supplied or Not
Standby with Power Saving	Supplied EC is in Doze or Sleep Mode	Supplied or Not
Power Fail	Not Supplied	Supplied
Battery Fail	Not Supplied	Not Supplied

Note:
(1) The AVCC should be derived from VSTBY.
(2) All other combinations of VCC / VSTBY / VBAT are invalid.
(3) In Power Saving mode, CPU program counter is stopped and no instruction will be executed no matter whether EC Clock is running or not.

Figure 5-1. Power State Transitions



5.3 Pin Power Planes and States

In the following tables of this section, Standby means that the VCC is not valid but VSTBY is supplied (S3, S4 or S5) and EC is in normal operation. Standby with Sleep means that CPU and most of its functions are out of work due to PLL power-down while VSTBY is still supplied.

Here are the abbreviations used in the following tables:
H means that EC drives high or is driven high.
L means that EC drives low or is driven low or the output pin powers off.
Z means that EC tri-states the I/O pin or output pin with enable.
RUN means that Output or I/O pins are in normal operation.
Driven means that the input pin is driven by the connected chip or logic.
STOP means that the output pin keeps its logical level before the clock is stopped.
OFF means that I/O pin powers off.

Note that reset sources of 'Reset Finish' columns depend on Reset Types and Applied Module Table and it means the reset is finished when its corresponding power plane is supplied.
Note that GPIO pins listed in different functional tables except the GPIO table indicate their pin status of the corresponding alternative function.

Table 5-24. Pin States of LPC Bus Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
LPCRST# (Y)	VSTBY	Driven	L	L	L
LPCCLK	VCC	Driven	L	L	L
LAD[3:0]	VCC	RUN	OFF	OFF	OFF
LFRAME#	VCC	Driven	L	L	L
SERIRQ	VCC	Z	OFF	OFF	OFF
LPCPD# (Y)	VSTBY	Table 7-8	L	L	L
CLKRUN# (Y)	VSTBY	Table 7-8	OFF	L	OFF
ECSMI#	VSTBY	Table 7-8	RUN	Z	OFF
ECSCI# (Y)	VSTBY	Table 7-8	RUN	Z	OFF
GA20 (Y)	VSTBY	Table 7-8	RUN	STOP	OFF
KBRST# (Y)	VSTBY	Table 7-8	RUN	STOP	OFF
WRST#	VSTBY	Driven	Driven	Driven	L
PWUREQ#	VSTBY	Table 7-8	RUN	STOP	OFF
L80HLAT (Y)	VSTBY	Table 7-8	L	L	OFF
L80LLAT (Y)	VSTBY	Table 7-8	L	L	OFF

Table 5-25. Pin States of Keyboard Matrix Scan Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
KSO	VSTBY	L	RUN	STOP	OFF
KSI	VSTBY	Driven	Driven	Driven	L

Table 5-26. Pin States of SMBus Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
SMCLK (Y)	VSTBY	Table 7-8	RUN	Z	OFF
SMDAT (Y)	VSTBY	Table 7-8	RUN	Z	OFF

Table 5-27. Pin States of PWM Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
PWM (Y)	VSTBY	Table 7-8	RUN	STOP	OFF

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
TACH (Y)	VSTBY	Table 7-8	Driven	Driven	OFF

Table 5-28. Pin States of Wake Up Control Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
WUI (Y)	VSTBY	Table 7-8	Driven	Driven	OFF
PWRSW (Y)	VSTBY	Table 7-8	Driven	Driven	OFF
RI (Y)	VSTBY	Table 7-8	Driven	Driven	OFF
RING# (Y)	VSTBY	Table 7-8	Driven	Driven	OFF
PWRFAIL# (Y)	VSTBY	Table 7-8	Driven	Driven	OFF

Table 5-29. Pin States of SSPI Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
SSCE# (Y)	VSTBY	Table 7-8	RUN	STOP	OFF
SSCK (Y)	VSTBY	Table 7-8	RUN	STOP	OFF
SMOSI (Y)	VSTBY	Table 7-8	RUN	STOP	OFF
SMISO (Y)	VSTBY	Table 7-8	Driven	Driven	OFF

Table 5-30. Pin States of Serial Port Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
SIN (Y)	VSTBY	Table 7-8	Driven	Driven	OFF
SOUT (Y)	VSTBY	Table 7-8	RUN	STOP	OFF
CTS # (Y)	VSTBY	Table 7-8	Driven	Driven	OFF
DSR # (Y)	VSTBY	Table 7-8	Driven	Driven	OFF
DCD # (Y)	VSTBY	Table 7-8	Driven	Driven	OFF
RIG # (Y)	VSTBY	Table 7-8	Driven	Driven	OFF
DTR # (Y)	VSTBY	Table 7-8	RUN	STOP	OFF
RTS # (Y)	VSTBY	Table 7-8	RUN	STOP	OFF

Table 5-31. Pin States of GPIO Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
GPA0…	VSTBY	Table 7-8	Depends on its mode	STOP	OFF

Table 5-32. Pin States of ADC Input Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
ADC (Y)	AVCC	Driven	Driven	Driven	L

5.4 PWRFAIL# Interrupt to INTC

The firmware may use the PWRFAIL# to do some necessary response if VSTBY is being lost.

5.5 Reset Sources and Types

Table 5-33. Reset Sources

Reset Sources	Description
VSTBY Power-Up Reset	Activated after VSTBY is powered up and PLL is stable It takes t_{PLLS} for PLL stabling, and the external flash has to be ready before VSTBY Power-Up Reset finish
VCC Power-Up Reset	Activated after VCC is powered up
Warm Reset	Activated if WRST# is asserted
LPC Hardware Reset	Activated if LPCRST# is asserted
Watch Dog Reset	Activated if External WDT time-out

Table 5-34. Reset Types and Applied Module

Reset Types	Sources	Applied Module
Host Domain Hardware Reset	Warm Reset, VCC Power-Up Reset or LPC Hardware Reset LPC Hardware Reset may be unused See also LPCRSTEN in GCR register.	LPC, PNPCFG, Logical Devices and EC2I
Host Domain Software Reset	Super I/O Software Reset	PNPCFG, Logical Devices and EC2I
EC Domain Reset	Warm Reset, VSTBY Power-Up Reset or Watch Dog Reset	EC Domain

The WRST# should be driven low for at least t_{WRSTW} before going high (Refer to Table 10-3. Warm Reset AC Table on page 571).

If the firmware wants to assert an EC Domain Reset, start an internal of external watchdog without clearing its counter or write invalid data to EWDKEYR register (refer to EWDKEYEN and EWDKEYR registers).
If the firmware wants to determine the source of the last EC Domain Reset, use LRS field in RSTS register.

5.5.1 Related Interrupts to INTC

- Interrupt to INTC

LPCRST# may come from pin LPCRST#/WUI4/GPD2 or RING#/PWRFAIL#/LPCRST#/GPB7. Both pins have another interrupt related alternative function. LPCRST# can be treated as an orthogonal input and LPCRST# event can be handled in the same interrupt routine of another alternative function.

5.6 Chip Power Mode and Clock Domain

Table 5-35. Clock Types

Types	Description
32.768 k Clock	32.768 kHz generated by internal clock generator.
PLL Clock	Clock (frequency = FreqPLL) generated by internal PLL which feds 32.768 k PLL Clock is also the base clock of the CPU core. (FreqPLL is listed in Table 10-2 on page 570
EC Clock	It's from internal PLL and its frequency is listed in Table 10-2 on page 570
Embedded Flash Clock	The clock (frequency = FreqFND) of the embedded flash varies from 2 conditions. System-boot: The frequency is FreqPLL/(CLK_FND_DIV_SEL+1) Run-time: The frequency is FreqPLL/((CLK_FND_DIV_SEL+1)*2) (FreqFND is listed in Table 10-2 on page 570)
Host LPC Clock	19.2MHz to 33MHz from LPCCLK pin and applied on Host Domain.

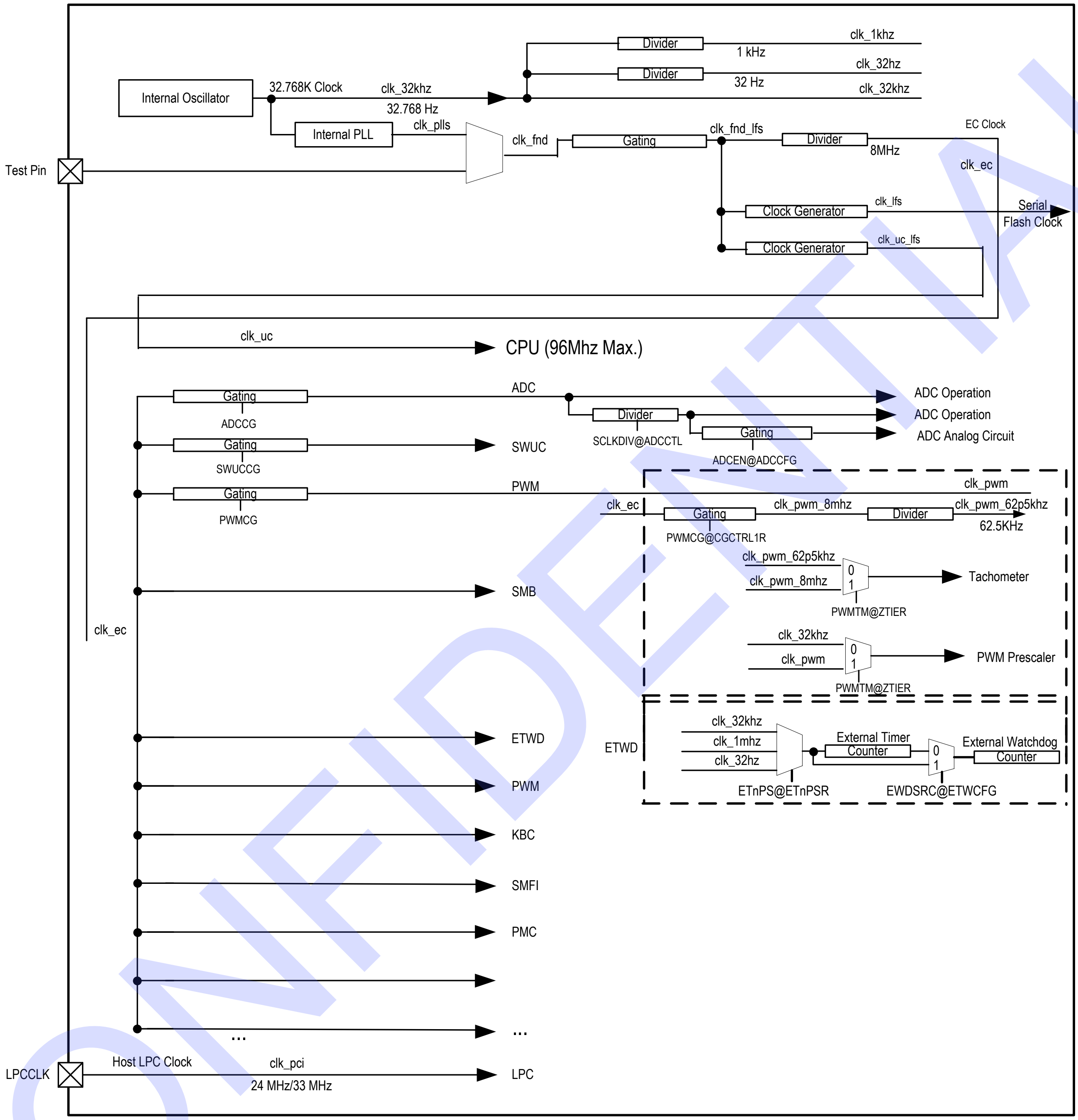
The CPU can enter Doze/Deep Doze/Sleep mode to reduce some power consumption. After entering Doze/Deep Doze/Sleep mode, clock of CPU is stopped but the external timer still works. Also see Table 5-38 on page 31 for the detail.

The way to wake up CPU from Doze/Deep Doze/Sleep mode is to enable external interrupts or hardware reset. Firmware may set PLLCTRL bit before executing STANDBY instruction to enter the Sleep mode since stopping PLL can reduce more power consumption, but it takes more time to wake up from Sleep mode due to waiting for PLL being stable. The steps to enter and exit Doze/Deep Doze/Sleep are listed below:
(a) Set related bits of IE register if they are cleared.
(b) Set channels of WUC which wants to wake up CPU and disable unwanted channels.
(c) Set channels of INTC which wants to wake up CPU and disable unwanted channels.
(d) Set PLLCTRL bit for Sleep mode, or clear it for Doze mode.
(e) Execute STANDBY instruction to enter the Doze/Deep Doze/Sleep mode.
(f) CPU waits for an interrupt to wake up.
(g) After an interrupt is asserted, CPU executes the corresponding interrupt routine and returns the next instruction after excuting STANDBY instruction.

The following figure describes the drivers and branches of the four clocks.
In this figure, clk_32kHz represents 32.768 k Clock; clk_uc represents the CPU core clock; clk_fnd and its branches represent EC Clock; clk_pci represents LPC Clock.

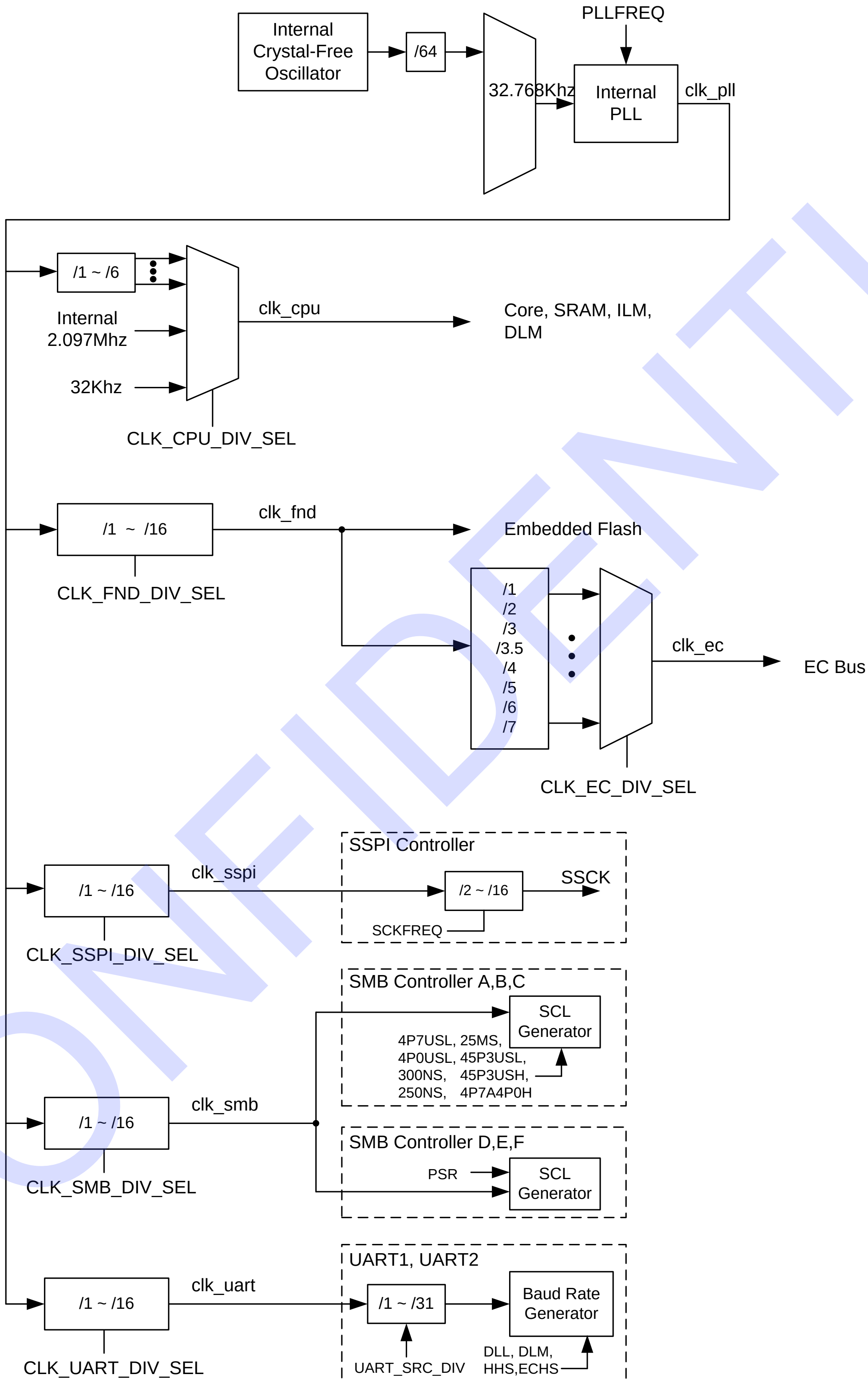
IT81202 has a built-in clock generator, which can generates 32.768kHz clock without an external crystal oscillator. This feature is called "Crytal-Free" and can be activated by the 16B-signature(refer to description of 8th byte's bit 4 in section 6.4.3.12.1 on page 116). Also, IT81202 works well in the presence of an external crystal oscillator.

Figure 5-2. Clock Tree



FreqPLL/FreqEC are listed in Table 10-2 on page 570.

Figure 5-3. Detailed Clock Tree of PLL, CPU, SSPI, SMB, and UART



The following table is the recommended setting of PLL, CPU, FND, EC clock when PLL frequency differs from 8MHz ~ 96MHz. Any clock setting except this recommended value is not guaranteed.

Table 5-36. Suggested System Clock Setting

NO.	PLLFREQ	PLL Clock	CLK_CPU_DIV_SEL	CPU Clock	CLK_FND_DIV_SEL	FND Clock
1	0001b	16Mhz	0001b	8Mhz	000b	16Mhz
2	0001b	16Mhz	0000b	16Mhz	000b	16Mhz
3	0010b	24Mhz	0000b	24Mhz	000b	24Mhz
4	0011b	32Mhz	0000b	32Mhz	001b	16Mhz
5	0100b	48Mhz	0000b	48Mhz	010b	16Mhz
6	0101b	64Mhz	0000b	64Mhz	011b	16Mhz
7	0110b	72Mhz	0000b	72Mhz	010b	24Mhz
8	0111b	96Mhz	0000b	96Mhz	101b	16Mhz

NO.	CLK_EC_DIV_SEL	EC Clock	Support USB	Support SHA-1
1	0001b	8Mhz	No	Yes
2	0001b	8Mhz	No	Yes
3	0010b	8Mhz	No	No
4	0001b	8Mhz	No	Yes
5	0001b	8Mhz	Yes	Yes
6	0001b	8Mhz	No	Yes
7	0010b	8Mhz	No	No
8	0001b	8Mhz	Yes	Yes

Table 5-37. Power Saving by EC Clock Operation Mode

Mode	Item	Description
Normal	Enter	VSTBY is supplied and hardware reset done
	Exit	Enter other modes
	32.768 k Clock	On
	PLL	On
	EC Domain Clock	Driven by PLL
	CPU Clock	Programmable by application (Max. 96MHz)
	Comment	Power consumption can be reduced by selectively disabling unused modules (refer to ECPM module)
Doze	Enter	Execute STANDBY instruction
	Exit	Interrupt from INTC or hardware reset
	32.768 k Clock	On
	PLL	On, clearing PLLCTRL of ECPM module is required
	EC Domain Clock	Driven by PLL
	CPU Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Deep Doze	Enter	Execute STANDBY instruction
	Exit	Interrupt from INTC or hardware reset
	32.768 k Clock	On
	PLL	D2EC disabled: On but gated D2EC enabled: On
	EC Domain Clock	Off
	CPU Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)

Mode	Item	Description
Sleep	Enter	Execute STANDBY instruction
	Exit	Interrupt from INTC or hardware reset
	32.768 k Clock	On
	PLL	D2EC disabled: Off, setting PLLCTRL of ECPM module is required D2EC enabled: On
	EC Domain Clock	Driven by PLL
	CPU Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)

Table 5-38. Module Status in Each Power State/Clock Operation

Power State and/or Clock Operation	Running Module	Stopped Module	Off Module	Note
Active Active with Power Saving	LPC, PNPCFG, EC2I, host parts of SMFI/ SWUC/ KBC/ PMC / BRAM			List host related modules only
Standby Standby with Power Saving			LPC, PNPCFG, EC2I, host parts of SMFI/ SWUC/ KBC/ PMC	List host related modules only
Active with Doze Mode Standby with Doze Mode	All other EC modules	CPU		List EC modules only
Active with Deep Doze/Sleep Mode Standby with Deep Doze/Sleep Mode	GPIO, WUC and its sources, INTC and its sources from running modules, SWUC wakeup logic, PWM channel outputs, KBS, ETWD, BRAM	All other EC modules		List all
Power Fail	BRAM		All others	List all
Battery Fail			All	List all

Note: Running module means this module works well.
Stopped module means this module is frozen because its clock is stopped.
Off module means this module is turned off due to power lost.

5.7 Pins with Pull, Schmitt-Trigger or Open-Drain Function

Table 5-39. Pins with Pull Function

Pin	Pull Function	Note
KSI[7:0]	Programmable 75k pull-up resistor	Default off
KSO[17:0]	Programmable 75k pull-up resistor	Default off
GPIO with pull capability and their alternative functions	Programmable 75k pull-up/down resistor	For the detailed pull capability and default on/off , please refer to the table “GPIO Alternate Function” of specification v3.0 or above.
ID7-0	Operational 75k pull-down resister	Default off No pull up or down during VSTBY power on to process the hardware strap function

Note: 75k ohm is a typical value. Refer to section 6 DC Characteristics on page 567 for the detail.

Table 5-40. Pins with Schmitt-Trigger Function

Pin	Pull Function	Note
All GPIO pins except GPIO group I/J and their alternative functions	Fixed Schmitt-Trigger Input	
KSI[7:0]	Fixed Schmitt-Trigger Input	
WRST#	Fixed Schmitt-Trigger Input	

Table 5-41. Signals with Open-Drain Function

Signal	Open-Drain Function	Note
CLKRUN#	Open-drain output signal	
KSO	Programmable open-drain output signal	Default is push-pull
SMCLK, SMDAT	Open-drain bi-directional signal	
ECSCI#, ECSMI#, PWUREQ#	Open-drain output signal	
GPIO with open-drain capability and their alternative functions (Other GPIO pin(s) can support open-drain by setting its(their) GPDR register(s) as 0 and switch GPMD field in GPCR register between input and output mode.)	Programmable open-drain output signal	Default is push-pull

5.8 Pins with 1.8V Input/Output

IT81202 supports 3.3V/1.8V LPC and FSPI interface. It also supports 1.8V input for some GPIOs, suitable for 1.8V open-drain applications like I2C. The setting of these voltage switches are shown below.

Table 5-42. Pins with 1.8V Input/Output

Function	Pin	1.8V		3.3V	
		I/O	Conditions	I/O	Conditions
LPC	LPCCLK, LAD[3:0], LFRAME#	1.8V Input 1.8V Output	VCC=1.8V	3.3V Input 3.3V Output	VCC=3.3V
FSPI SERIRQ	FSCK, FSCE#, FMOSI, FMISO, SERIRQ	1.8V Input 1.8V Output	VFSPI= 1.8V Refer to GCR29	3.3V Input 3.3V Output	VFSPI= 3.3V Refer to GCR29
SMB	SMCLK[5:0], SMDAT[5:0]	1.8V Open-drain Internal pull-up must be disabled	Refer to GCR19 - GCR28	3.3V Open-drain	Refer to GCR19 - GCR28
SMB	SMINT[11:0]	1.8V Input Only Internal pull-up must be disabled	Refer to GCR19 - GCR28	3.3V Input	Refer to GCR19 - GCR28
GPIO	Refer to Table 7-8. GPIO Alternate Function on page 254.	1.8V Input Only Internal pull-up must be disabled	Refer to GCR19 - GCR28, GCR30, GCR33	3.3V Input 3.3V Output	Refer to GCR19 - GCR28, GCR30, GCR33

5.9 Power Consumption Consideration

- Each input pin should be driven or pulled

Input floating causes leakage current and should be prevented.
Pins can be pulled by an external pull resistor or internal pull for a pin with programmable pull.

- Each output-drain output pin should be pulled

If an output-drain output pin is not used and pulled by an external pull resistor or internal pull for a pin with programmable pull, make it drive low by the firmware.

- Each input pin which belongs to VSTBY power plane is connected or pulled up to VCC power plane

Such cases may cause leakage current when VCC is not supplied and a diode may be used to isolate leakage current from VSTBY to VCC. For example, use diodes for KBRST# and GA20 if they are connected to VCC logic of South-Bridge.

- Any pin which belongs to VSTBY power plane should not be pulled to VCC in most cases.

It may cause a leakage current path when VCC is shut down. Refer to the above consideration.

- Program GPIO ports as output mode as soon as possible

Any GPIO port used in output mode should be programmed as soon as possible since this pin may not be driven (be floating) if its default value of pull is off.

- Disable unnecessary pull in power saving mode

Prevent from driving a pin low or letting a pin be driven low but its pull high function is enabled in power saving mode.
Prevent from driving a pin high or letting a pin be driven high but its pull low function is enabled in power saving mode.

- Handle the connector if no cable is plugged into it

The firmware or the hardware should prevent the wire connected to the connector from no driving if no cable is plugged into the connector.

- Disable unnecessary pull for a programmable pull pin

Pull control may be enabled for an input pin or an open-drain output pin and should be disabled for a push-pull output pin.
Pull control should be disabled if an external pull resistor exists.
External pull resistor can control the pull current precisely since the register value of the internal pull has large tolerance. Refer to section 9 DC Characteristics on page 567 for the detail.

- Flash standby mode

Make flash enter standby mode to reduce power consumption if it is not used.
It's controlled by AFSTBY bit in FPCFG register.

- Prevent accessing Scratch RAM before entering power-saving mode

There is unnecessary power consumption after Scratch RAM is accessed in data space. Read any other registers of external data memory once to prevent this condition.

- Use Doze mode

Doze mode has huge power consumption reduction due to the CPU clock is gated (stopped) in this mode.

- Use Sleep mode rather than Doze mode

Sleep mode has less power consumption than Doze mode because PLL is power-down and EC clock is stopped in Sleep mode although most EC modules are not available.
Refer to Table 5-38 on page 31 for the detail.

- Gate clock by module in EC domain

All modules in EC domain are not clock gated in default but can be gated by module to get less power consumption.
It's controlled by CGCTRL1R and CGCTRL2R registers.

- Power-down ADC analog circuit if it is unnecessary.

ADC analog circuits are power-down in default and should be activated only if necessary.
ADC analog circuit power-down is controlled by ADCEN bit in ADCCFG register.

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6. Host Domain Functions

6.1 The Enhanced Serial Peripheral Interface (eSPI)

6.1.1 Overview

The Enhanced Serial Peripheral Interface (eSPI) is basically a LPC replacement, and it has more benefits such as low voltage level, low power, higher bandwidth, pin-count saving, etc.

The MAFS (Master Attached Flash Sharing) lets the EC runtime code-fetch from the chipset.

Additionally, SAFS (Slave Attached Flash Sharing) is supported. This implies that the physical flash component is attached to the EC, and the eSPI master can access this flash over the eSPI bus by PUT_FLASH_NP and GET_FLASH_C commands.

6.1.2 Features

- Compatible with eSPI specification v1.0
- Supports Peripheral Channel
- Supports OOB Message Channel
- Supports Virtual Wires Channel
- Supports Flash Access Channel, MAFS/SAFS both supported
- Supports eSPI 20MHz to 66MHz

6.1.3 Function Description

To support eSPI, FreqFND is required to be higher than half of the eSPI clock frequency.
To read the flash attached to the eSPI master, it can be done by the EC-Indirect Memory cycle or eSPI upstream cycle.
To erase/program the flash attached to the eSPI master, it can be done by the eSPI upstream cycle.

6.1.3.1 Peripheral Channel

EC supports legacy LPC transactions over the Peripheral Channel. Short I/O transactions (PUT_IORD_SHORT and PUT_IOWR_SHORT) are used to access PNPCFG and Logical Devices. The length of short I/O transactions is 1, 2 or 4 bytes, and it is recommended to use the short I/O commands with 1-byte data only. Short Memory transactions (PUT_MEMRD32_SHORT and PUT_MEMWR32_SHORT) or transactions with memory access cycle types (Memory Read 32 and Memory Write 32) are used to access the flash content through SMFI module. Host-Indirect memory cycles based on short I/O transactions can access the flash as well.

- Supports HLPC
- Supports H2RAM
- Supports I2EC
- Supports Host-Indirect memory cycles
- Supports port 80h read via parallel port with the software provided by ITE

The PUT_PC, PUT_NP, GET_PC, PUT_IORD_SHORT, PUT_IOWR_SHORT, PUT_MEMRD32_SHORT and PUT_MEMWR32_SHORT commands are supported.

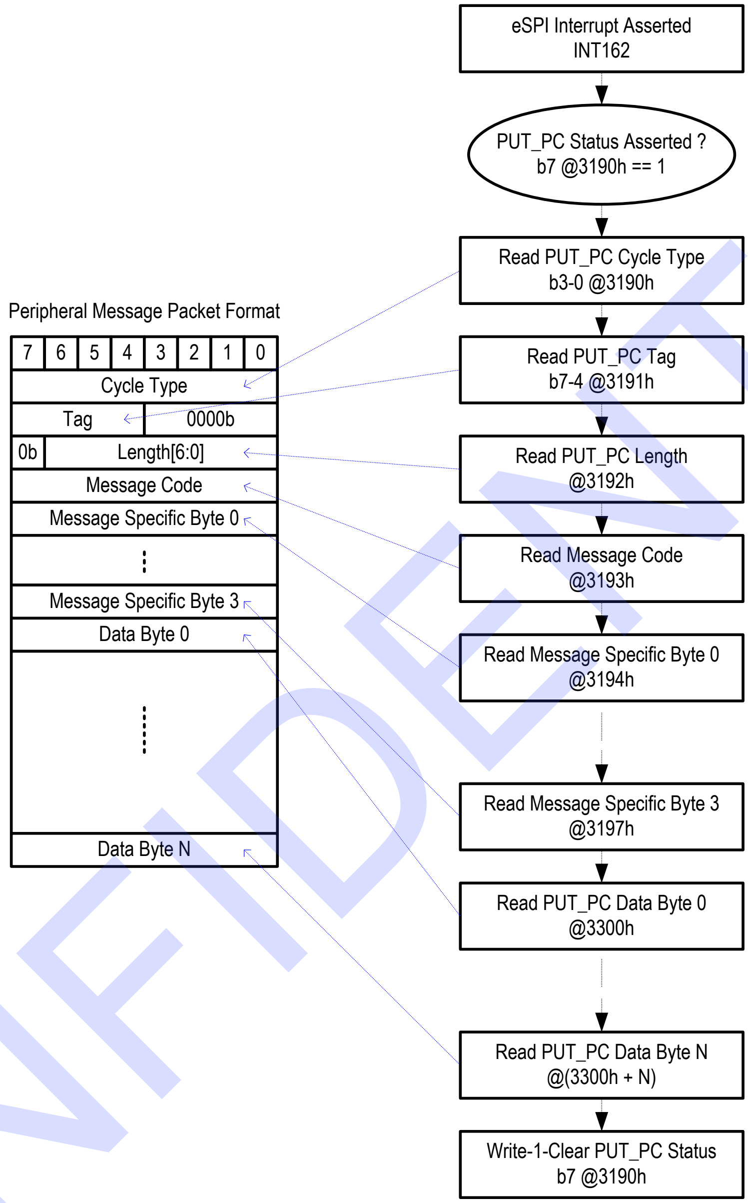
The GET_NP command is reserved and upstream memory access transactions are not supported.

- **Receive A Message through eSPI Peripheral Channel**

After receiving a message transaction initiated by the eSPI master, EC clears its eSPI PC_FREE status (refer to eSPI specification) to 0, which indicates EC is not free to accept another peripheral posted or completion

transaction. The software needs to follow the sequence listed below to release the PC_FREE status.

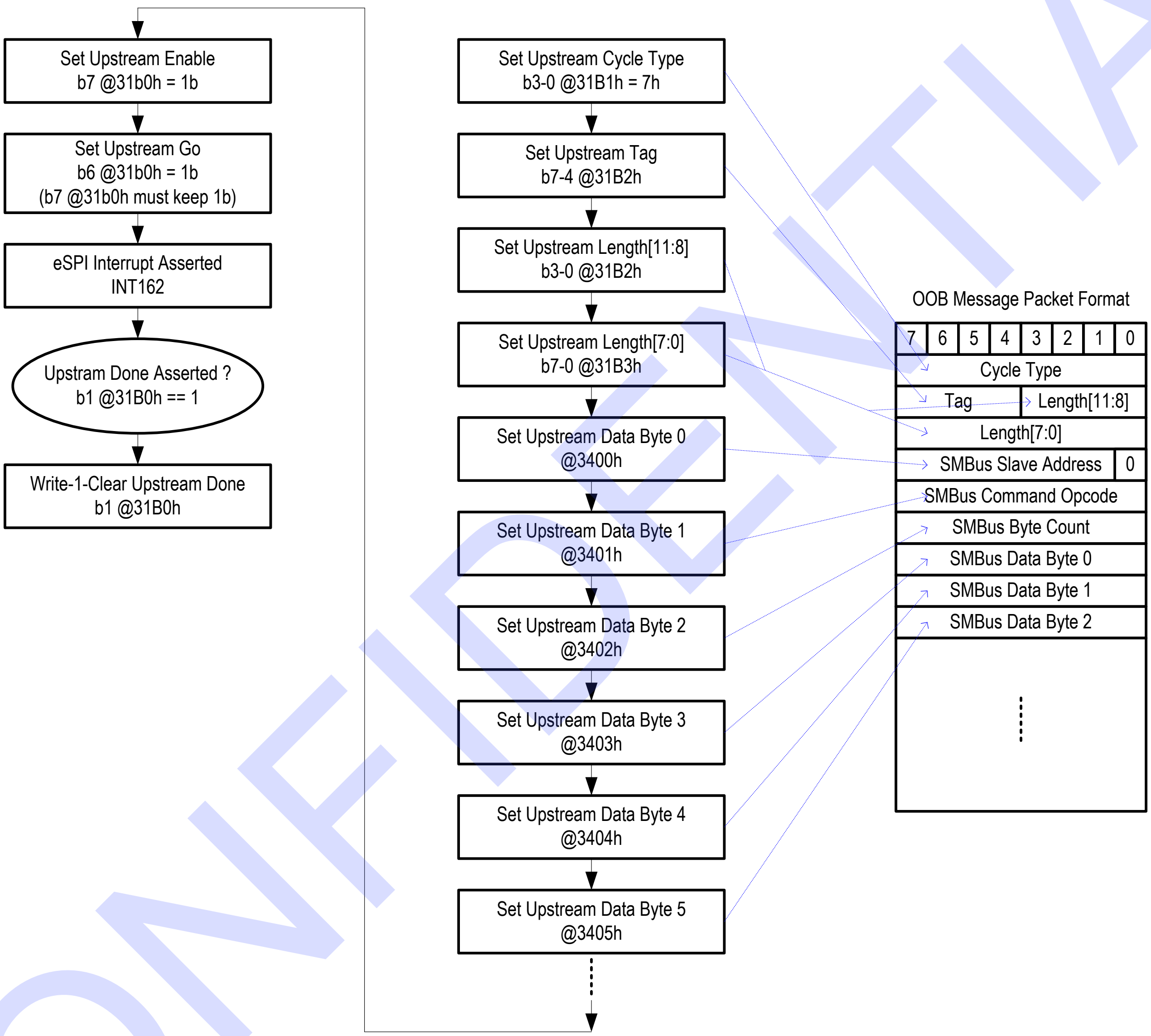
Figure 6-1. Flow of Receiving a Peripheral Message Transcation over eSPI Bus



- **Initiate A Message through eSPI Peripheral Channel**

EC also can initiate a peripheral message transaction over the eSPI bus. The software sequence is listed below.

Figure 6-2. Flow of Initiating a Peripheral Message Transcation over eSPI Bus



6.1.3.2 Flash Access Channel (MAFS)

The flash access channel provides a path allowing the flash components to be shared run-time between chipset and EC. For the master attached to the flash sharing, refers to the scheme where flash components are attached to the eSPI master such as the chipset. EC is allowed to access the shared flash component through the flash access channel.

If MAFS configuration is enabled for a platform, only GET_FLASH_NP and PUT_FLASH_C flash commands, which are required for Master-Attached Flash access, are supported. Under this configuration, the PUT_FLASH_NP and GET_FLASH_C commands are not supported.

- **Code-fetch Switched from Flash to eSPI Flash Sharing**
  - EC power-on (default FreqPLL=48MHz, FreqFND=16MHz)
  - Copy flash data to Scratch SRAM
  - The program counter jumps to Scratch ROM
  - Switch PLL=96MHz, FreqFND=32MHz
  - Let RSMRST# low-to-high
  - Endless loop to wait for FCEAF@ESGCTRL0 = 1 and Write 1b Clear.
  - Write 1b to FTHS@FLHCTRL5R to make code-fetch from eSPI flash sharing later
  - Endless loop to wait for FTHS@FLHCTRL5R = 1
  - VW SLAVE_BOOT_LOAD_DONE = 1
  - Leave Scratch ROM
  - Fetch through eSPI flash sharing
- **Code-fetch Switched from eSPI Flash Sharing to Flash**
  - Copy flash data to Scratch SRAM
  - The program counter jumps to Scratch ROM
  - Write 0b to FTHS@FLHCTRL5R to make code-fetch from SPI flash later
  - Endless loop to wait for FTHS@FLHCTRL5R = 0
  - Write 0b to FFSPITRI@FLHCTRL3R to re-drive FSPI I/F
  - Switch PLL=48MHz, FreqFND=16MHz
  - Let RSMRST# high-to-low
  - Leave Scratch ROM
  - Fetch from SPI flash

- **Initiate a Non-Posted Transaction through eSPI Flash Access Channel**

EC also can access the shared flash component through EC bus.

- Maximum read request size: 64 bytes
- Maximum payload size: 64 bytes
- Tag field in Flash Access Request Packet Format must be set 1h
- Flash Read, Flash Write and Flash Erase supported

The software sequence of initiating a Flash Read transaction is listed below.

Figure 6-3. Flow of Initiating a Flash Read Transcation over eSPI Bus

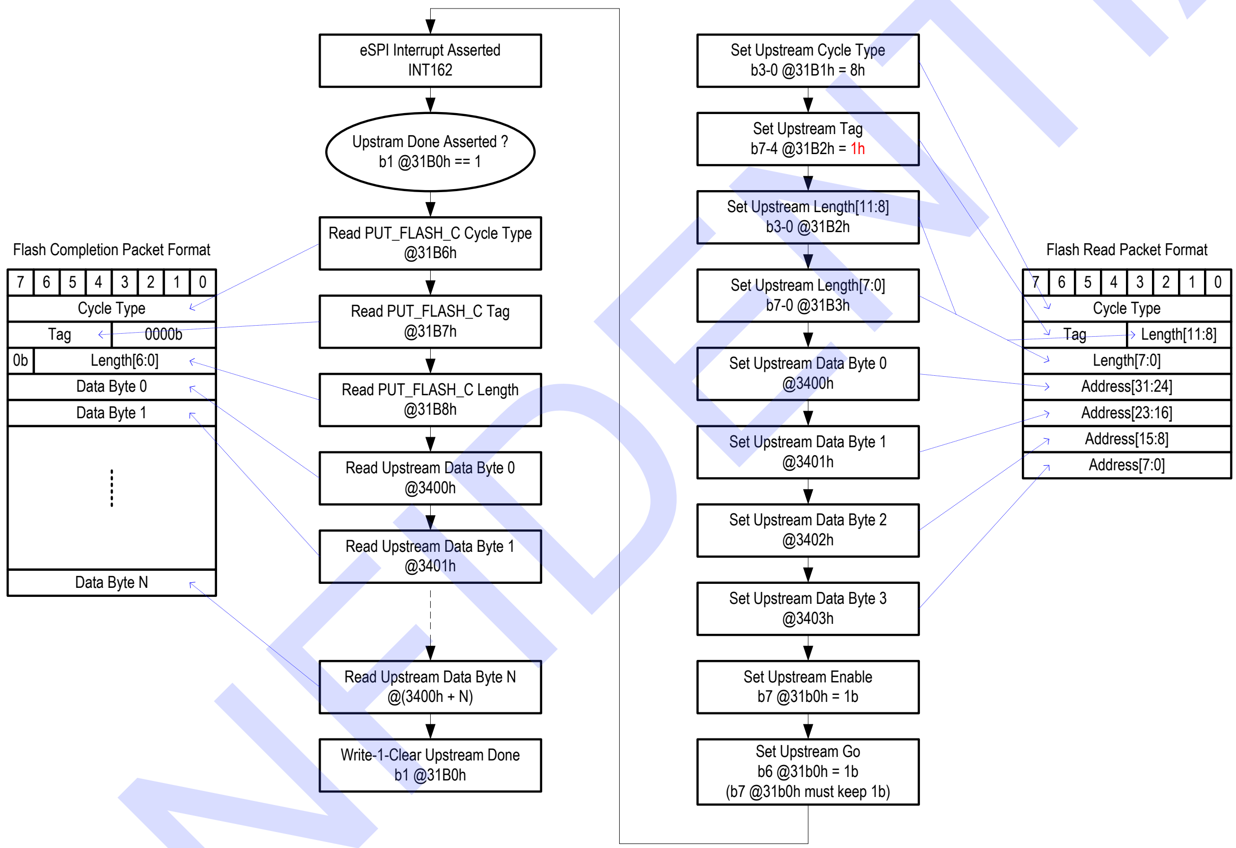
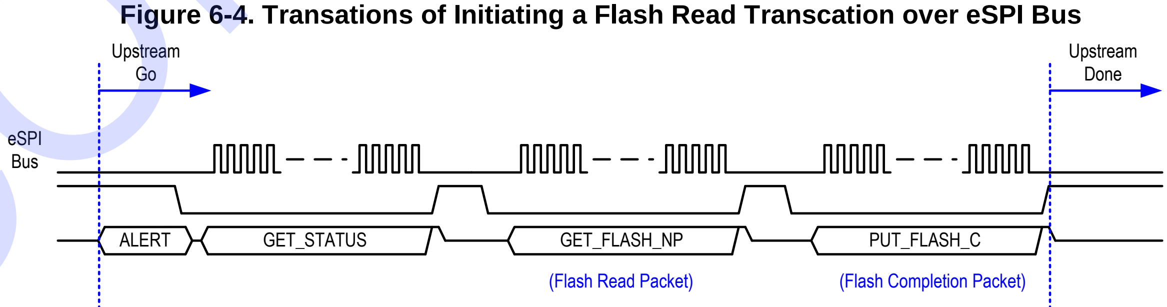
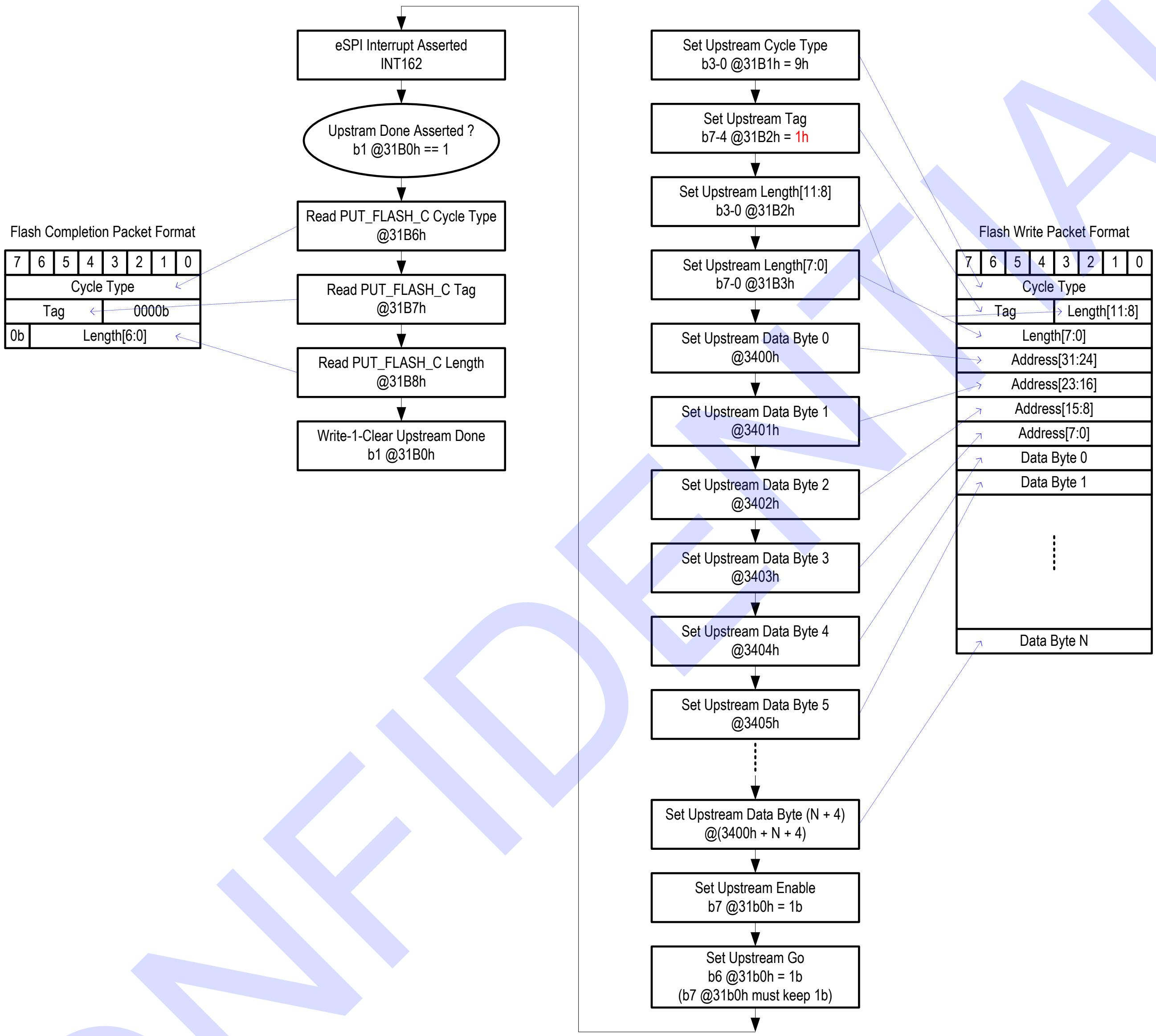


Figure 6-4. Transations of Initiating a Flash Read Transcation over eSPI Bus



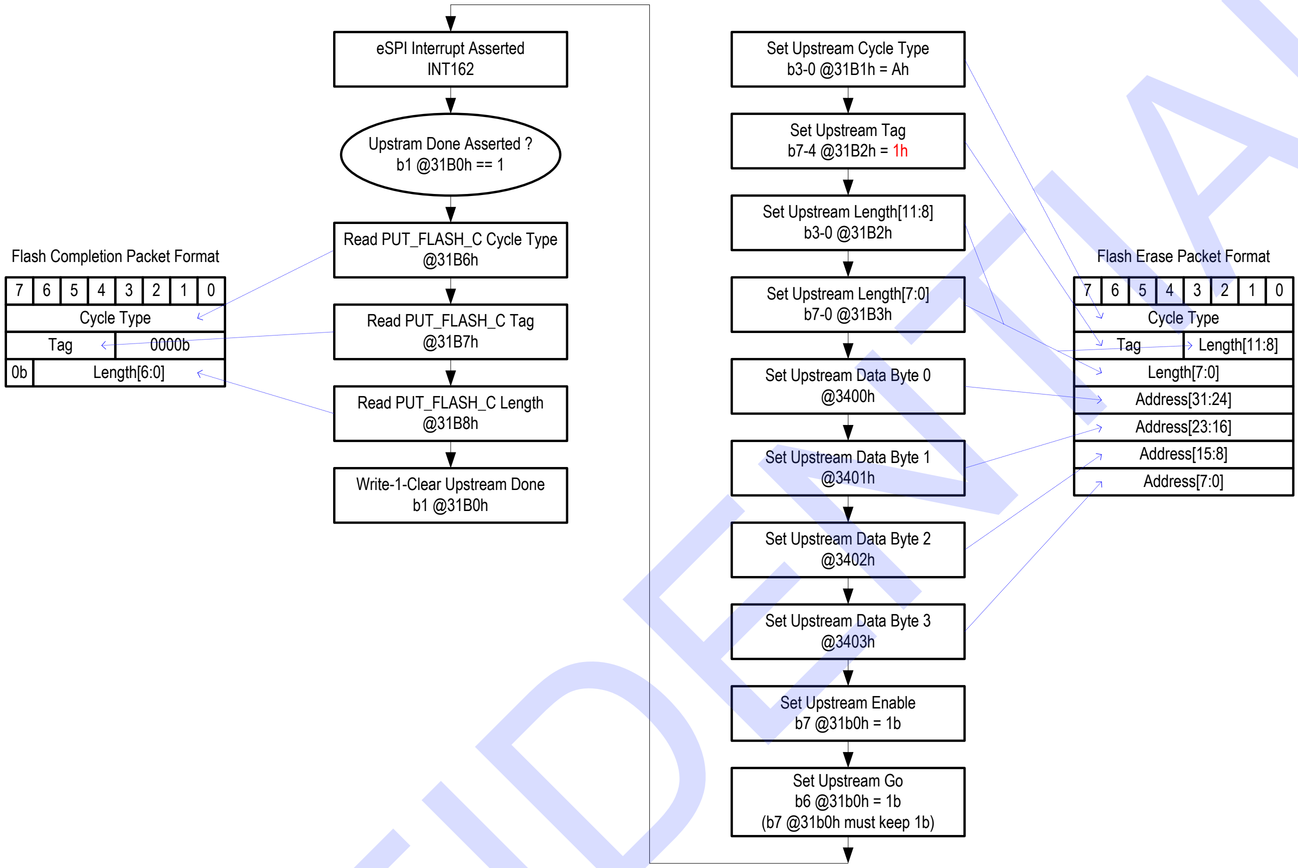
The software sequence of initiating a Flash Write transaction is listed below.

Figure 6-5. Flow of Initiating a Flash Write Transcation over eSPI Bus



The software sequence of initiating a Flash Erase transaction is listed below.

Figure 6-6. Flow of Initiating a Flash Erase Transcation over eSPI Bus



EC uses tag 0 to label the flash access request is initiated for code-fetch and tag 1 for other applications. Different tags allow non-posted requests to be outstanding at any time and there are no requirements for order between each other.

6.1.3.3 Flash Access Channel (SAFS)

If SAFS configuration is enabled for a platform, only PUT_FLASH_NP and GET_FLASH_C flash commands are supported. The eSPI master can access the flash attached to EC over the eSPI bus by PUT_FLASH_NP and GET_FLASH_C flash commands.

- **Receive a Flash Read through eSPI Flash Channel**

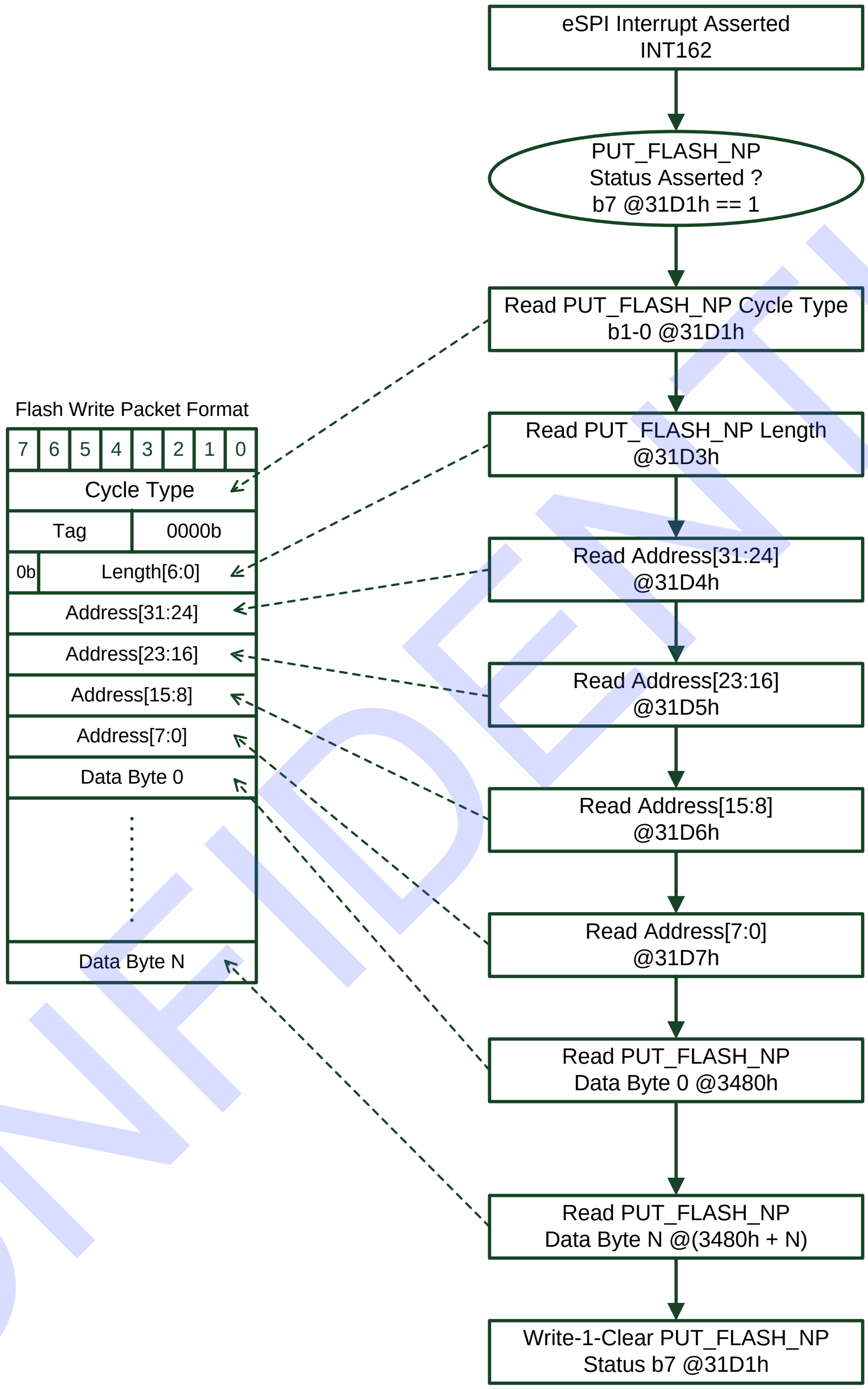
EC issues read cycles with the specified address to the flash, and returns the content of the flash to the eSPI master automatically.

- **Receive a Flash Write through eSPI Flash Channel**

EC issues program sequences with the specified address to the flash, and returns “Successful Completion” to the eSPI master automatically.

For some purpose, it also allows for processing the flash write with software’s intervention. The software sequence is listed below.

Figure 6-7. Flow of Receiving a Flash Write Transcation over eSPI Bus



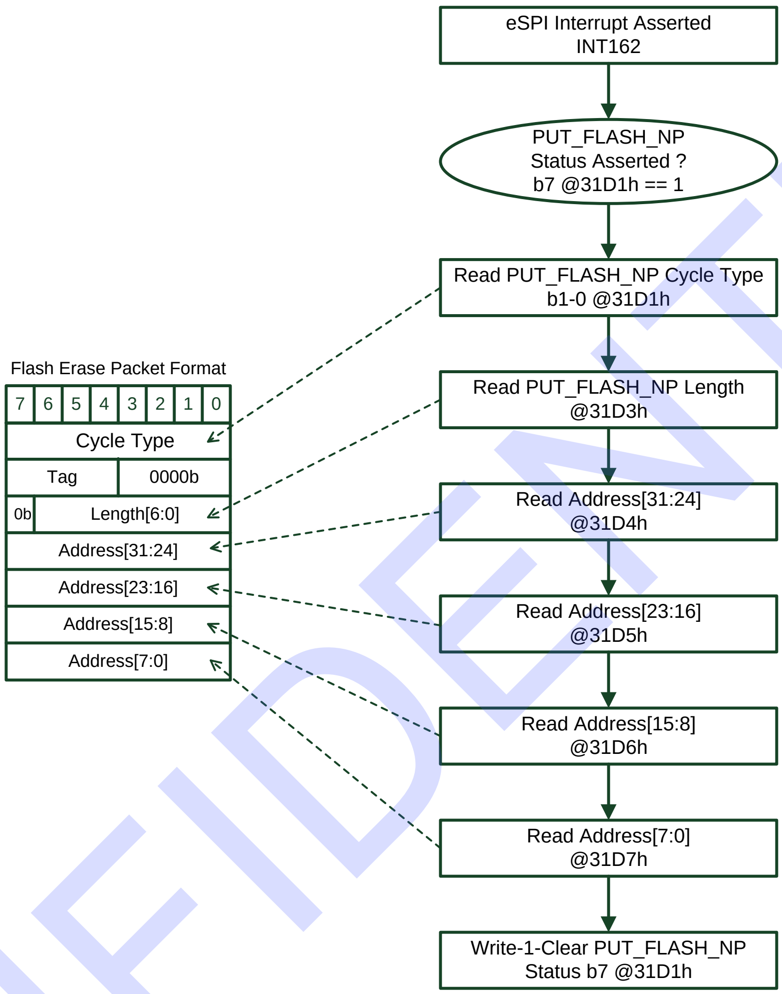
- **Receive A Flash Erase through eSPI Flash Channel**

EC issues erase sequences with the specified address to the flash, and returns “Successful Completion” to the eSPI master automatically. The software sequence is listed below.

For some purpose, it also allows for processing the flash erase with software’s intervention. The software

sequence is listed below.

Figure 6-8. Flow of Receiving a Flash Erase Transcation over eSPI Bus



6.1.3.4 OOB Message Channel

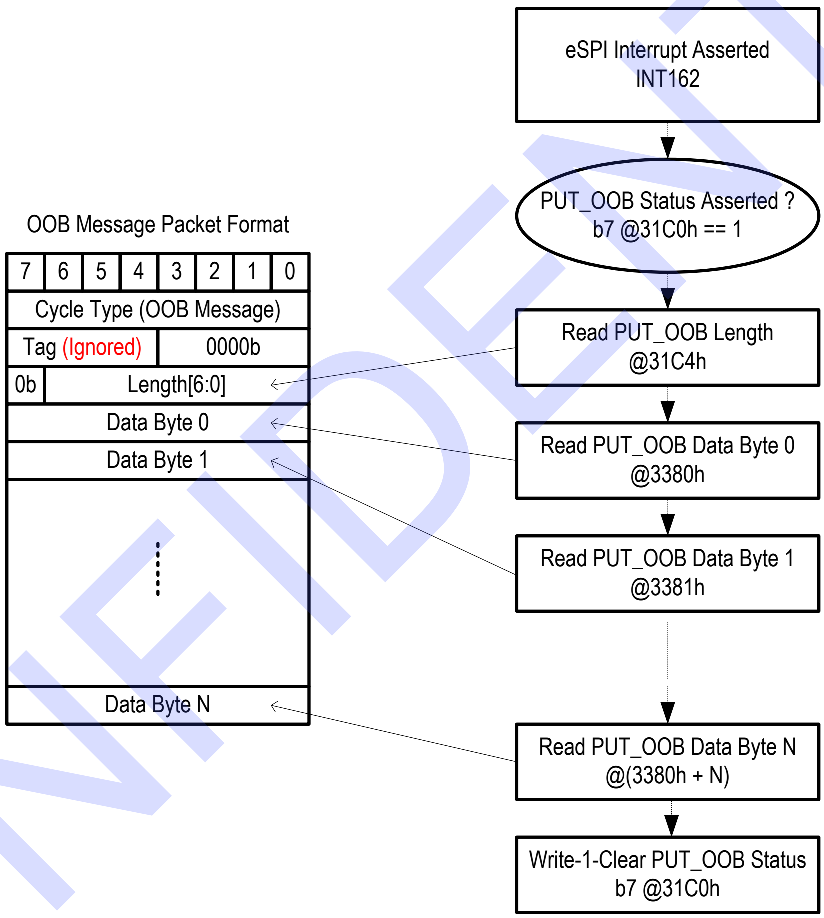
The OOB channel is used to handle transactions between the OOB processor and EC. EC is able to initiate an upstream OOB message transaction for reading of SKL-PCH HW information, including temperature and RTC time/date, using messages with predefined slave address and command codes.

The GET_OOB and PUT_OOB commands are supported.

- **Receive A Posted Transaction through eSPI OOB Message Channel**

EC is able to receive a posted OOB message transaction over the eSPI bus. The software sequence is listed below.

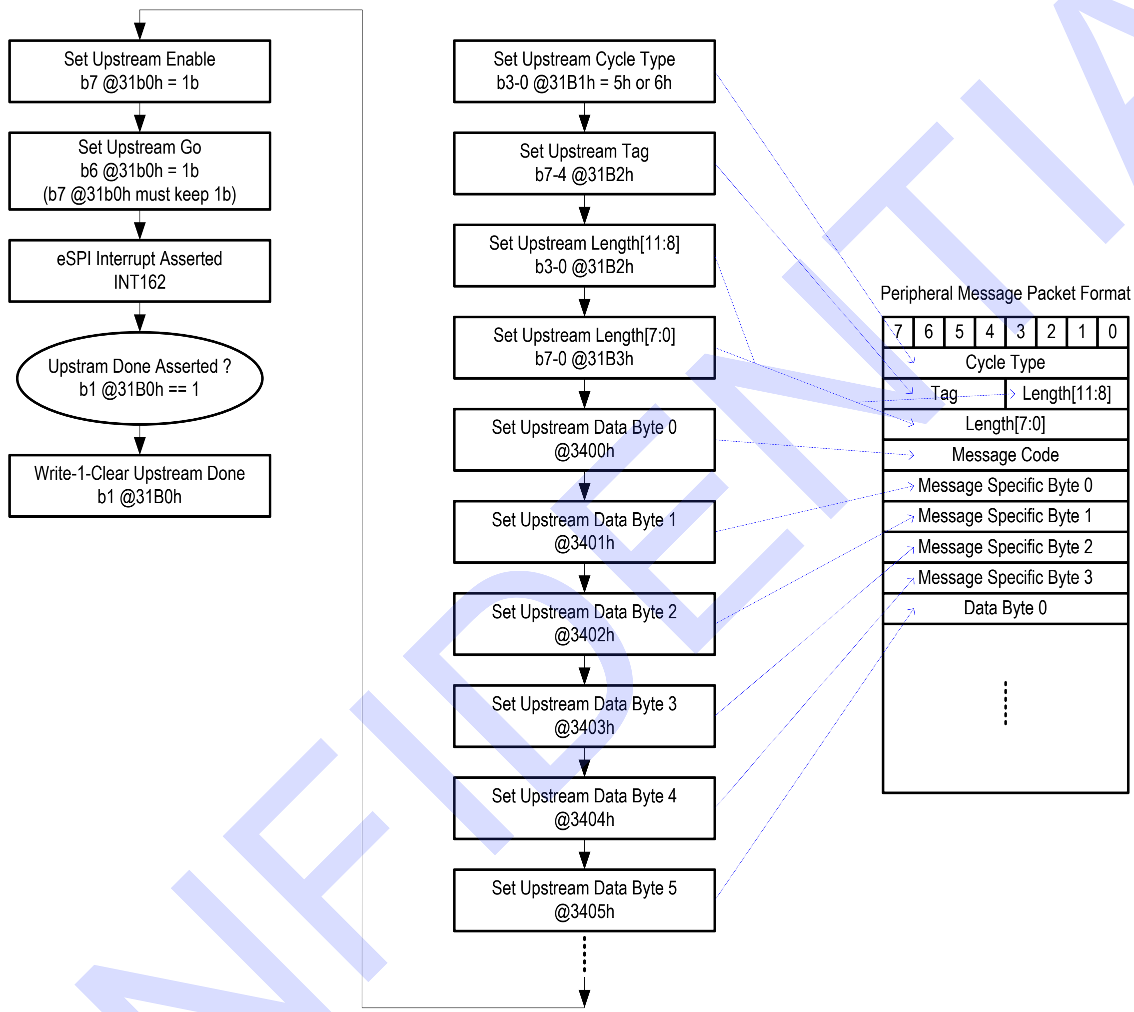
Figure 6-9. Flow of Receiving a OOB Message Transcation over eSPI Bus



- **Initiate A Posted Transaction through eSPI OOB Message Channel**

EC is able to initiate a posted OOB message transaction over the eSPI bus. The software sequence is listed below.

Figure 6-10. Flow of Initiating a OOB Message Transcation over eSPI Bus



6.1.3.5 Virtual Wires Channel

The Virtual Wires channel is used to communicate the state of sideband pins tunneled through eSPI as in-band messages. Serial IRQ interrupts are also communicated through this channel as in-band messages.
.

- Maximum virtual wire count supported: 7
- Supports interrupt event: IRQ0 – IRQ15
- Supports system event

- **Receive An In-band Message through eSPI Virtual Wires Channel**

EC is able to receive an in-band message through the eSPI Virtual Wires channel. The software sequence of handling an updated VW Index 2 event is listed below.

- eSPI VW Interrupt asserted (INT163)
- VWIDX2 Updated Flag asserted? (b0 @3291h)
- Read VW Index 2 @3202h to get the state of VW Index 2
- Write-1-clear VWIDX2 Updated Flag (b0 @3291h)
- Read VW Index2 @3202h again to prevent event losing during "Write-1-clear VWIDX2 Updated Flag"

- **Initiate an In-band Message through eSPI Virtual Wires Channel**

EC is able to initiate an in-band message through eSPI Virtual Wires channel. The software sequence of initiating an in-band message for VW Index 4 is listed below.

Method 1: Write VW Index 4 @3204h to change the state of VW Index 4

If the state of VW Index 4 is different from that sent during the previous transaction, EC initiates an in-band message over the eSPI bus for updating VW Index 4. If not, EC does not initiate an in-band message.

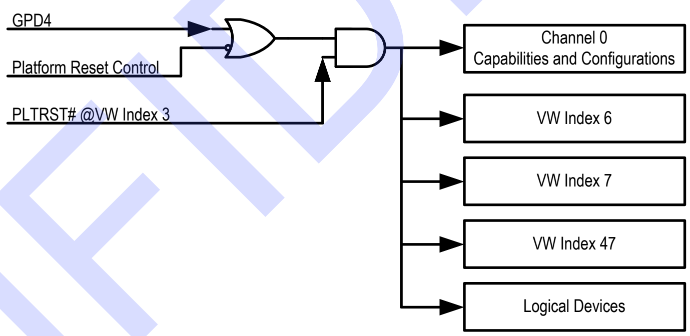
Method 2: Write 1 to VW Index 4 Resend @3293h

Writing 1 to VW Index 4 Resend forces EC to resend the state of VW Index 4 regardless of that sent during the previous transaction. VW Index 4 Resend is automatically cleared after the in-band message is sent through the eSPI Virtual Wires channel.

- **Platform Reset**

Platform Reset event is communicated through the PLTRST# virtual wire. It also can be asserted from GPD4 if Platform Reset Control is set. The Platform Reset event is used in resetting the circuits listed below.

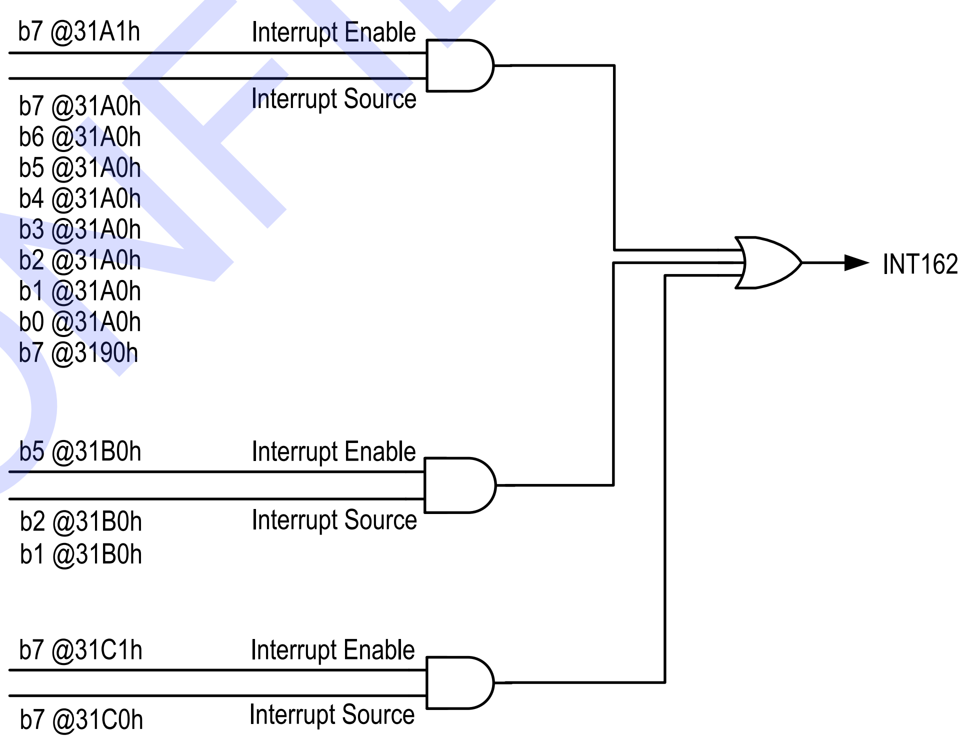
Figure 6-11. Scheme of Platform Reset



6.1.3.6 Expression of eSPI Interrupt Events

eSPI Interrupt Events	Interrupt Register	Description
eSPI Interrupt	b7@3190h & b7@31A1h	PUT_PC Status
	b7@31A0h & b7@31A1h	Flash Access Channel Enable Deasserted Flag
	b6@31A0h & b7@31A1h	OOB Message Channel Enable Deasserted Flag
	b5@31A0h & b7@31A1h	VW Channel Enable Deasserted Flag
	b4@31A0h & b7@31A1h	Peripheral Channel Enable Deasserted Flag
	b3@31A0h & b7@31A1h	Flash Access Channel Enable Asserted Flag
	b2@31A0h & b7@31A1h	OOB Message Channel Enable Asserted Flag
	b1@31A0h & b7@31A1h	VW Channel Enable Asserted Flag
	b0@31A0h & b7@31A1h	Peripheral Channel Enable Asserted Flag
	b2@31B0h & b5@31B0h	Upstream Channel Disable
	b1@31B0h & b5@31B0h	Upstream Done
	b7@31C0h & b7@31C1h	PUT_OOB Status
eSPI VW Interrupt	b7@3291h & b7@3290h	VWIDX47 Updated Flag
	b6@3291h & b7@3290h	VWIDX44 Updated Flag
	b5@3291h & b7@3290h	VWIDX43 Updated Flag
	b4@3291h & b7@3290h	VWIDX42 Updated Flag
	b3@3291h & b7@3290h	VWIDX41 Updated Flag
	b2@3291h & b7@3290h	VWIDX7 Updated Flag
	b1@3291h & b7@3290h	VWIDX3 Updated Flag
	b0@3291h & b7@3290h	VWIDX2 Updated Flag

Figure 6-12. eSPI Interrupt Events



6.1.4 EC Interface Registers, eSPI slave

The EC interface registers are listed below. The base address for eSPI slave is 3100h.
The address 00h-17h are DWord registers defined in eSPI specification and stored in Big Endian order.

Table 6-1. EC View Register Map, eSPI slave

7 … 0	Offset
Device Identification	00h-03h
General Capabilities and Configurations	04h-07h
Channel 0 Capabilities and Configurations	08h-0Bh
Channel 1 Capabilities and Configurations	0Ch-0Fh
Channel 2 Capabilities and Configurations	10h-13h
Channel 3 Capabilities and Configurations	14h-17h
Channel 3 Capabilities and Configurations 2	18h-1Bh
eSPI PC Control 0 (ESPCTRL0)	90h
eSPI PC Control 1 (ESPCTRL1)	91h
eSPI PC Control 2 (ESPCTRL2)	92h
eSPI PC Control 3 (ESPCTRL3)	93h
eSPI PC Control 4 (ESPCTRL4)	94h
eSPI PC Control 5 (ESPCTRL5)	95h
eSPI PC Control 6 (ESPCTRL6)	96h
eSPI PC Control 7 (ESPCTRL7)	97h
eSPI General Control 0 (ESGCTRL0)	A0h
eSPI General Control 1 (ESGCTRL1)	A1h
eSPI General Control 2 (ESGCTRL2)	A2h
eSPI General Control 3 (ESGCTRL3)	A3h
eSPI Upstream Control 0 (ESUCTRL0)	B0h
eSPI Upstream Control 1 (ESUCTRL1)	B1h
eSPI Upstream Control 2 (ESUCTRL2)	B2h
eSPI Upstream Control 3 (ESUCTRL3)	B3h
eSPI Upstream Control 6 (ESUCTRL6)	B6h
eSPI Upstream Control 7 (ESUCTRL7)	B7h
eSPI Upstream Control 8 (ESUCTRL8)	B8h
eSPI OOB Control 0 (ESOCTRL0)	C0h
eSPI OOB Control 1 (ESOCTRL1)	C1h
eSPI OOB Control 4 (ESOCTRL4)	C4h
eSPI SAFS Control 0 (ESPISAFSC0)	D0h
eSPI SAFS Control 1 (ESPISAFSC1)	D1h
eSPI SAFS Control 2 (ESPISAFSC2)	D2h
eSPI SAFS Control 3 (ESPISAFSC3)	D3h
eSPI SAFS Control 4 (ESPISAFSC4)	D4h
eSPI SAFS Control 5 (ESPISAFSC5)	D5h
eSPI SAFS Control 6 (ESPISAFSC6)	D6h
eSPI SAFS Control 7 (ESPISAFSC7)	D7h

6.1.4.1 Device Identification

Address Offset: 00h-02h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R	-	**Version ID** Read returns 01h.

6.1.4.2 General Capabilities and Configurations

Address Offset: 04h

Bit	R/W	Default	Description
7	R	0b	**CRC Checking Enable** This bit is set to '1' by the eSPI master to enable the CRC's checking on the eSPI bus. 0b: CRC checking is disabled. 1b: CRC checking is enabled.
6	R	0b	**Response Modifier Enable** This bit is set to '1' to enable the use of Response Modifier by eSPI slave to append either a peripheral (channel 0) completion, a virtual wire (channel 1) packet or a flash access (channel 3) completion to the GET_STATUS response phase. When this bit is a '0', the eSPI slave must only use the Response Modifier of "00", i.e. no append.
5	-	-	**Reserved**
4	R	0b	**Alert Mode** This bit serves to configure the Alert mechanism used by the slave to initiate a transaction on the eSPI interface. 0b: EIO1 (I/O[1]) pin is used to signal the Alert event. 1b: A dedicated ALERT# pin is used to signal the Alert event. **Note:** This bit can only be '0' in a single master-single slave topology. For single master-multiple slave topology, this bit must be programmed to '1'.
3-2	R	0b	**I/O Mode Select** The eSPI master programs this field to enable the appropriate mode of operation, which will take effect at the deassertion edge of the Chip Select#. The I/O mode configured in this field must be supported by both the master and slave. 00b: Single I/O 01b: Dual I/O 10b: Quad I/O 11b: Reserved
1-0	R	11b	**I/O Mode Support** Read returns 11b. 00b: Single I/O 01b: Single and Dual I/O 10b: Single and Quad I/O 11b: Single, Dual and Quad I/O

Address Offset: 05h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	000b	**Operating Frequency** This field identifies the frequency of operation. 000b: 20 MHz 001b: 25 MHz 010b: 33 MHz 011b: 50 MHz 100b: 66 MHz Otherwise: Reserved
3	-	0h	**Reserved**
2-0	R/W	010b	**Maximum Frequency Supported** This field identifies the maximum frequency of operation supported by the slave. 000b: 20 MHz 001b: 25 MHz 010b: 33 MHz 011b: 50 MHz 100b: 66 MHz Otherwise: Reserved The slave that indicates support for the maximum frequency of operation through this field will support all the lower frequencies on the list as well.

Address Offset: 06h

Bit	R/W	Default	Description
7-4	R	0h	**Maximum WAIT STATE Allowed** The eSPI master sets the maximum WAIT STATE allowed to be responded by the slave before it must respond with an ACCEPT, DEFER, NON-FATAL ERROR or FATAL ERROR response code. This is a 1-based field in the granularity of byte time. When “0”, it indicates a value of 16 byte time. A byte time corresponds to 8 serial clocks in the Single I/O mode, 4 serial clocks in the Dual I/O mode or 2 serial clocks in the Quad I/O mode.
3	-	0h	**Reserved**

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R	1111b	**Channel Supported** When any of the four bits is set, it indicates its corresponding channel is supported by the slave. Bit-0: Peripheral Channel Bit-1: Virtual Wire Channel Bit-2: OOB Message Channel Bit-3: Flash Access Channel Otherwise: Reserved for platform specific channels

6.1.4.3 Channel 0 Capabilities and Configurations

Address Offset: 08h-09h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 0Ah

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	001b	**Peripheral Channel Maximum Read Request Size** The eSPI master sets the maximum size of the read request for the Peripheral channel. The length must not cross the naturally aligned address boundary of the corresponding Maximum Read Request Size. 001b: 64 bytes address aligned max. read request size. Otherwise: Reserved
3	-	-	**Reserved**
2-0	R	001b	**Peripheral Channel Maximum Payload Size Selected** The eSPI master sets the maximum payload size for the Peripheral channel. The value set by the eSPI master must never be more than that advertised in the Max. Payload Size Supported field. The payload of the transaction must not cross the naturally aligned address boundary of the corresponding Maximum Payload Size. 001b: 64 bytes address aligned max. payload size. Otherwise: Reserved

Address Offset: 0Bh

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	000b	**Peripheral Channel Maximum Payload Size Supported** This field advertises the Maximum Payload Size supported by the slave. 001b: 64 bytes address aligned max. payload size. Otherwise: Reserved
3	-	-	**Reserved**
2	R	0b	**Bus Master Enable** Not supported.
1	R	0b	**Peripheral Channel Ready** When this bit is a '1', it indicates that the slave is ready to accept transactions on the Peripheral channel. The eSPI master should poll this bit after the channel is enabled before running any transaction on this channel to the slave. 0b: Channel is not ready. 1b: Channel is ready.
0	R	1b	**Peripheral Channel Enable** The channel is by default enabled after the ERST# (eSPI Reset#). This bit is cleared to '0' by the eSPI master to disable the Peripheral channel. Besides, clearing this bit from '1' to '0' triggers a reset to the Peripheral channel. The channel remains disabled until this bit is set to '1' again. Prior to disabling the Peripheral channel, the Bus Master Enable bit should be cleared to '0' to disable the bus mastering cycles.

6.1.4.4 Channel 1 Capabilities and Configurations

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 0Dh

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	R	0h	**Operating Maximum Virtual Wire Count** This is the maximum number of Virtual Wire groups that can be sent in a single Virtual Wire packet. This is a 0-based count. The default value of 0 indicates count of 1. The value configured in this field must never be more than that advertised in the Maximum Virtual Wire Count Supported field.

Address Offset: 0Eh

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	R	111b	**Maximum Virtual Wire Count Supported** This field advertises the Maximum Virtual Wire Count supported by the slave. If the slave supports different count values as initiators and as receivers of the Virtual Wires, this field indicates the lower of the two. The Virtual Wire Count specifies the maximum number of Virtual Wire groups being communicated in a single Virtual Wire packet. The eSPI slave must advertise a value of “000111b” or more in this field to indicate the support of at least 8 Virtual Wire groups being communicated in a single Virtual Wire packet. This is a 0-based count.

Address Offset: 0Fh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R	0b	**Virtual Wire Channel Ready** When this bit is a ‘1’, it indicates that the slave is ready to accept transactions on the Virtual Wire channel. The eSPI master should poll this bit after the channel is enabled before running any transaction on this channel to the slave. 0b: Channel is not ready. 1b: Channel is ready.
0	R	0b	**Virtual Wire Channel Enable** This bit is set to ‘1’ by the eSPI master to enable the Virtual Wire channel. Clearing this bit from ‘1’ to ‘0’ will not reset the Virtual Wire channel. The channel is by default disabled after the ERST# (eSPI Reset#).

6.1.4.5 Channel 2 Capabilities and Configurations

Address Offset: 10h-11h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 12h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**

Bit	R/W	Default	Description
2-0	R	001b	**OOB Message Channel Maximum Payload Size Selected** The eSPI master sets the maximum payload size for the OOB Message channel. The value set by the eSPI master must never be more than the value advertised in the Max. Payload Size Supported field. 001b: 69 bytes max. payload size. Otherwise: Reserved

Address Offset: 13h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	001b	**OOB Message Channel Maximum Payload Size Supported** This field advertises the Maximum Payload Size supported by the slave. 001b: 69 bytes max. payload size. Otherwise: Reserved
3-2	-	-	**Reserved**
1	R	0b	**OOB Message Channel Ready** When this bit is a '1', it indicates that the slave is ready to accept transactions on the OOB Message channel. The eSPI master should poll this bit after the channel is enabled before running any transaction on this channel to the slave. 0b: Channel is not ready. 1b: Channel is ready.
0	R	0b	**OOB Message Channel Enable** This bit is set to '1' by the eSPI master to enable the OOB Message channel. Clearing this bit from '1' to '0' triggers a reset to the OOB Message channel such as during error handling. The channel remains disabled until this bit is set to '1' again. The channel is by default disabled after the ERST# (eSPI Reset#).

6.1.4.6 Channel 3 Capabilities and Configurations

Address Offset: 14h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 15h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Flash Sharing Capability Supported** This field indicates the flash sharing capability supported by the slave. 00b: MAFS supported 01b: MAFS supported 10b: SAFS supported 11b: MAFS/SAFS supported

Address Offset: 16h

Bit	R/W	Default	Description
7	-	-	**Reserved**

Bit	R/W	Default	Description
6-4	R	001b	**Flash Access Channel Maximum Read Request Size** The eSPI master sets the maximum read request size for the Flash Access channel. The length of the read request must not cross the naturally aligned address boundary of the corresponding Maximum Read Request Size. 001b: 64 bytes max. payload size. Otherwise: Reserved
3	R	0b	**Flash Sharing Mode** When Flash Access channel is supported, this bit advertises the flash sharing scheme intended by the slave. 0b: Master attached flash sharing. 1b: Slave attached flash sharing. This bit is read-only and the readout value is always ‘0’ in the base specification as it is defined as the master attached flash sharing.
2-0	R	001b	**Flash Access Channel Maximum Payload Size Selected** The eSPI master sets the maximum payload size for the Flash Access channel. The value set by the eSPI master must never be more than that advertised in the Max. Payload Size Supported field. 001b: 64 bytes max. payload size. Otherwise: Reserved

Address Offset: 17h

Bit	R/W	Default	Description
7-5	R	001b	**Flash Access Channel Maximum Payload Size Supported** This field advertises the Maximum Payload Size supported by the slave. 001b: 64 bytes max. payload size. Otherwise: Reserved
4-2	R	001b	**Flash Block Erase Size** The eSPI master sets this field to communicate the block erase size to the slave. This field is applicable only to the master attached flash sharing scheme. 000b: Reserved 001b: 4 Kbytes 010b: 64 Kbytes 011b: Both 4 Kbytes and 64 Kbytes are supported 100b: 128 Kbytes 101b: 256 Kbytes 110b – 111b: Reserved
1	R	0b	**Flash Access Channel Ready** When this bit is a ‘1’, it indicates that the slave is ready to accept transactions on the Flash Access channel. eSPI master should poll this bit after the channel is enabled before running any transaction on this channel to the slave. 0b: Channel is not ready. 1b: Channel is ready.
0	R	0b	**Flash Access Channel Enable** This bit is set to ‘1’ by eSPI master to enable the Flash Access channel. Clearing this bit from ‘1’ to ‘0’ triggers a reset to the Flash Access channel such as during error handling. The channel remains disabled until this bit is set to ‘1’ again. The channel is by default disabled after the ERST# (eSPI Reset#).

6.1.4.7 Channel 3 Capabilities and Configurations 2

Address Offset: 18h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 19h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	R	00000b	**Target RPMC Supported** This field indicates the total number of Replay Protected Monotonic Counters (RPMC) supported by the slave. It is a 1-based field. 0h: The slave does not support RPMC. 1h: The slave supports up to 1 RPMC. 2h: The slave supports up to 2 RPMC. ... 3Fh: The slave supports up to 63 RPMC.

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R/W	00000100b	**Target Flash Erase Block Size for Master's Regions** This field indicates the sizes of the erase commands the master may issue. If multiple bits are set, it may issue an erase using any of the indicated sizes. If multiple regions are accessible by the master, this field advertises the common erase block sizes for these regions. This field is only applicable when slave attached flash sharing scheme is selected. Bit 0: 1 Kbytes EBS supported Bit 1: 2 Kbytes EBS supported Bit 2: 4 Kbytes EBS supported Bit 3: 8 Kbytes EBS supported Bit 4: 16 Kbytes EBS supported Bit 5: 32 Kbytes EBS supported Bit 6: 64 Kbytes EBS supported Bit 7: 128 Kbytes EBS supported

Address Offset: 1Bh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R	001b	**Target Maximum Read Request Size Supported** This field indicates the maximum read request size supported by the slave as the Target on the Flash Access channel. This field is only applicable when slave attached flash sharing scheme is selected. 000b, 001b: 64 bytes max. read request size 010b: 128 bytes max. read request size 011b: 256 bytes max. read request size 100b: 512 bytes max. read request size 101b: 1024 bytes max. read request size 110b: 2048 bytes max. read request size 111b: 4096 bytes max. read request size

6.1.4.8 eSPI PC Control 0 (ESPCTRL0)

Address Offset: 90h

Bit	R/W	Default	Description
7	R/WC	0b	**PUT_PC Status** It indicates that the eSPI slave has received a peripheral posted/completion. Write-1-clear to release PC_FREE.
6-4	-	-	**Reserved**
3-0	R	-	**PUT_PC Cycle Type** It stores the decoded cycle type in a received posted/completion cycle. 3h: Message 4h: Message with Data 5h: Successful Completion Without Data 6h: Successful Completion With Data / the first completion 7h: Successful Completion With Data / the middle completion 8h: Successful Completion With Data / the last completion 9h: Successful Completion With Data / the only completion Ah: Unsuccessful Completion Without Data / the last completion Bh: Unsuccessful Completion Without Data / the only completion Ch: Reserved Dh: Reserved Eh: Reserved Fh: Invalid Cycle Type

6.1.4.9 eSPI PC Control 1 (ESPCTRL1)

Address Offset: 91h

Bit	R/W	Default	Description
7-4	R	-	**PUT_PC Tag** It stores the Tag field in a received posted/completion cycle.
3-0	-	-	**Reserved**

6.1.4.10 eSPI PC Control 2 (ESPCTRL2)

Address Offset: 92h

Bit	R/W	Default	Description
1	-	-	**Reserved**
6-0	R	-	**PUT_PC Length** It stores the Length field in a received posted/completion cycle.

6.1.4.11 eSPI PC Control 3 (ESPCTRL3)

Address Offset: 93h

Bit	R/W	Default	Description
7-0	R	-	**Message Code** It stores the Message Code field in a message packet.

6.1.4.12 eSPI PC Control 4 (ESPCTRL4)

Address Offset: 94h

Bit	R/W	Default	Description
7-0	R	-	**Message Specific Byte 0** It stores the Message Specific Byte 0 field in a message packet.

6.1.4.13 eSPI PC Control 5 (ESPCTRL5)

Address Offset: 95h

Bit	R/W	Default	Description
7-0	R	-	**Message Specific Byte 1** It stores the Message Specific Byte 1 field in a message packet.

6.1.4.14 eSPI PC Control 6 (ESPCTRL6)

Address Offset: 96h

Bit	R/W	Default	Description
7-0	R	-	**Message Specific Byte 2** It stores the Message Specific Byte 2 field in a message packet.

6.1.4.15 eSPI PC Control 7 (ESPCTRL7)

Address Offset: 97h

Bit	R/W	Default	Description
7-0	R	-	**Message Specific Byte 3** It stores the Message Specific Byte 3 field in a message packet.

6.1.4.16 eSPI General Control 0 (ESGCTRL0)

Address Offset: A0h

Bit	R/W	Default	Description
7	R/WC	0b	**Flash Access Channel Enable Deasserted Flag** It indicates a 1-to-0 transition of 'Flash Access Channel Enable' bit after eSPI issues SET_CONFIGURATION.
6	R/WC	0b	**OOB Message Channel Enable Deasserted Flag** It indicates a 1-to-0 transition of 'OOB Message Channel Enable' bit after eSPI issues SET_CONFIGURATION.
5	R/WC	0b	**VW Channel Enable Deasserted Flag** It indicates a 1-to-0 transition of 'Virtual Wire Channel Enable' bit after eSPI issues SET_CONFIGURATION.
4	R/WC	0b	**Peripheral Channel Enable Deasserted Flag** It indicates a 1-to-0 transition of 'Peripheral Channel Enable' bit after eSPI issues SET_CONFIGURATION.
3	R/WC	0b	**Flash Channel Enable Asserted Flag** It indicates a 0-to-1 transition of 'Flash Access Channel Enable' bit after eSPI issues SET_CONFIGURATION.
2	R/WC	0b	**OOB Message Channel Enable Asserted Flag** It indicates a 0-to-1 transition of 'OOB Message Channel Enable' bit after eSPI issues SET_CONFIGURATION.
1	R/WC	0b	**VW Channel Enable Asserted Flag** It indicates a 0-to-1 transition of 'Virtual Wire Channel Enable' bit after eSPI issues SET_CONFIGURATION.
0	R/WC	0b	**Peripheral Channel Enable Asserted Flag** It indicates a 0-to-1 transition of 'Peripheral Channel Enable' bit after eSPI issues SET_CONFIGURATION.

6.1.4.17 eSPI General Control 1 (ESGCTRL1)

Address Offset: A1h

Bit	R/W	Default	Description
7	R/W	0b	**eSPI Interrupt Enable**
6	-	-	**Reserved**
5	R/W	0b	**Ignore eSPI Unsupported Memory Read Address (IESPIUMRA)** 0b: Return "Unsuccessful Completion" for unsupported memory addresses (only for read cycle). 1b: Return "Successful Completion" for all memory addresses (only for read cycle).
4	R/W	0b	**Ignore eSPI Unsupported IO Address (IESPIUIOA)** 0b: Return "Unsuccessful Completion" for unsupported IO addresses. 1b: Return "Successful Completion" for all IO addresses.
3-0	-	-	**Reserved**

6.1.4.18 eSPI General Control 2 (ESGCTRL2)

Address Offset: A2h

Bit	R/W	Default	Description
7	R/W	0b	**eSPI Queue Clock Switch Enable (ESPIQCSE)** 0b: eSPI Tx/Rx queues are clocked by the PLL clock and do not work during the sleep mode. 1b: Switch the clock of eSPI Tx/Rx queues to ESCK while entering the sleep mode, which lets eSPI Tx/Rx queues work without the PLL clock.
6	R/W	0b	**eSPI Input Pad Gating (ESPIIPG)** 0b: eSPI Pad is not gated. 1b: eSPI Pad is gated.
5	-	-	**Reserved**
4	R/W	0b	**eSPI To WUC Enable** 0b: Disable 1b: If an eSPI transaction is accepted, WU42 interrupt will be asserted.
3-0	-	-	**Reserved**

6.1.4.19 eSPI General Control 3 (ESGCTRL3)

Address Offset: A3h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Suspend eSPI Peripheral Channel (SESPIPC)** 0b: Return peripheral channel ready for the GET_CONFIGURATION cycle. 1b: Return peripheral channel non-ready for the GET_CONFIGURATION cycle.

6.1.4.20 eSPI Upstream Control 0 (ESUCTRL0)

Address Offset: B0h

Bit	R/W	Default	Description
7	R/W	0b	**Upstream Enable** 0b: Disable 1b: Initiating eSPI upstream transactions is allowed.
6	R/W	-	**Upstream Go** Write-1 to initiate an eSPI upstream transaction if not ‘Upstream Busy’. Write-0 is ignored.
5	R/W	0b	**Upstream Interrupt Enable** 0b: Disable 1b: Enable
4-3	-	-	**Reserved**
2	R/WC	0b	**Upstream Channel Disable** A flag to indicate the corresponding channel of the eSPI upstream transaction is disabled. Wrtie-1 to clear this bit.
1	R/WC	0b	**Upstream Done** A flag to indicate the eSPI upstream transaction is done. Wrtie-1 to clear this bit.
0	R	0b	**Upstream Busy** The upstream is in progress (busy).

6.1.4.21 eSPI Upstream Control 1 (ESUCTRL1)

Address Offset: B1h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0b	**Upstream Cycle Type** 7h: OOB Message 8h: Flash Read 9h: Flash Write Ah: Flash Erase Otherwise: Reserved

6.1.4.22 eSPI Upstream Control 2 (ESUCTRL2)

Address Offset: B2h

Bit	R/W	Default	Description
7-4	R/W	0h	**Upstream Tag** The written data will be filled in the Tag field of the upstream transaction.
3-0	R/W	0h	**Upstream Length** The written data will be filled in the Length[11:8] field of the upstream transaction.

6.1.4.23 eSPI Upstream Control 3 (ESUCTRL3)

Address Offset: B3h

Bit	R/W	Default	Description
0	R/W	00h	**Upstream Length** The written data will be filled in the Length[7:0] field of the upstream transaction.

6.1.4.24 eSPI Upstream Control 6 (ESUCTRL6)

Address Offset: B6h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R	0b	**PUT_FLASH_C Cycle Type** It stores the decoded cycle type in a received flash completion transaction. 0h: Successful Completion Without Data 4h: Successful Completion With Data / the only completion 5h: Unsuccessful Completion Without Data / the last completion 6h: Unsuccessful Completion Without Data / the only completion Fh: Invalid Cycle Type Otherwise: Reserved

6.1.4.25 eSPI Upstream Control 7 (ESUCTRL7)

Address Offset: B7h

Bit	R/W	Default	Description
7-4	R	0b	**PUT_FLASH_C Tag** It stores the Tag field in a received flash completion transaction.
3-0	-	-	**Reserved**

6.1.4.26 eSPI Upstream Control 8 (ESUCTRL8)

Address Offset: B8h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-0	R	0b	**PUT_FLASH_C Length** It stores the Length field in a received flash completion transaction.

6.1.4.27 eSPI OOB Control 0 (ESOCTRL0)

Address Offset: C0h

Bit	R/W	Default	Description
7	R/WC	0b	**PUT_OOB Status** It indicates that the eSPI slave has received a PUT_OOB message. Write-1 to clear this bit for the next coming posted transaction.
6-0	-	-	**Reserved**

6.1.4.28 eSPI OOB Control 1 (ESOCTRL1)

Address Offset: C1h

Bit	R/W	Default	Description
7	R/W	0b	**PUT_OOB Interrupt Enable** 0b: Interrupt disabled 1b: Interrupt enabled
6-0	-	-	**Reserved**

6.1.4.29 eSPI OOB Control 4 (ESOCTRL4)

Address Offset: C4h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-0	R	00h	**PUT_OOB Length** It stores the Length field in a received PUT_OOB Message packet.

6.1.4.30 eSPI SAFS Control 0 (ESPISAFSC0)

Address Offset: D0h

Bit	R/W	Default	Description
7	R/W	0b	**PUT_FLASH_NP Interrupt Enable** 0b: Interrupt disabled 1b: Interrupt enabled
6-2	-	-	**Reserved**
1	R/W	0b	**PUT_FLASH_NP Flash Erase Software Mode Enable** 0b: Process flash erase sequences by hardware. 1b: Process flash erase sequences with software's intervention.
0	R/W	0b	**PUT_FLASH_NP Flash Write Software Mode Enable** 0b: Process flash program sequences by hardware. 1b: Process flash program sequences with software's intervention.

6.1.4.31 eSPI SAFS Control 1 (ESPISAFSC1)

Address Offset: D1h

Bit	R/W	Default	Description
7	R/WC	0b	**PUT_FLASH_NP Status** It indicates that the eSPI slave has received a PUT_FLASH_NP packet. Write 1 to clear this bit for the next coming transaction.
6-2	-	-	**Reserved**
1-0	R	00h	**PUT_FLASH_NP Cycle Type** It stores the decoded cycle type in a received PUT_FLASH_NP packet. 1h: Flash write 2h: Flash erase Otherwise: Reserved

6.1.4.32 eSPI SAFS Control 2 (ESPISAFSC2)

Address Offset: D2h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

6.1.4.33 eSPI SAFS Control 3 (ESPISAFSC3)

Address Offset: D3h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-0	R	00h	**PUT_FLASH_NP Length** It stores the length field in a received PUT_FLASH_NP packet.

6.1.4.34 eSPI SAFS Control 4 (ESPISAFSC4)

Address Offset: D4h

Bit	R/W	Default	Description
7-0	R	00h	**PUT_FLASH_NP Address[31:24]** It stores the address field in a received PUT_FLASH_NP packet.

6.1.4.35 eSPI SAFS Control 5 (ESPISAFSC5)

Address Offset: D5h

Bit	R/W	Default	Description
7-0	R	00h	**PUT_FLASH_NP Address[23:16]** It stores the address field in a received PUT_FLASH_NP packet.

6.1.4.36 eSPI SAFS Control 6 (ESPISAFSC6)

Address Offset: D6h

Bit	R/W	Default	Description
7-0	R	00h	**PUT_FLASH_NP Address[15:8]** It stores the address field in a received PUT_FLASH_NP packet.

6.1.4.37 eSPI SAFS Control 7 (ESPISAFSC7)

Address Offset: D7h

Bit	R/W	Default	Description
7-0	R	00h	**PUT_FLASH_NP Address[7:0]** It stores the address field in a received PUT_FLASH_NP packet.

6.1.5 EC Interface Registers, eSPI VW

The EC interface registers are listed below. The base address for eSPI VW is 3200h.

Table 6-2. EC View Register Map, eSPI VW

7 0	Offset
VW Index 0 (VWIDX0)	00h
VW Index 2-7 (VWIDX2-7)	02h-07h
VW Index 40-47 (VWIDX40-47)	40h-47h
VW Contrl 0 (VWCTRL0)	90h

7	0	Offset
VW Contrl 1 (VWCTRL1)		91h
VW Contrl 2 (VWCTRL2)		92h
VW Contrl 3 (VWCTRL3)		93h
VW Contrl 5 (VWCTRL5)		95h
VW Contrl 6 (VWCTRL6)		96h
VW Contrl 7 (VWCTRL7)		97h

6.1.5.1 VW Index 0 (VWIDX0)

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	0b	**Interrupt Level** 0b: Low 1b: High
6-4	-	-	**Reserved**
3-0	R/W	11b	**Interrupt Line** IRQ0-15

6.1.5.2 VW Index 2-7 (VWIDX2-7)

Address Offset: 02h-07h

Bit	R/W	Default	Description
7-4	R/W	0b	**Valid** 0b: Low 1b: High
3-0	R/W	11b	**Level** 0b: Low 1b: High These registers correspond to the eSPI specification.

6.1.5.3 VW Index 40-47 (VWIDX40-47)

Address Offset: 40h-47h

Bit	R/W	Default	Description
7-4	R/W	0b	**Valid** 0b: Low 1b: High
3-0	R/W	11b	**Level** 0b: Low 1b: High These registers correspond to the Skylake specification.

6.1.5.4 VW Contrl 0 (VWCTRL0)

Address Offset: 90h

Bit	R/W	Default	Description
7	R/W	0b	**VW Interrupt Enable** 0b: Disable 1b: Enable
6-2	-	-	**Reserved**

Bit	R/W	Default	Description
1	R/W	0b	**Auto Send VW SUS_ACK# Interrupt Enable (ASVWSIE)** 0b: Disable 1b: Issue an interrupt if ASVWSF is set.
0	R/W	0b	**Auto Send VW Boot_Load_Done/Status Interrupt Enable (ASVWBIE)** 0b: Disable 1b: Issue an interrupt if ASVWBF is set.

6.1.5.5 VW Contrl 1 (VWCTRL1)

Address Offset: 91h

Bit	R/W	Default	Description
7	R/WC	0b	**VWIDX47 Updated Flag** Write-1 to clear this bit.
6	R/WC	0b	**VWIDX44 Updated Flag** Write-1 to clear this bit.
5	R/WC	0b	**VWIDX43 Updated Flag** Write-1 to clear this bit.
4	R/WC	0b	**VWIDX42 Updated Flag** Write-1 to clear this bit.
3	R/WC	0b	**VWIDX41 Updated Flag** Write-1 to clear this bit.
2	R/WC	0b	**VWIDX7 Updated Flag** Write-1 to clear this bit.
1	R/WC	0b	**VWIDX3 Updated Flag** Write-1 to clear this bit.
0	R/WC	0b	**VWIDX2 Updated Flag** Write-1 to clear this bit.

6.1.5.6 VW Contrl 2 (VWCTRL2)

Address Offset: 92h

Bit	R/W	Default	Description
7	R/W	0b	**DSW_PWROK Source** 0b: Refers to SW_DSW_PWROK for DSW_PWROK. 1b: Refers to eSPI Reset# for DSW_PWROK.
6	R/W	0b	**SW_DSW_PWROK** Scratch bit and read returns the written data.
5	R/W	0b	**Platform Reset Control** 0b: Refers to PLTRST# virtual wire for Platform Reset. 1b: Refers to GPD4 for Platform Reset.
5-0	-	-	**Reserved**

6.1.5.7 VW Contrl 3 (VWCTRL3)

Address Offset: 93h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**VW Index 46 Resend** Write-1 to resend VW Index 46 over eSPI bus. This bit is automatically cleared after the transaction.

Bit	R/W	Default	Description
4	R/W	0b	**VW Index 45 Resend** Write-1 to resend VW Index 45 over eSPI bus. This bit is automatically cleared after the transaction.
3	R/W	0b	**VW Index 40 Resend** Write-1 to resend VW Index 40 over eSPI bus. This bit is automatically cleared after the transaction.
2	R/W	0b	**VW Index 6 Resend** Write-1 to resend VW Index 6 over eSPI bus. This bit is automatically cleared after the transaction.
1	R/W	0b	**VW Index 5 Resend** Write-1 to resend VW Index 5 over eSPI bus. This bit is automatically cleared after the transaction.
0	R/W	0b	**VW Index 4 Resend** Write-1 to resend VW Index 4 over eSPI bus. This bit is automatically cleared after the transaction.

6.1.5.8 VW Contrl 5 (VWCTRL5)

Address Offset: 95h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**VW SUS_WARN# Select (VWSS)** 0b: If ASVWSE is set to 1, EC sends SUS_ACK# after SUS_WARN# is deasserted. 1b: If ASVWSE is set to 1, EC sends SUS_ACK# after SUS_WARN# is asserted.
3-2	-	-	**Reserved**
1	R/W	0b	**Auto Send VW SUS_ACK# Enable (ASVWSE)** eSPI_Reset# is the fundamental reset to the eSPI interface. While MAFS configuration is enabled for a platform, EC may not fetch the codes through MAFS if an unexpected eSPI_Reset# event occurs. Set this bit to allow EC to send VW SUS_ACK# automatically after the eSPI master deasserts/asserts SUS_WARN#. 0b: Disable 1b: Enable
0	R/W	0b	**Auto Send VW Boot_Load_Done/Status Enable (ASVWBE)** eSPI_Reset# is the fundamental reset to the eSPI interface. While MAFS configuration is enabled for a platform, EC may not fetch the codes through MAFS if an unexpected eSPI_Reset# event occurs. Set this bit to allow EC to send VW Boot_Load_Done/Status automatically after an unexpected eSPI_Reset# event is deasserted. 0b: Disable 1b: Enable

6.1.5.9 VW Contrl 6 (VWCTRL6)

Address Offset: 96h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/WC	0b	**Auto Send VW SUS_ACK# Flag (ASVWSF)** Write 1 to clear this bit. 0b: Otherwise. 1b: VW SUS_ACK# has been sent automatically.
0	R/WC	0b	**Auto Send VW Boot_Load_Done/Status Flag (ASVWBF)** Write 1 to clear this bit. 0b: Otherwise. 1b: VW Boot_Load_Done/Status has been sent automatically.

6.1.5.10 VW Contrl 7 (VWCTRL7)

Address Offset: 97h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Auto Send VW SUS_ACK# Select (ASVWSS)** 0b: If ASVWSE is 1, EC sends SUS_ACK# =0. 1b: If ASVWSE is 1, EC sends SUS_ACK# =1.

6.1.6 EC Interface Registers, eSPI Queue 0

The EC interface registers are listed below. The base address for eSPI Queue 0 is 3300h.

Table 6-3. EC View Register Map, eSPI Queue 0

7 0	Offset
PUT_PC Data Byte 0-63	00h-3Fh
PUT_OOB Data Byte 0-79	80h-CFh

6.1.6.1 PUT_PC Data Byte 0-63 (PUTPCDB0-63)

Address Offset: 00h-3Fh

Bit	R/W	Default	Description
7-0	R	-	**PUT_PC Data Byte 0-63**

6.1.6.2 PUT_OOB Data Byte 0-79 (PUTOOBDB0-79)

Address Offset: 80h-CFh

Bit	R/W	Default	Description
7-0	R	-	**PUT_OOB Data Byte 0-79**

6.1.7 EC Interface Registers, eSPI Queue 1

The EC interface registers are listed below. The base address for eSPI Queue 1 is 3400h.

Table 6-4. EC View Register Map, eSPI Queue 1

7 0	Offset
Upstream Data Byte 0-79	00h-4Fh
PUT_FLASH_NP Data Byte 0-63	80h-BFh

6.1.7.1 Upstream Data Byte 0-79 (UDB0-79)

Address Offset: 00h-4Fh

Bit	R/W	Default	Description
7-0	R/W	-	**Upstream Data Byte 0-79**

6.1.7.2 PUT_FLASH_NP Data Byte 0-63 (PUTFLASHNPDB0-63)

Address Offset: 80h-BFh

Bit	R/W	Default	Description
7-0	R	-	**PUT_FLASH_NP Data Byte 0-63**

6.2 Low Pin Count Interface

6.2.1 Overview

The Low Pin Count (LPC) is an interface for modern ISA-free system. It is defined in Intel's LPC Interface Specification, Revision 1.1. There are seven host-controlled modules that can be accessed by the host via the LPC interface. These host-controlled modules are "Logical Devices" defined in Plug and Play ISA Specification, Version 1.0a.

6.2.2 Features

- Complies with Intel's LPC Interface Specification, Revision 1.1
- Supports SERIRQ and complies with Serialized IRQ Support for PCI Systems, Revision 6.0
- Supports LPCPD#/CLKRUN#
- Supports Plug and Play ISA registers
- Supports LPC 19.2MHz to 33MHz

6.2.3 Accepted LPC Cycle Type

The supported LPC cycle types are listed below:
* LPC I/O Read(16-bit address, 8-bit data)
* LPC I/O Write (16-bit address, 8-bit data)
* LPC Memory Read(32-bit address, 8-bit data)
* LPC Memory Write(32-bit address, 8-bit data)
* FWH Read (32-bit address, 8-bit data)
* FWH Write (32-bit address, 8-bit data)

I/O cycles are used to access PNPCFG and Logical Devices. Memory or FWH is used to access Flash content through SMFI module Host-Indirect memory cycles based on I/O cycles able to access Flash as well. Refer to SMFI Module for the detail about Host-Indirect memory access.

The following table describes how LPC module responds the I/O, Memory and FWH cycles from Host side in different conditions.

Table 6-5. LPC/FWH Response

Cycle Type/Condition	Read Response	Write Response
All Cycles before PLL Stable [NOTE 4]	Long-Wait	Long-Wait
I/O Cycle to PNPCFG or Logical Devices	Ready	Ready
I/O Cycle but Address Out Of Range	Cycle Ignored	Cycle Ignored
I/O Cycle to Locked PNPCFG by EC2I	Returns 00h	Cycle Ignored
Host-Indirect Memory Address [NOTE 3]	Ready	Ready
Memory Cycle, FWH Cycle or Host-Indirect Memory Data	Long-Waits until Ready	Long-Waits until Ready [NOTE 1]
Memory Cycle, FWH Cycle or Host-Indirect Memory Data but Address Protected by SMFI HERES=01	Returns 00h	Cycle Ignored
Memory Cycle or Host-Indirect Memory Data but Address Out of Range	Cycle Ignored	Cycle Ignored
FWH Cycle but Address Out of Range	Ready	Ready
FWH Cycle but FWH ID is unmatched [NOTE 2]	Cycle Ignored	Cycle Ignored
FWH Cycle but HBREN bit in HCTRL2R register cleared	Cycle Ignored	Cycle Ignored

Note 1:
After reset, IT81202 responds Long-Waits before Ready for FWH Write Cycle.

If LPC host (South-Bridge) fails to recognize Long-Wait SYNC during FWH Write Cycle, it is recommended to use Host-Indirect Memory.

Note 2:
FWH ID is defined in FWHID field in SHMC register.

Note 3:
Host-Indirect Memory Cycles access the flash via LPC I/O Cycle. Host-Indirect Memory Address is combined with SMIMAR0, SMIMAR1, SMIMAR2 and SMIMAR3 registers. Host-Indirect Memory Data is SMIMDR register.

Note 4:
The host LPC interface is disabled in Sleep mode.

6.2.4 Debug Port Function

LPC module implements two latch signals for Main-Board debug purpose. LPC I/O write cycles with address equal to 80h will cause the LPC module to assert L80HLAT and L80LLAT signals which provide a simple external logic to latch it in order to display on LED, even though I/O port 80h is not recognized by PNPCFG or any Logical Device. L80HLAT goes high when it is time to latch the high-nibble of the data written to port 80h, and L80LLAT means the low-nibble.

Port 80h data can be read via parallel port with the software provided by ITE.

6.2.5 Serialized IRQ (SERIRQ)

IT81202 has programmable IRQ number for each logical device. Available IRQ numbers are 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, and 15.

Different logical devices inside IT81202 can share the same IRQ number if they have the same IRQPS bit in IRQTP register and are configured as the same triggered mode (all level-triggered or all edge-triggered) in their EC side registers.

But it is not allowed to share an IRQ number with a logical device outside IT81202. Note that edge-triggered interrupts are not suitable for sharing in most cases.

6.2.6 Related Interrupts to WUC

- Interrupt to WUC
  If the LPC address of an I/O, LPC Memory or FWH Cycle on LPC bus is accepted, WU42 interrupt will be asserted.

6.2.7 LPCPD# and CLKRUN#

- LPCPD#
  LPCPD# is used as an internal “power good” signal to indicate the status of VCC. It is recommended to be implemented. See also VCCDO bit in RSTS register in 7.15.4.6 on page 429.

- CLKRUN#
  When SERIRQ is in the continuous/quiet mode and LPCCLK is active, CLKRUN# is used for maintaining LPCCLK to make sure that the SERIRQ status is entirely transferred to the host side.

  When SERIRQ is in the quiet mode and LPCCLK is stopped, CLKRUN# is used for restoring LPCCLK if there is any interrupt status transition required to be transferred to the host side.

6.2.8 Check Items

If EC fails in LPC memory or I/O cycles at boot, check the following recommended items first.

- LPC/FWH memory cycles
  Check whether LPCRST# reset source from GPD2 or GPB7 is logic low if it is in alternative function.
  Check whether LPCPD# signal from GPE6 is logic low if it is in alternative function.
  Check whether HBREN bit is enabled in HCTRL2R register.
  Check whether the firmware doesn't change the read protection control.

- LPC I/O cycles
  Check whether LPCRST# reset source from GPD2 or GPB7 is logic low if it is in alternative function.
  Check whether LPCPD# signal from GPE6 is logic low if it is in alternative function.
  Check whether BADDR1-0 field in BADRSEL register are in correct setting.
  Check whether EC2I is not locking PNPCFG access from the host side.

6.3 Plug and Play Configuration (PNPCFG)

The host interface registers of PNPCFG (Plug and Play Configuration) are listed below. The base address can be configured via BADDR1-0 field in BADRSEL register. Note that bit 0 of SWCBALR has to be zero.

To access a register of PNPCFG, write target index to address port and access this PNPCFG register via data port. If accessing the data port without writing index to address port, the latest value written to address port is used as the index. Reading the address port register returns the last value written to it.

Table 6-6. Host View Register Map, PNPCFG

7 0	BADDR1-0 =00b	BADDR1-0 =01b	BADDR1-0 =10b	BADDR1-0 =11b
	I/O Port Address			
Address Port	2Eh	4Eh	(SWCBAHR, SWCBALR)	Reserved
Data Port	2Fh	4Fh	(SWCBAHR, SWCBALR+1)	Reserved

Note 1: SWCBALR should be on boundary = 2, which means bit 0 has to be 0.
Note 2: Only use BADDR1-0=10b if the port pair is not 2Eh/2Fh or 4Eh/4Fh.

The host interface registers for Logic Device Control are listed below. The base address can be configured via the following Plug and Play Configuration Registers. Note that if a logical device is activated but with base address equal to 0000h, the host side cannot access this logical device since 0000h means the I/O address range is disabled.

Table 6-7. Host View Register Map, Logical Devices

7 0	I/O Port Address
Serial Port 1 (UART1)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+07h) Base address boundary = 16 Legacy Address = 03F8h
Serial Port 2 (UART2)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+07h) Base address boundary = 16 Legacy Address = 02F8h
System Wake-Up Control (SWUC)	Depend on PnP SW Used Addr: (IOBAD0+00h,+02h,+06h,+07h,13h,15h) Base address boundary = 32
KBC / Mouse Interface	Unused
KBC / Keyboard Interface	Depend on PnP SW Used Addr: (IOBAD0+00h), (IOBAD1+00h) Base address boundary = none, none Legacy Address = 60h,64h
Shared Memory/Flash Interface (SMFI)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+8h,+0Ch) Base address boundary = 16
Power Management I/F Channel 1 (PMC1)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 62h,66h
Power Management I/F Channel 2 (PMC2)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 68h,6Ch

7 0	I/O Port Address
Power Management I/F Channel 3 (PMC3)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 6Ah,6Eh
Power Management I/F Channel 4 (PMC4)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 74h,78h
Power Management I/F Channel 5 (PMC5)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 7Ah,7Ch
Serial Peripheral Interface (SSPI)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+03h) Base address boundary = 4
Platform Environment Control Interface (PECI)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+07h) Base address boundary = 8

Note: The boundary number means the address has to be the multiple of this number.

The host interface registers for Standard Plug and Play Configuration of PNPCFG are listed below. These registers are accessed via the Index-Data I/O ports defined in Table 6-7 on page 73. Note PNPCFG registers are not allowed to be accessed if LKCFG bit in LSIOHA register of EC2I module is set. They are divided into two parts, Super I/O Configuration Registers and Logical Device Registers.

Table 6-8. Host View Register Map via Index-Data I/O Pair, Standard Plug and Play Configuration Registers

	Register Name (7 … 0)	Index
Super I/O Configuration Registers	Logical Device Number (LDN)	07h
	Chip ID Byte 1(CHIPID1)	24h
	Chip ID Byte 2(CHIPID2)	20h
	Chip ID Byte 3(CHIPID3)	21h
	Chip Version (CHIPVER)	22h
	Super I/O Control (SIOCTRL)	23h
	Super I/O IRQ Configuration (SIOIRQ)	25h
	Super I/O General Purpose (SIOGP)	26h
	Reserved	27h
	Reserved	28h
	Reserved	29h
	Reserved	2Ah
	Reserved	2Bh
	Super I/O Power Mode (SIOPWR)	2Dh
	Depth 2 I/O Address (D2ADR)	2Eh
	Depth 2 I/O Data (D2DAT)	2Fh
Logical Device Configuration Registers Selected by LDN Register	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

7 … 0	Index
DMA Channel Select 0 (DMAS0)	74h
DMA Channel Select 1 (DMAS1)	75h
Device Specific Logical Device Configuration 1 to 10	F0h-F9h

The IRQ numbers for Logic Device IRQ via LPC/SERIRQ are listed below. The IRQ numbers can be configured via the above Plug and Play Configuration Registers.

Table 6-9. Interrupt Request (IRQ) Number Assignment, Logical Device IRQ via SERIRQ

Logical Device	IRQ number
Serial Port 1 (UART1)	Depend on PnP SW, Legacy IRQ Num=04
Serial Port 2 (UART2)	Depend on PnP SW, Legacy IRQ Num=03
System Wake-Up Control (SWUC)	Depend on PnP SW
KBC / Mouse Interface	Depend on PnP SW, Legacy IRQ Num=12
KBC / Keyboard Interface	Depend on PnP SW, Legacy IRQ Num=01
Shared Memory/Flash Interface (SMFI)	Unused
Power Management I/F Channel 1 (PMC1)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 2 (PMC2)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 3 (PMC3)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 4 (PMC4)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 5 (PMC5)	Depend on PnP SW, Legacy IRQ Num=01
Serial Peripheral Interface (SSPI)	Depend on PnP SW
Platform Environment Control Interface (PECI)	Unused

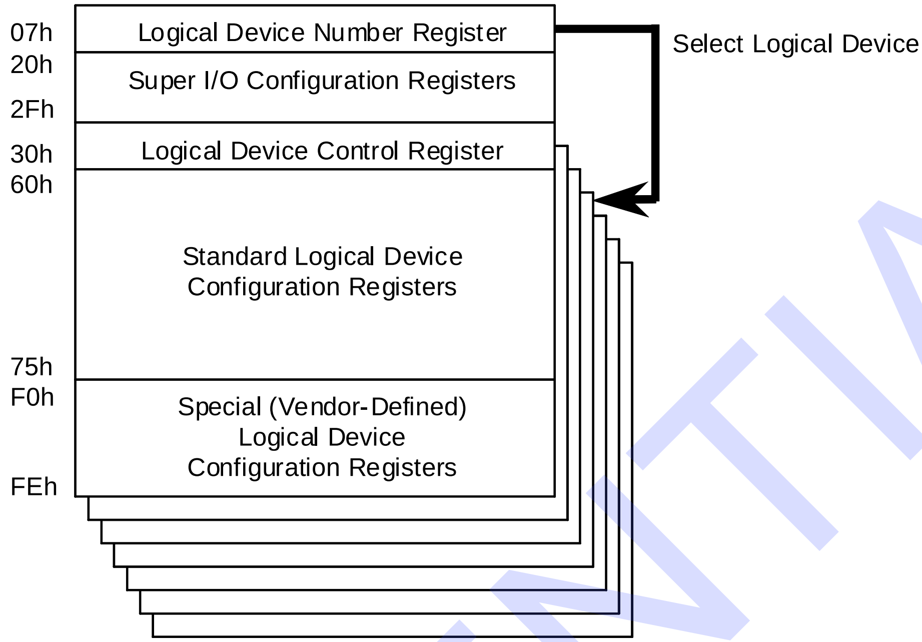
6.3.1 Logical Device Assignment

Table 6-10. Logical Device Number (LDN) Assignments

LDN	Functional Block
01h	Serial Port 1 (UART1)
02h	Serial Port 2 (UART2)
04h	System Wake-Up Control (SWUC)
05h	KBC/Mouse Interface
06h	KBC/Keyboard Interface
0Fh	Shared Memory/Flash Interface (SMFI)
11h	Power Management I/F Channel 1 (PMC1)
12h	Power Management I/F Channel 2 (PMC2)
13h	Serial Peripheral Interface (SSPI)
14h	Platform Environment Control Interface (PECI)
17h	Power Management I/F Channel 3 (PMC3)
18h	Power Management I/F Channel 4 (PMC4)
19h	Power Management I/F Channel 5 (PMC5)

The following figure indicates the PNPCFG registers are combined with Super I/O Configuration Registers and Logical Device Configuration Registers. Logical Device Configuration Registers of a specified Logical Device is accessible only when Logical Device Number Register is filled with corresponding Logical Device Number listed in Table 6-10 on page 75 .

Figure 6-13. Host View Register Map via Index-Data Pair



6.3.1.1 Super I/O Configuration Registers

Registers with index from 07h to 2Eh contain Super I/O configuration settings.

6.3.1.2 Logical Device Number (LDN)

This register contains general Super I/O configurations.

Index: 07h

Bit	R/W	Default	Description
7-0	R/W	04h	**Logical Device Number (LDN)** This register selects the current logical device. All other values are reserved.

6.3.1.3 Chip ID Byte 1 (CHIPID1)

Index: 24h

Bit	R/W	Default	Description
7-0	R	08h	**Chip ID Byte 1 (CHIPID1)** This register contains the Chip ID byte 1.

6.3.1.4 Chip ID Byte 2 (CHIPID2)

Index: 20h

Bit	R/W	Default	Description
7-0	R	12h	**Chip ID Byte 2 (CHIPID2)** This register contains the Chip ID byte 2.

6.3.1.5 Chip ID Byte 3 (CHIPID3)

Index: 21h

Bit	R/W	Default	Description
7-0	R	02h	**Chip ID Byte 3 (CHIPID3)** This register contains the Chip ID byte 3.

6.3.1.6 Chip Version (CHIPVER)

This register contains revision ID of this chip

Index: 22h

Bit	R/W	Default	Description
7-4	R	-	**Embedded Flash Size** Ah: 0KB 4h: 256KB 8h: 512KB Ch: 1MB
3-0	R	1h	**Chip Version (CHIPVER)**

6.3.1.7 Super I/O IRQ Configuration Register (SIOIRQ)

This register contains general Super I/O configurations.

Index: 25h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0b	**SMI# to IRQ2 Enable (SMI2IRQ2)** This bit enables using IRQ number 2 in the SERIRQ protocol as an SMI# interrupt. This bit is similar to LDACT bit in LDA register. 0: Disable 1: Enable
3-0	-	0h	**Reserved**

6.3.1.8 Super I/O General Purpose Register (SIOGP)

This register contains general Super I/O configurations.

Index: 26h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-5	R/W	00b	**General-Purpose Scratch (GPSCR)** Reading returns the value that was previously written. Note that the EC side can access whole PNPCFG registers via EC2I.
4-0	-	0h	**Reserved**

6.3.1.9 Super I/O Power Mode Register (SIOPWR)

This register is a battery-backed register used by the EC side. See also 6.5.5.2.

Index: 2Dh

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/W	0b	**Power Supply Off (PWRSLY)** It indicates the EC side that the host requests to shut down the power in legacy mode. Refer to SCRDPSO bit in SWCTL2 register on page 152 0: No action 1: It indicates power shuts down if PWRSLY is Legacy mode. **Note:** It always returns 0 when read.
0	R/W	0h	**Power Button Mode (PWRBTN)** This bit controls the power button mode in the SWUC. Refer to SCRDPBM bit in SWCTL2 register on page 152 0: Legacy 1: ACPI

6.3.1.10 Depth 2 I/O Address (D2ADR)

For the address/data pair (a.k.a. index/data pair) listed in Table 6-6. Host View Register Map, PNPCFG on page 73, there are two registers to create a sub address space containing 256 addresses, and its depth is 1.

In addition, there are two registers (D2ADR and D2DAT) to create a further sub address, and its depth is 2.

In the depth 2 address space, there are following three registers.
Offset 10h: I2EC_ADDR_L
Offset 11h: I2EC_ADDR_H
Offset 12h: I2EC_DATA

Index: 2Eh

Bit	R/W	Default	Description
7-0	R/W	-	**D2ADR**

6.3.1.11 Depth 2 I/O Data (D2DAT)

Index: 2Fh

Bit	R/W	Default	Description
7-0	R/W	-	**D2DAT**

6.3.2 Standard Logical Device Configuration Registers

Registers with index from 30h to F9h contain Logical Device configuration settings. LDN of the wanted logical device should be written to LDN register before accessing these registers.

This section lists a standard description of these registers. Some default values for each register and more detailed information for each logical device should be referred in each section.

6.3.2.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-1	-	0h	**Reserved**

Bit	R/W	Default	Description
0	R/W	0b	**Logical Device Activation Control (LDACT)** 0: Disable The registers (Index 60h-FEh) are not accessible. 1: Enable

6.3.2.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBA[15:8])** This register indicates selected I/O base address bits 15-8 for I/O Descriptor 0.

6.3.2.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBA[7:0])** This register indicates selected I/O base address bits 7-0 for I/O Descriptor 0.

6.3.2.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBA[15:8])** This register indicates selected I/O base address bits 15-8 for I/O Descriptor 1.

6.3.2.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBA[7:0])** This register indicates selected I/O base address bits 7-0 for I/O Descriptor 1.

6.3.2.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

This register will be read-only if it is unused by a logical device.

Index: 70h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0	**Wake-Up IRQ Enable (WKIRQEN)** Allow this logical device to trigger a wake-up event to SWUC. This bit should not be set in SWUC Logical Device since it is used to collect IRQ sources for SWUC. 0: Disable 1: Enable
3-0	R/W	Depend on Logical Device	**IRQ Number (IRQNUM)** Select the IRQ number (level) asserted by this logical device via SERIRQ. 00d: This logical device doesn't use IRQ. 01d-012d: IRQ1-12 are selected correspondingly. 14d-15d: IRQ14-15 are selected correspondingly. Otherwise: Invalid IRQ routing configuration.

6.3.2.7 Interrupt Request Type Select (IRQTP)

This register will be read-only if it is unused by a logical device.

Index: 71h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/W	Depend on Logical Device	**Interrupt Request Polarity Select (IRQPS)** This bit indicates the polarity of the interrupt request. 0: IRQ request is buffered and applied to SERIRQ. 1: IRQ request is inverted before being applied to SERIRQ. This bit should be configured before the logical device is activated.
0	R/W	Depend on Logical Device	**Interrupt Request Triggered Mode Select (IRQTMS)** This bit indicates that edge or level triggered mode is used by this logical device and should be updated by EC firmware via EC2I since the triggered mode is configured in EC side registers. This bit is just read as previously written (scratch register bit) and doesn't affect SERIRQ operation. 0: Edge triggered mode 1: Level triggered mode

6.3.2.8 DMA Channel Select 0 (DMAS0)

Index: 74h

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2-0	R	4h	**DMA Channel Select 0** A value of 4 indicates that no DMA channel is active.

6.3.2.9 DMA Channel Select 1 (DMAS1)

Index: 75h

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2-0	R	4h	**DMA Channel Select 1** A value of 4 indicates that no DMA channel is active.

6.3.3 Serial Port 1 (UART1) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-11. Host View Register Map via Index-Data I/O Pair, UART1 Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	High Speed Baud Rate Select (HHS)	F0h

6.3.3.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.3.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.3.2.2 on page 79.** Bit 7-4 (IOBAD0[15:12]) are forced to 0000b and can't be written.

6.3.3.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	F8h	**Refer to section 6.3.2.3 on page 79.** Bit 3-0 (IOBAD0[3:0]) are forced to 8h and can't be written. It means the base address is on the 16-byte boundary.

6.3.3.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.4 on page 79.**

6.3.3.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.5 on page 79.**

6.3.3.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	04h	**Refer to section 6.3.2.6 on page 79.**

6.3.3.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.2.7 on page 80.**

6.3.3.8 High Speed Baud Rate Select (HHS)

Index: F0h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	R/W	0b	**High Speed Baud Rate Select (HHS)** This bit indicates that the baud rate of UART1 can be up to 230.4K/460.8K baud, which is determined by the divisor of the baud rate generator. (From Host Side) 0: Not selected 1: Selected
0	-	0b	**Reserved**

6.3.4 Serial Port 2 (UART2) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-12. Host View Register Map via Index-Data I/O Pair, UART2 Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	High Speed Baud Rate Select (HHS)	F0h

6.3.4.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.4.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.2.2 on page 79.** Bit 7-4 (IOBAD0[15:12]) are forced to 0000b and can't be written.

6.3.4.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	F8h	**Refer to section 6.3.2.3 on page 79.** Bit 3-0 (IOBAD0[3:0]) are forced to 8h and can't be written. It means the base address is on the 16-byte boundary.

6.3.4.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.4 on page 79.**

6.3.4.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.5 on page 79.**

6.3.4.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.3.2.6 on page 79.**

6.3.4.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.2.7 on page 80.**

6.3.4.8 High Speed Baud Rate Select (HHS)

Index: F0h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	R/W	0b	**High Speed Baud Rate Select (HHS)** This bit indicates that the baud rate of UART2 can be up to 230.4K/460.8K baud, which is determined by the divisor of the baud rate generator. (From Host Side) 0: Not selected 1: Selected
0	-	0b	**Reserved**

6.3.5 System Wake-Up Control (SWUC) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-13. Host View Register Map via Index-Data I/O Pair, SWUC Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.5.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.5.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.2 on page 79.**

6.3.5.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.3 on page 79.** Bits 4-0 (IOBAD0[4:0]) are forced to 00000b and can't be written. It means the base address is on the 32-byte boundary.

6.3.5.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.4 on page 79.**

6.3.5.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.5 on page 79.**

6.3.5.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.6 on page 79.**

6.3.5.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.7 on page 80.**

6.3.6 KBC / Mouse Interface Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-14. Host View Register Map via Index-Data I/O Pair, KBC / Mouse Interface Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8]) – Unused	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0]) –Unused	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8]) – Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) –Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.6.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.6.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

This register is unused and read-only.

Index: 60h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.2 on page 79.**

6.3.6.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

This register is unused and read-only.

Index: 61h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.3 on page 79.**

6.3.6.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.4 on page 79.**

6.3.6.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.5 on page 79.**

6.3.6.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	0Ch	**Refer to section 6.3.2.6 on page 79.**

6.3.6.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.7 on page 80.**

6.3.7 KBC / Keyboard Interface Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-15. Host View Register Map via Index-Data I/O Pair, KBC / Keyboard Interface Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.7.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.7.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.2 on page 79.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.3.7.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	60h	**Refer to section 6.3.2.3 on page 79.**

6.3.7.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.4 on page 79.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.3.7.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	64h	**Refer to section 6.3.2.5 on page 79.**

6.3.7.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.6 on page 79.**

6.3.7.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.7 on page 80.**

6.3.8 Consumer IR Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-16. Host View Register Map via Index-Data I/O Pair, Consumer IR Interface Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.8.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.8.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.3.2.2 on page 79.**

6.3.8.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	10h	**Refer to section 6.3.2.3 on page 79.** Bit 2-0 (IOBAD0[2:0]) are forced to 000b and can't be written.

6.3.8.4 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.6 on page 79.**

6.3.8.5 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R	02h	**Refer to section 6.3.2.7 on page 80.**

6.3.9 Shared Memory/Flash Interface (SMFI) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-17. Host View Register Map via Index-Data I/O Pair, SMFI Interface Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])-Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	LPC Memory Window Base Address [31:24] (LPCMWBA)	F0h
	LPC Memory Window Base Address [23:16] (LPCMWBA)	F1h
	LPC Memory Window Mapping Region Select (LPCMWMRS)	F2h
	LPC Memory Window Control Register (LPCMWCR)	F3h
	Shared Memory Configuration Register (SHMC)	F4h
	H2RAM-HLPC Base Address [15:12] (HLPCRAMBA[15:12])	F5h
	H2RAM-HLPC Base Address [23:16] (HLPCRAMBA[23:16])	F6h
	H2RAM Host Semaphore Interrupt Enable (H2RAMHSIE)	F9h
	H2RAM Host Semaphore Address (H2RAMHSA)	FAh

	7 0	Index
	H2RAM EC Semaphore Status (H2RAMECSS)	FBh
	H2RAM-HLPC Base Address [31:24] (HLPCRAMBA[31:24])	FCh

6.3.9.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.9.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.2 on page 79.**

6.3.9.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.3 on page 79.** Bits 3-0 (IOBAD0[3:0]) are forced to 0000b and can't be written. It means the base address is on the 16-byte boundary.

6.3.9.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.4 on page 79.**

6.3.9.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.5 on page 79.**

6.3.9.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.6 on page 79.**

6.3.9.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.2.7 on page 80.**

6.3.9.8 LPC Memory Window Base Address [31:24] (LPCMWBA[31:24])

The base address of LPC memory window should not overlap with legacy BIOS range, extended legacy BIOS range and HLPCRAMBA.

Index: F0h

Bit	R/W	Default	Description
7-0	R/W	00h	**LPC Memory Window Base Address [31:24] (LPCMWBA[31:24])** Specify the base address of the user-defined 64K window on LPC memory space for PCH LGMR application.

6.3.9.9 LPC Memory Window Base Address [23:16] (LPCMWBA[23:16])

Index: F1h

Bit	R/W	Default	Description
7-0	R/W	00h	**LPC Memory Window Base Address [23:16] (LPCMWBA[23:16])** Specify the base address of the user-defined 64K window on LPC memory space for PCH LGMR application.

6.3.9.10 LPC Memory Window Mapping Region Select (LPCMWMRS)

Index: F2h

Bit	R/W	Default	Description
7-0	R/W	00h	**LPC Memory Window Mapping Region Select (LPCMWMRS)** The LPC memory window is mapped into the region that ranges from (10000_0000h – flash size + 64K*LPCMWMRS) to (FFFF_FFFFh – flash size + 64K*(LPCMWMRS + 1)) on LPC memory space. The flash size is specified by FMSS.

6.3.9.11 LPC Memory Window Control Register (LPCMWCR)

Index: F3h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**LPC Memory Window Enable (LPCMWE)** 0b: Disable 1b: The address located in the user-defined LPC memory window of LPC memory space is mapped into the region of flash address space, which is defined by LPCMWMRS.

6.3.9.12 Shared Memory Configuration Register (SHMC)

Index: F4h

Bit	R/W	Default	Description
7-4	R/W	0h	**BIOS FWH ID (FWHID)** These bits correspond to the 4-bit ID, which is part of a FWH transaction.
3-2	-	-	**Reserved**
1	R/W	0b	**BIOS Extended Space Enable (BIOSEXTS)** This bit expands the BIOS address space to make this chip respond the Extended BIOS address range.
0	-	-	**Reserved**

6.3.9.13 H2RAM-HLPC Base Address [15:12] (HLPCRAMBA[15:12])

The H2RAM-HLPC base address is only within the range: XXXX_X000h. (X denotes it's programmable by registers).

The H2RAM-HLPC function will be disabled if SPI follow mode is enabled.

Index: F5h

Bit	R/W	Default	Description
7-4	R/W	0h	**H2RAM-HLPC Base Address Bits [15:12] (HLPCRAMBA[15:12])** If H2RAMPS is set to 0, this field defines EC internal RAM base address on LPC memory space. If H2RAMPS is set to 1, this field defines EC internal RAM base address on LPC IO space.
3-0	-	-	**Reserved**

6.3.9.14 H2RAM-HLPC Base Address [23:16] (HLPCRAMBA[23:16])

Index: F6h

Bit	R/W	Default	Description
7-0	R/W	00h	**H2RAM-HLPC Base Address Bits [23:16] (HLPCRAMBA[23:16])** If H2RAMPS is set to 0, this field defines EC internal RAM base address on LPC memory space. If H2RAMPS is set to 1, write 1b to HLPCRAMBA[16] to enable H2RAM LPC IO-path.

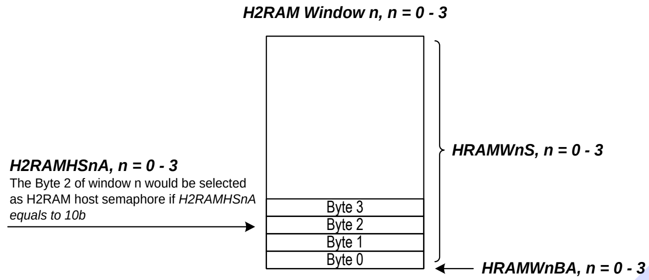
6.3.9.15 H2RAM Host Semaphore Interrupt Enable (H2RAMHSIE)

Address Offset: F9h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**H2RAM Host Semaphore 3 Interrupt Enable (H2RAMHS3IE)** 0b: Disable 1b: A LPC Memory/FWH/IO Write cycle targeted on H2RAM host semaphore 3 will produce an interrupt (INT83) to EC.
2	R/W	0b	**H2RAM Host Semaphore 2 Interrupt Enable (H2RAMHS2IE)** 0b: Disable 1b: A LPC Memory/FWH/IO Write cycle targeted on H2RAM host semaphore 2 will produce an interrupt (INT83) to EC.
1	R/W	0b	**H2RAM Host Semaphore 1 Interrupt Enable (H2RAMHS1IE)** 0b: Disable 1b: A LPC Memory/FWH/IO Write cycle targeted on H2RAM host semaphore 1 will produce an interrupt (INT83) to EC.
0	R/W	0b	**H2RAM Host Semaphore 0 Interrupt Enable (H2RAMHS0IE)** 0b: Disable 1b: A LPC Memory/FWH/IO Write cycle targeted on H2RAM host semaphore 0 will produce an interrupt (INT83) to EC.

6.3.9.16 H2RAM Host Semaphore Address (H2RAMHSA)

Figure 6-14. Location of H2RAM Host Semaphore



Address Offset: FAh

Bit	R/W	Default	Description
7-6	R/W	00b	**H2RAM Host Semaphore 3 Address (H2RAMHS3A)** 00b: H2RAM host semaphore 3 locates at (HRAMW3BA[11:0] + 0) 01b: H2RAM host semaphore 3 locates at (HRAMW3BA[11:0] + 1) 10b: H2RAM host semaphore 3 locates at (HRAMW3BA[11:0] + 2) 11b: H2RAM host semaphore 3 locates at (HRAMW3BA[11:0] + 3) This field is available only when H2RAM window 3 is enabled.
5-4	R/W	00b	**H2RAM Host Semaphore 2 Address (H2RAMHS2A)** 00b: H2RAM host semaphore 2 locates at (HRAMW2BA[11:0] + 0) 01b: H2RAM host semaphore 2 locates at (HRAMW2BA[11:0] + 1) 10b: H2RAM host semaphore 2 locates at (HRAMW2BA[11:0] + 2) 11b: H2RAM host semaphore 2 locates at (HRAMW2BA[11:0] + 3) This field is available only when H2RAM window 2 is enabled.
3-2	R/W	00b	**H2RAM Host Semaphore 1 Address (H2RAMHS1A)** 00b: H2RAM host semaphore 1 locates at (HRAMW1BA[11:0] + 0) 01b: H2RAM host semaphore 1 locates at (HRAMW1BA[11:0] + 1) 10b: H2RAM host semaphore 1 locates at (HRAMW1BA[11:0] + 2) 11b: H2RAM host semaphore 1 locates at (HRAMW1BA[11:0] + 3) This field is available only when H2RAM window 1 is enabled.
1-0	R/W	00b	**H2RAM Host Semaphore 0 Address (H2RAMHS0A)** 00b: H2RAM host semaphore 0 locates at (HRAMW0BA[11:0] + 0) 01b: H2RAM host semaphore 0 locates at (HRAMW0BA[11:0] + 1) 10b: H2RAM host semaphore 0 locates at (HRAMW0BA[11:0] + 2) 11b: H2RAM host semaphore 0 locates at (HRAMW0BA[11:0] + 3) This field is available only when H2RAM window 0 is enabled.

6.3.9.17 H2RAM EC Semaphore Status (H2RAMECSS)

The host can know the status of H2RAM EC semaphore by reading this register.

Address Offset: FBh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/WC	0b	**H2RAM EC Semaphore 3 Status (H2RAMECS3S)** This bit is automatically set to 1b while H2RAM EC semaphore 3 is written. 0b: H2RAM EC semaphore 3 is not written. 1b: H2RAM EC semaphore 3 is written. Writing 1 clears this bit.

Bit	R/W	Default	Description
2	R/WC	0b	**H2RAM EC Semaphore 2 Status (H2RAMECS2S)** This bit is automatically set to 1b while H2RAM EC semaphore 2 is written. 0b: H2RAM EC semaphore 2 is not written. 1b: H2RAM EC semaphore 2 is written. Writing 1 clears this bit.
1	R/WC	0b	**H2RAM EC Semaphore 1 Status (H2RAMECS1S)** This bit is automatically set to 1b while H2RAM EC semaphore 1 is written. 0b: H2RAM EC semaphore 1 is not written. 1b: H2RAM EC semaphore 1 is written. Writing 1 clears this bit.
0	R/WC	0b	**H2RAM EC Semaphore 0 Status (H2RAMECS0S)** This bit is automatically set to 1b while H2RAM EC semaphore 0 is written. 0b: H2RAM EC semaphore 0 is not written. 1b: H2RAM EC semaphore 0 is written. Writing 1 clears this bit.

6.3.9.18 H2RAM-HLPC Base Address [31:24] (HLPCRAMBA[31:24])

Index: FCh

Bit	R/W	Default	Description
7-0	R/W	FFh	**H2RAM-HLPC Base Address Bits [31:24] (HLPCRAMBA[31:24])** This field defines EC internal RAM base address on LPC memory space.

6.3.10 Power Management I/F Channel 1 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-18. Host View Register Map via Index-Data I/O, PMC1 Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.10.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.10.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.2 on page 79.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.3.10.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	62h	**Refer to section 6.3.2.3 on page 79.**

6.3.10.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.4 on page 79.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.3.10.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	66h	**Refer to section 6.3.2.5 on page 79.**

6.3.10.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
3-0	R/W	01h	**Refer to section 6.3.2.6 on page 79.**

6.3.10.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-2	R/W	01h	**Refer to section 6.3.2.7 on page 80.**

6.3.11 Power Management I/F Channel 2 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-19. Host View Register Map via Index-Data I/O, PMC2 Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	I/O Port Base Address Bits [15:8] for Descriptor 2 (IOBAD2[15:8])	64h
	I/O Port Base Address Bits [7:0] for Descriptor 2 (IOBAD2[7:0])	65h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	General Purpose Interrupt (GPINTR)	F0h

6.3.11.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.11.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.2 on page 79.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.3.11.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	68h	**Refer to section 6.3.2.3 on page 79.**

6.3.11.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.4 on page 79.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.3.11.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	6Ch	**Refer to section 6.3.2.5 on page 79.**

6.3.11.6 I/O Port Base Address Bits [15:8] for Descriptor 2 (IOBAD2[15:8])

It contains Command/Status Register Base Address Register.

Index: 64h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.4 on page 79.**

6.3.11.7 I/O Port Base Address Bits [7:0] for Descriptor 2 (IOBAD2[7:0])

It contains Command/Status Register Base Address Register.

Index: 65h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.5 on page 79.** Bits 3-0 (IOBAD2[3:0]) are forced to 0000b and can't be written.

6.3.11.8 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.6 on page 79.**

6.3.11.9 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.7 on page 80.**

6.3.11.10 General Purpose Interrupt (GPINTR)

Index: F0h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	W	-	**General Purpose Interrupt 3 (GPINT3)** Writing 1 to this bit will issue an interrupt to INT35.
2	W	-	**General Purpose Interrupt 2 (GPINT2)** Writing 1 to this bit will issue an interrupt to INT34.
1	W	-	**General Purpose Interrupt 1 (GPINT1)** Writing 1 to this bit will issue an interrupt to INT33.
0	W	-	**General Purpose Interrupt 0 (GPINT0)** Writing 1 to this bit will issue an interrupt to INT32.

6.3.12 Power Management I/F Channel 3 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-20. Host View Register Map via Index-Data I/O, PMC3 Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.12.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.12.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.2 on page 79.** Bit 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.3.12.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	6Ah	**Refer to section 6.3.2.3 on page 79.**

6.3.12.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.4 on page 79.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.3.12.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	6Eh	**Refer to section 6.3.2.5 on page 79.**

6.3.12.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.6 on page 79.**

6.3.12.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.7 on page 80.**

6.3.13 Power Management I/F Channel 4 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-21. Host View Register Map via Index-Data I/O, PMC4 Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.13.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.13.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.2 on page 79.** Bit 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.3.13.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	74h	**Refer to section 6.3.2.3 on page 79.**

6.3.13.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.4 on page 79.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.3.13.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	78h	**Refer to section 6.3.2.5 on page 79.**

6.3.13.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.6 on page 79.**

6.3.13.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.7 on page 80.**

6.3.14 Power Management I/F Channel 5 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-22. Host View Register Map via Index-Data I/O, PMC5 Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.14.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.14.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.2 on page 79.** Bit 7-4 (IOBAD0[15:12]) are forced to 0000b and can't be written.

6.3.14.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	7Ah	**Refer to section 6.3.2.3 on page 79.**

6.3.14.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.4 on page 79.** Bits 7-4 (IOBAD1[15:12]) are forced to 0000b and can't be written.

6.3.14.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	7Ch	**Refer to section 6.3.2.5 on page 79.**

6.3.14.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.6 on page 79.**

6.3.14.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.2.7 on page 80.**

6.3.15 Serial Peripheral Interface (SSPI) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-23. Host View Register Map via Index-Data I/O Pair, SSPI Logical Device

	7 … 0	Index
	Register Name	
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h

	7 0	Index
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.15.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.15.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.3.2.2 on page 79.** Bit 7-4 (IOBAD0[15:12]) are forced to 0000b and can't written.

6.3.15.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.3 on page 79.** Bit 1-0 (IOBAD0[1:0]) are forced to 00b and can't be written. It means the base address is on the 4-byte boundary.

6.3.15.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.4 on page 79.**

6.3.15.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.5 on page 79.**

6.3.15.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.6 on page 79.**

6.3.15.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.2.7 on page 80.**

6.3.16 Platform Environment Control Interface (PECI) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-24. Host View Register Map via Index-Data I/O Pair, PECI Interface Logical Device

	Register Name (7 … 0)	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])-Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX) – Unused	70h
	Interrupt Request Type Select (IRQTP) -Unused	71h

6.3.16.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.1 on page 78.**

6.3.16.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.2 on page 79.**

6.3.16.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.2.3 on page 79.** Bits 2-0 (IOBAD0[2:0]) are forced to 000b and can't be written. It means the base address is on the 8-byte boundary.

6.3.16.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.4 on page 79.**

6.3.16.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.5 on page 79.**

6.3.16.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

This register is unused and read-only.

Index: 70h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.6 on page 79.**

6.3.16.7 Interrupt Request Type Select (IRQTP)

This register is unused and read-only.

Index: 71h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.2.7 on page 80.**

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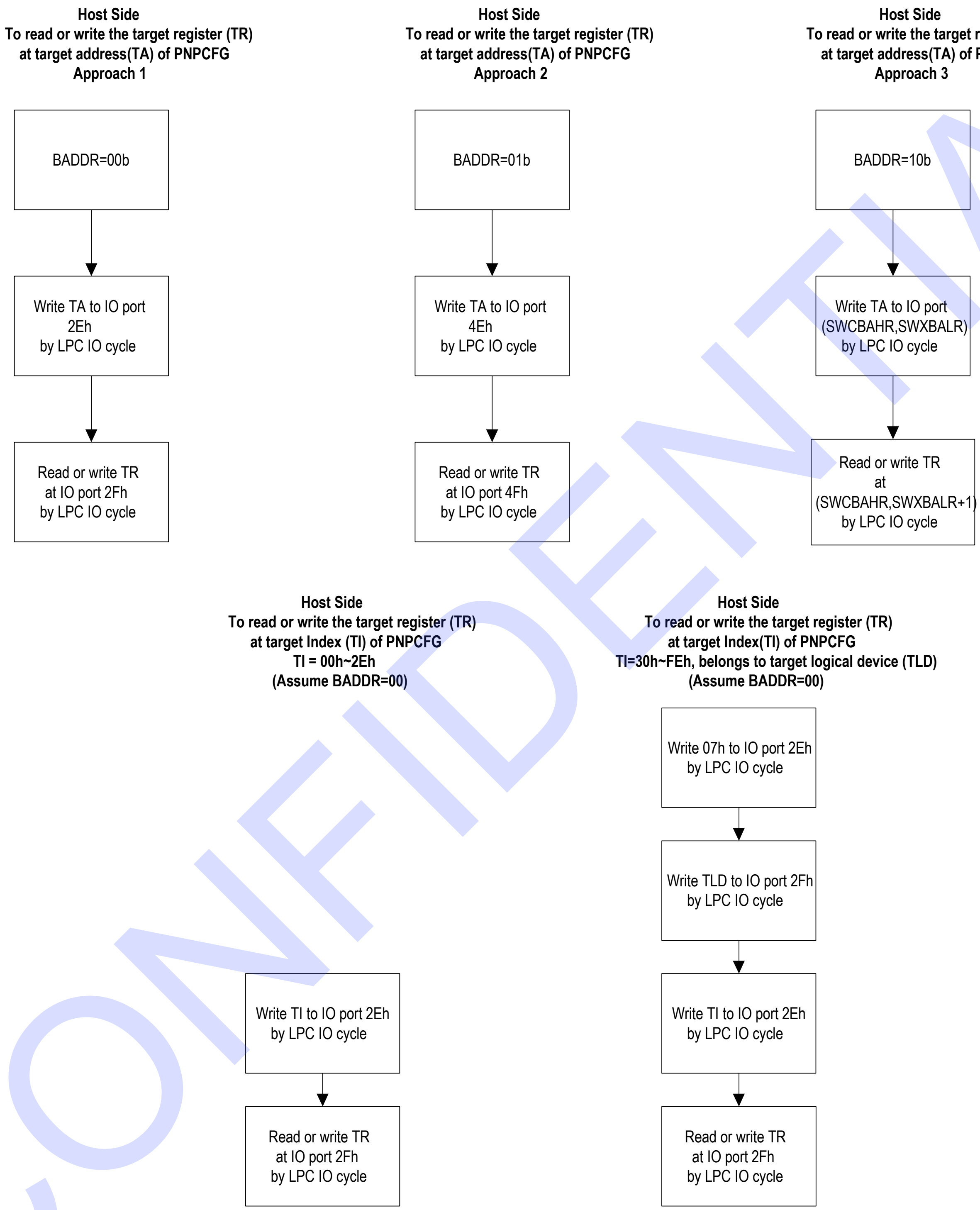
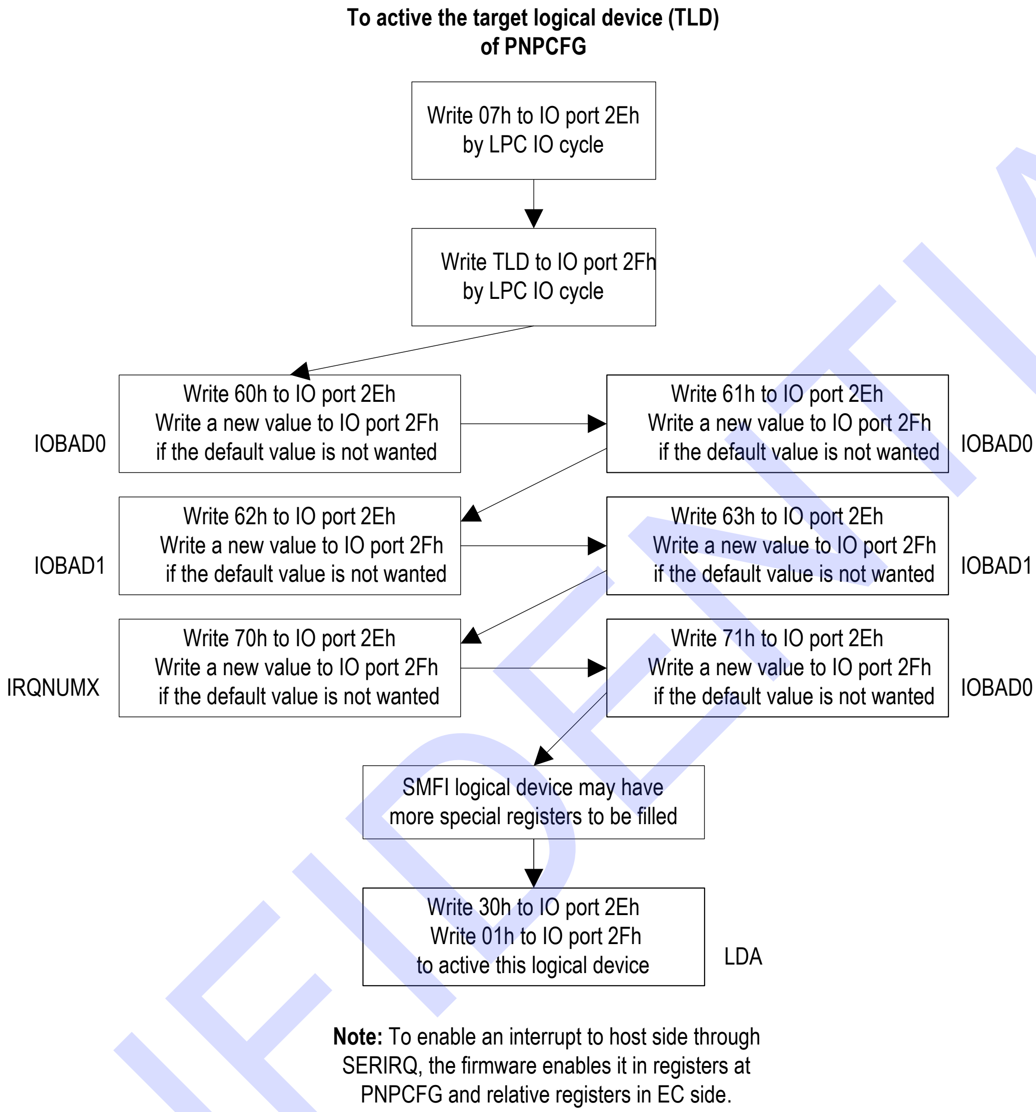


Figure 6-15. Program Flow Chart for PNPCFG



See also section 7.13.5 on page 405 for accessing PNPCFG through EC2I.

6.4 Shared Memory Flash Interface Bridge (SMFI)

6.4.1 Overview

The bridge provides the host to access the shared memory. It also provides EC code address space mapped into the host domain address space, and locking mechanism for read/write protection.

6.4.2 Features

- Behaves as a LPC/FWH memory device (HLPC)
- Supports memory mapping between host domain and EC domain
- Supports read/write(program/erase) flash operations and protection mechanism
- Supports two shared memory access paths: host and EC
- Supports 256KB/512KB e-flash

6.4.3 Function Description

6.4.3.1 Supported Interface

IT81202/SMFI can behave as a LPC/FWH memory device on LPC bus connected to the host Southbridge and this function is abbreviated as HLPC.

6.4.3.2 Supported Flash

256KB/512KB e-flash

6.4.3.3 HLPC: Host Translation

The SMFI provides an HLPC interface between the host bus and the M bus. The flash is mapped into the host memory address space for host accesses. The flash is also mapped into the EC memory address space for EC accesses.

An M bus transaction is generated by the host bus translations and has the following three types:
- 8-bit LPC Memory Read/Write
- 8-bit FWH Read/Write
- 8-bit Host-Indirect Memory Read/Write

After the LPC address translation is done, the host memory transaction is forwarded to M-bus (flash interface) if it is accessing an unprotected region. The host side can't issue a write transaction until the firmware writes 1 to HOSTWA bit SMECCS register.

6.4.3.4 EC-Indirect Memory Read/Write Transaction

The full flash address range can be accessed by the CPU in IT81202.
The firmware code to issue EC-Indirect Memory cycle should be executed within Scratch ROM.
This kind of access is useful to
1. read flash ID for EC BIOS.
2. customize user-defined flash programming interface.
3. put extra BIOS data outside EC 64K.

- **EC-Indirect Memory Address Registers (ECINDAR3-0)**

Stand for flash address bit 31 to 0.

- **EC-Indirect Memory Data Register (ECINDDR)**

Stand for read or write data bit 7 to 0.

- **EC-Indirect Read Mode**

The EC firmware can read the flash byte located at the flash address combined by ECINDAR2-0 from ECINDDR when ECINDAR3 is 00h.

- **EC-Indirect Follow Mode**

For serial flash, another mode to access whole flash is performed by EC-Indirect Follow Mode.

EC-Indirect Follow Mode is enabled after
1. Writing 0Fh to ECINDAR3 register.

EC-Indirect Follow Mode is disabled after
1. Writing 00h to ECINDAR3 register.

In EC-Indirect Follow Mode,
1. Writing 00h to EC-Indirect Memory Address FFFF_FExxh generates FSCE# with high level.
2. Writing data to EC-Indirect Memory Address FFFF_FDxxh generates FSCE# with low level and FMOSI with written data.
3. Reading data from EC-Indirect Memory Address FFFF_FDxxh generates FSCE# with low level and read data from FMISO.
4. All of the above actions are clocked by 8 FSCK clock-ticks and FSCK is stopped in other cases.

6.4.3.5 Flash Shared between Host and EC Domains

A hardware arbiter handles flash read/write translation between the host and EC side.

- **HLPC**

IT81202 bridges the memory cycles on LPC bus and bridges them to the attached SPI flash.
The SMFI internal flash controller performs interleave mechanism control to let the flash fetch for the host and EC side.

It may responde to Long-Waits on LPC bus or freeze the CPU code-fetch due to interleave mechanism.
There is no internal hard-wired mechanism to monitor whether the attached SPI flash is in the WIP (busy) state caused by the WIP instruction from the host.

When the host wants to erase or program the flash via Follow Mode 0, the signaling interface (Semaphore Write or KBC/PMC extended command such as 62h/66h command) notifies the firmware to write 1 to HOSTWA bit in SMECCS register. EC CPU will fail to code fetch due to the WIP (busy) state caused by erasing/programming so Scratch ROM must be applied. Once the host accessing to the flash is completed, the host should indicate this to the EC, allowing EC to clear HOSTWA bit and resume normal operation. The EC can clear HOSTWA bit at any time, and prevent the host from issuing any erase or program operations.

When the host wants to erase or program the flash via Follow Mode 1, it is not necessary for the firmware to shadow code to the SRAM if the EC code is not modified since there is an internal hard-wired mechanism to monitor the WIP (busy) state of the flash. Refer to section 6.4.3.10 HLPC: Serial Flash Programming on page 112 for its description and limitation.

6.4.3.6 Serial Flash Performance Consideration

Clock-tick number spent for each cycle = 8

Clock-tick number spent for branching instruction = M + (4 + N) x 8
M = FSCE# Min High Width = 1 + SCEMINHW
(SCEMINHW field in FLHCTRL2R register

N = 1 if “Fast Read” (SPIFR bit in FLHCTRL1R register)

The selection of these registers depends on the flash specification.
Note that the flash clock frequency is FreqPLL.
(FreqPLL is listed in Table 10-2 on page 570)

Host LPC has very poor read performance on M-bus if HOSTWA bit in SMECCS register is set.

6.4.3.7 Response to a Forbidden Access

A forbidden access is generated by a translated host address which is protected.
HLPC:
The response to the host bus is according to HERES field in SMECCS register.

6.4.3.8 DMA for Scratch SRAM

Static DMA program flow:

1. Select Direct-map SRAM used in this Static DMA by program register STCDMACR bit4-bit1.
2. Set the logic memory address in eflash by programing the register SCAR0~12 bit19-bit0. Which register among SCAR0~12 is selected by program is according to the value set in register STCDMACR bit4-bit1, i.e. if STCDMACR[4:1] == 10, select register SCAR10[19:0] to set the logic memory address in eflash.
3. Start Static DMA by setting register STCDMACR[0] = 1.
4. Wait for Static DMA to finish according to STCDMACR[0] = 0.
5. Validate Direct-map SRAM function by programing register SCAR0~12 bit20=0. The flow is the same as that of step 2. Which register among SCAR0~12 will be selected to set is according to the register value in STCDMACR bit4-bit1, i.e. if STCDMACR[4:1] == 10, set register SCAR10[20]=0 to validate Direct-map SRAM function.
6. Call the function which has been moved to the Direct-map SRAM.

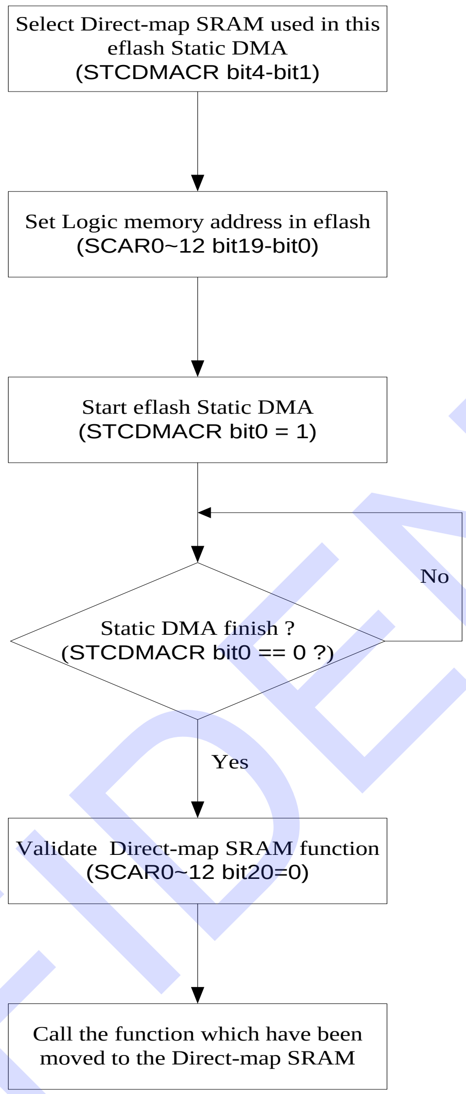
Note:
The Static DMA program flow must be executed by calling the ROM API. The following is the example to how the ROM API will be used.

If the user wants to set “STCDMACR[4:1] == 10” and “SCAR10[19:0] = 0x1000”, the Static DMA program flow by calling the ROM API is as the following:

```
eflash_to_direct_map(0x1000,10);
dm_set_segment_valid(10);
```

The Static DMA program flow is finished after calling these two ROM API and then the user can call the function to be run in the Direct-map SRAM.

Figure 6-16. Program Flow Chart of DMA for Scratch SRAM



6.4.3.9 HLPC: Flash Programming via Host LPC Interface with Scratch SRAM

When programming flash via HLPC Follow Mode 0 is processing, the flash will be busy and code fetch from flash by the CPU and will be invalid and cause CPU to fail to execute instructions. It means the firmware must copy necessary instructions from code space to Scratch SRAM, enable mapping Scratch SRAM to Scratch ROM, and jump to Scratch ROM before programming flash.

Flash Programming Steps:
(a) The host side communicates with the EC side via KBC/PMC extended or semaphore registers
(b) EC side: Write 1 to HOSTWA bit in SMECCS register
(c) EC side: Copy necessary code to Scratch RAM
(d) EC side: Enable code space mapping of Scratch SRAM
(e) EC side: Make the host processor enter SMM mode if necessary
(f) EC side: Jump instruction to Scratch ROM
(g) Host side: Set related memory-write registers in South-Bridge
(h) Host side: Start flash programming
(i) End flash programming and reset EC domain if necessary.

(Refer to section 5.4 on page 25)
Note: Do not let EC enter Doze/Deep Doze/Sleep mode while processing flash programming flow.

6.4.3.10 HLPC: Serial Flash Programming

There is Follow Mode dedicated for serial flash programming through host LPC interface.

There are mode 0 and 1 for Follow Mode and they can not be enabled at the same time.

In mode 0, there is no internal hard-wired mechanism to monitor the WIP (busy) state of the flash.
In mode 1, there is an internal hard-wired mechanism to monitor the WIP (busy) state of the flash; however, the utility in the host side is still required to poll the flash status via RDSR instruction.

In mode 0, it's necessay for the firmware to shadow code to the SRAM and stop all flash access to let the HLPC occupy the flash arbiter.
In mode 1, it's not necessay for the firmware to shadow code to the SRAM and HLPC interleaves with other flash access issued by the firmware.

In mode 0, if the hardware protection is disabled, the program in the host side can construct any SPI cycle.
In mode 0, if the hardware protection is enabled, the WIP instructions listed in Table 6-25 are monitored by protection logic.

Table 6-25. SPI Instruction List Monitored by HLPC Follow Mode 0, Protection Enabled

Instruction	Hex Code	Note
Program Data (PROG)	02h	Monitored by protection logic.
AAI Program Byte (AAIB/AAI)	AFh	Monitored by protection logic.
AAI Program Word (AAIW/AAI)	ADh	Monitored by protection logic.
Chip/Bulk Erase (ERASE)	60h,C7h	Inhibited by protection logic.
Sector/Block Erase (ERASE)	20h,52h,D7h,D8h	Monitored by protection logic.
Otherwise	-	Not monitored by protection logic.

In mode 1, only some specified instructions are supported.
If the leading two bytes of JEDEC ID of flash is "BFh 25h","50h 01h" will be sent to the flash before bridging a WIP instruction.

Table 6-26. SPI Instruction List Supported by HLPC Follow Mode 1

Instruction	Hex Code	Note
Program Data (PROG)	02h	Monitored by protection logic. Programming single byte supported. Programming multiple bytes isn't supported.
Read Status (RDSR)	05h	Monitored by protection logic. Reading single status byte supported. Reading multiple status bytes isn't supported.
Chip/Bulk Erase (ERASE)	60h,C7h	Not supported
Sector/Block Erase (ERASE)	20h,52h,D7h,D8h	Monitored by protection logic. Supported
Otherwise	-	Not supported

Follow Mode 0 is enabled after
1. Writing 1 to HOSTWA bit in SMECCS register in the EC side.
2. Writing 00h to LPC/FWH Address FFFF_FExxh in the host side

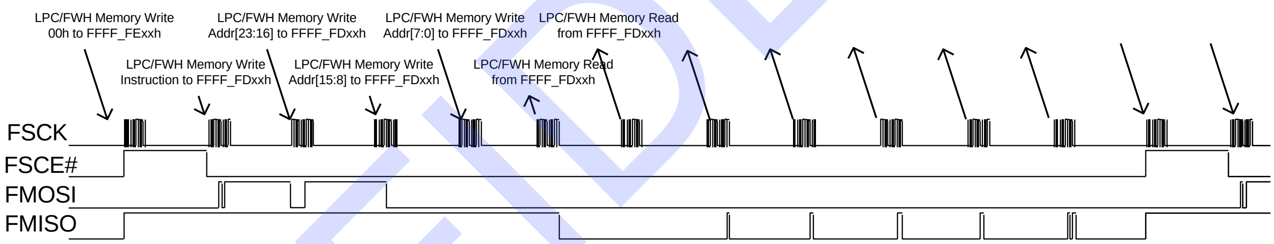
Follow Mode 0 is disabled after
1. Writing 0 to HOSTWA bit in SMECCS register in the EC side.

Follow Mode 1 is enabled after
1. Writing 1 to HFW1EN bit in HCTRL2R register in the EC side.
2. Writing 00h to LPC/FWH Address FFFF_FExxh in the host side
3. Write 1 to ACP80 bit in SPCTRL1 register to enable LPC_IO-to-FSPI function.

Follow Mode 1 is disabled after
1. Writing 0 to HFW1EN bit in HCTRL2R register in the EC side.

In HLPC Follow Mode,
1. Writing 00h to LPC/FWH Memory Address FFFF_FExxh generates FSCE# with high level.
2. Writing data to LPC/FWH Memory Address FFFF_FDxxh generates FSCE# with low level and FMOSI with written data.
3. Reading data from LPC/FWH Memory Address FFFF_FDxxh generates FSCE# with low level and read data from FMISO.
4. All the above actions are clocked by 8 FSCK clock ticks and FSCK is stopped in other cases.

Figure 6-17. HLPC Follow Mode for Serial Flash (e.g. Fast Read Instruction)

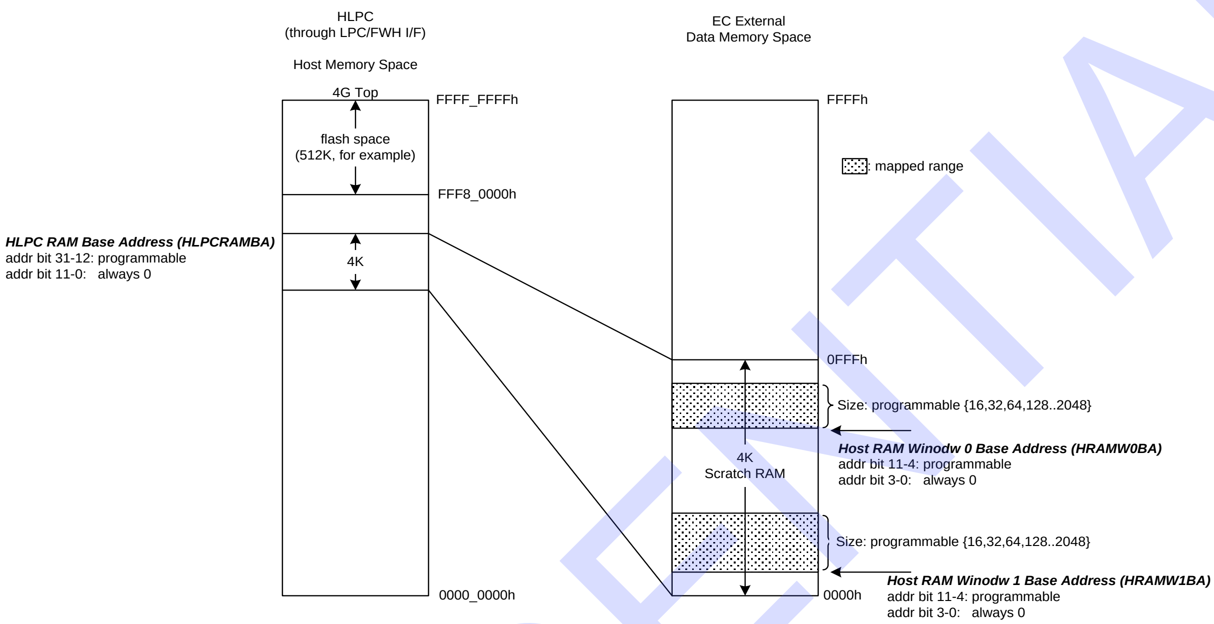


6.4.3.11 Host Side to EC Scratch RAM (H2RAM)

6.4.3.11.1 HLPC to EC Scratch RAM (H2RAM-HLPC) through LPC Memory/FWH Cycles

- H2RAM can be used by the host side software to access Scratch RAM through LPC Memory/FWH cycles.
- The read/write protection mechanism is also supported by this function.
- H2RAM isn't available through Host-Indirect Memory path.

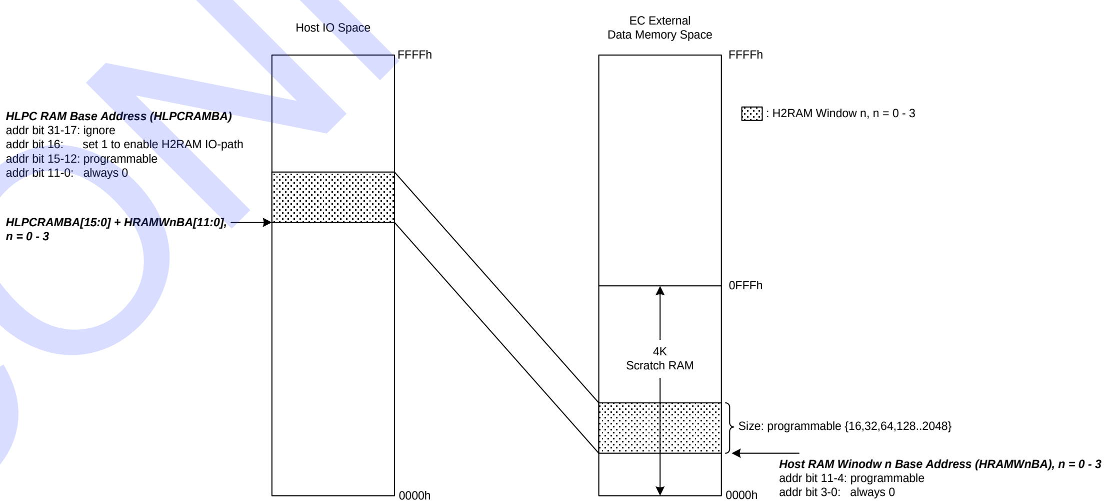
Figure 6-18. H2RAM-HLPC Mapping through LPC Memory/FWH Cycles



6.4.3.11.2 HLPC to EC Scratch RAM (H2RAM-HLPC) through LPC IO Cycles

- H2RAM also can be used in translating some addresses from the host IO space to Scratch RAM space.
- The read/write protection mechanism is also supported by this function.

Figure 6-19. H2RAM-HLPC Mapping through LPC IO Cycles



6.4.3.11.3 H2RAM EC/Host Semaphore

A LPC Memory/FWH/IO Write cycle targeted on H2RAM host semaphore will produce an interrupt (INT83) to inform EC and a Data-Write instruction executed on H2RAM EC semaphore also generates an IRQ to the host. Through these semaphores, the host and EC can communicate with each other during H2RAM data transfer.

Figure 6-20. H2RAM EC/Host Semaphore Interrupt through LPC Memory/FWH Cycles

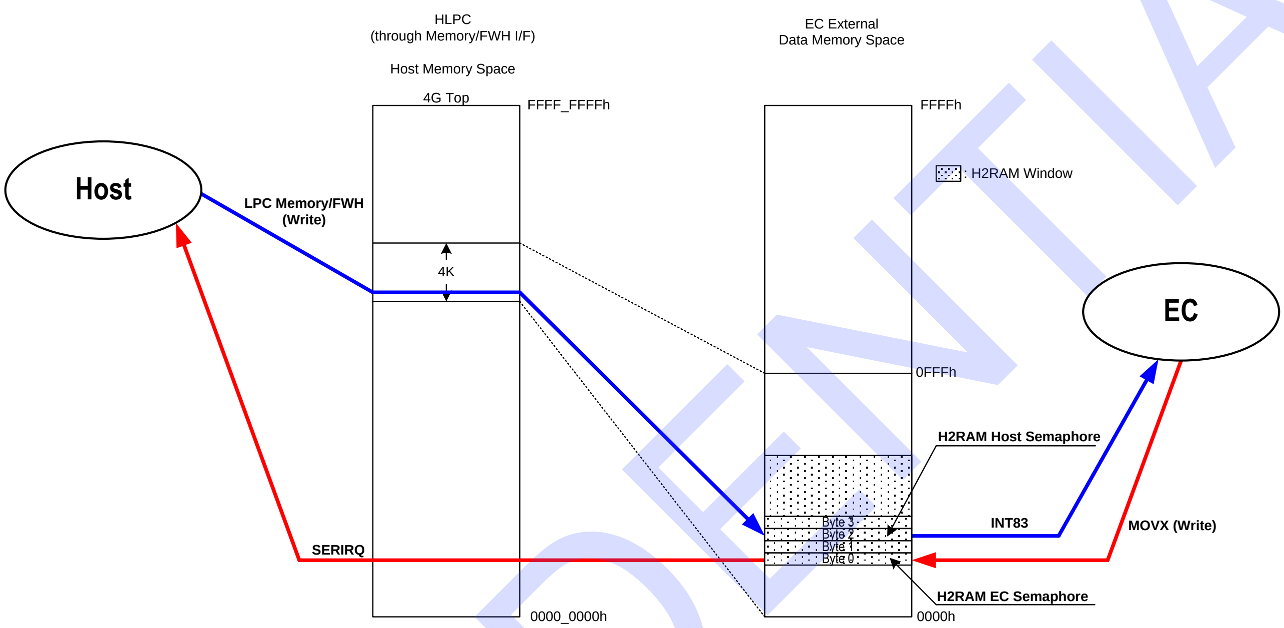
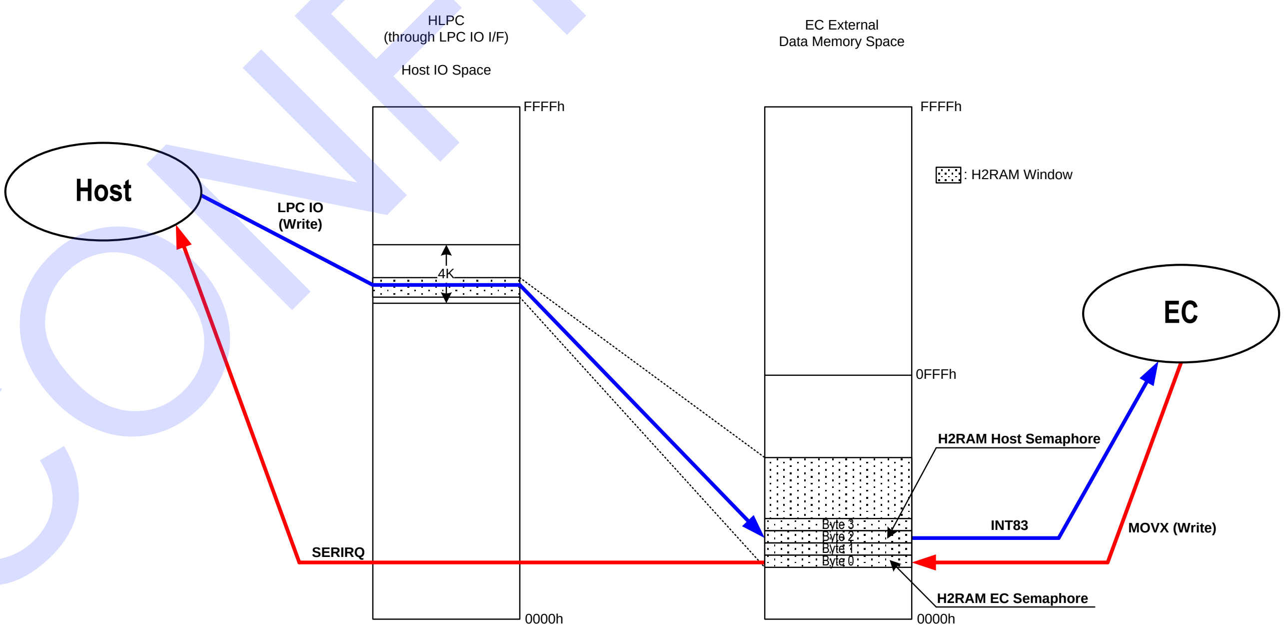


Figure 6-21. H2RAM EC/Host Semaphore Interrupt through LPC IO Cycles



6.4.3.12 E-flash Power-on Detection

6.4.3.12.1 16B-signature and Implicit/Explicit EC Code Base Address

A specific 16B-signature is used to locate the EC code base address.

1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th
A5h	A5h	A5h	A5h	A5h	A5h	A5h	flag	85h	12h	5Ah	5Ah	AAh	AAh	55h	55h

All content of the 16 bytes must match the content in the table.
Note: Add 16-bytes signature in F/W (strongly recommented)

8th byte's bit 7:
It must be 1b.
8th byte's bit 6:
0b: Disable
1b: Suspend internal-to-external clock switching request.
When this bit is set, the internal clock would act as a temporary clock to enable EC to configure some GPIO setting before the external crystal is ready to work.
This bit is available only when the 8th byte's bit 4 is 0.
Refer to section 7.7.3.6 on page 264.
8th byte's bit 5:
It must be 1b.
8th byte's bit 4:
It must be 1b.
8th byte's bit 3:
It must be 0b.
8th byte's bit 2:
It must be 1b.
8th byte's bit 1:
It must be 0b.
8th byte's bit 0:
It must be 0b.

1st byte must be located at 16-byte boundary.
For example, let the address of 1st byte be ADDR1[23:0], then ADDR1[3:0] must be 0000b.

The 1st byte must be located at the address 40h, 50h, 60h, …F0h offset to the EC code base. For example, let the address of 1st byte be ADDR1[23:0], then ADDR1[7:0] must be 40h, 50h, 60h…F0h (interval 10h) and the EC code base is loated at (ADDR1[23:12] * 2^12).

6.4.3.12.2 Detection Sequence

Table 6-27. Corresponding Table of SPI Flash Power-on Detection

	Scanned Address or Scanned Range	Contents	If content is matched, EC code base address wil be at	Note
(a)	[addr 0040h], [addr 0050h], [addr 0060h], … [addr 00F0h]	16B-signature with implicit format.	000000h	Use implicit format.

6.4.4 EC Interface Registers

The registers of SMFI can be divided into two parts, Host Interface Registers and EC Interface Registers and this section lists the EC interface. The EC interface can only be accessed by the internal processor. The base address for SMFI is 1000h.

These registers are listed below.

Table 6-28. EC View Register Map, SMFI

7 0	Offset
FBIU Configuration (FBCFG)	00h
Flash Programming Configuration Register (FPCFG)	01h
Shared Memory EC Control and Status Register (SMECCS)	20h
Shared Memory Host Semaphore (SMHSR)	22h
Flash Control Register 1 (FLHCTRL1R)	31h
Flash Control Register 2 (FLHCTRL2R)	32h
Host Control 2 Register (HCTRL2R)	36h
EC-Indirect Memory Address Register 0 (ECINDAR0)	3Bh
EC-Indirect Memory Address Register 1 (ECINDAR1)	3Ch
EC-Indirect Memory Address Register 2 (ECINDAR2)	3Dh
EC-Indirect Memory Address Register 3 (ECINDAR3)	3Eh
EC-Indirect Memory Data Register (ECINDDR)	3Fh
Scratch SRAM 0 Address Low Byte Register (SCAR0L)	40h
Scratch SRAM 0 Address Middle Byte Register (SCAR0M)	41h
Scratch SRAM 0 Address High Byte Register (SCAR0H)	42h
Scratch SRAM 1 Address Low Byte Register (SCAR1L)	43h
Scratch SRAM 1 Address Middle Byte Register (SCAR1M)	44h
Scratch SRAM 1 Address High Byte Register (SCAR1H)	45h
Scratch SRAM 2 Address Low Byte Register (SCAR2L)	46h
Scratch SRAM 2 Address Middle Byte Register (SCAR2M)	47h
Scratch SRAM 2 Address High Byte Register (SCAR2H)	48h
Scratch SRAM 3 Address Low Byte Register (SCAR3L)	49h
Scratch SRAM 3 Address Middle Byte Register (SCAR3M)	4Ah
Scratch SRAM 3 Address High Byte Register (SCAR3H)	4Bh
Scratch SRAM 4 Address Low Byte Register (SCAR4L)	4Ch
Scratch SRAM 4 Address Middle Byte Register (SCAR4M)	4Dh
Scratch SRAM 4 Address High Byte Register (SCAR4H)	4Eh
Deferred SPI Instruction (DSINST)	55h
Deferred SPI Address 15-12 (DSADR1)	56h
Deferred SPI Address 23-16 (DSADR2)	57h
Flash Control Register 3 (FLHCTRL3R)	63h
Flash Control 5 Register (FLHCTRL5R)	A3h

7 0	Offset
Flash Control 6 Register (FLHCTRL6R)	A2h
Host Instruction Control 2 (HINSTC2)	59h
Host RAM Window Control (HRAMWC)	5Ah
Host RAM Window 0 Base Address (HRAMW0BA[11:4])	5Bh
Host RAM Window 1 Base Address (HRAMW1BA[11:4])	5Ch
Host RAM Window 0 Access Allow Size (HRAMW0AAS)	5Dh
Host RAM Window 1 Access Allow Size (HRAMW1AAS)	5Eh
Host RAM Window 2 Base Address (HRAMW2BA[11:4])	76h
Host RAM Window 3 Base Address (HRAMW3BA[11:4])	77h
Host RAM Window 2 Access Allow Size (HRAMW2AAS)	78h
Host RAM Window 3 Access Allow Size (HRAMW3AAS)	79h
H2RAM EC Semaphore Interrupt Enable (H2RAMECSIE)	7Ah
H2RAM EC Semaphore Address (H2RAMECSA)	7Bh
H2RAM Host Semaphore Status (H2RAMHSS)	7Ch
Static DMA Control Register (STCDMACR)	80h
Scratch SRAM 5 Address Low Byte Register (SCAR5L)	81h
Scratch SRAM 5 Address Middle Byte Register (SCAR5M)	82h
Scratch SRAM 5 Address High Byte Register (SCAR5H)	83h
Scratch SRAM 6 Address Low Byte Register (SCAR6L)	84h
Scratch SRAM 6 Address Middle Byte Register (SCAR6M)	85h
Scratch SRAM 6 Address High Byte Register (SCAR6H)	86h
Scratch SRAM 7 Address Low Byte Register (SCAR7L)	87h
Scratch SRAM 7 Address Middle Byte Register (SCAR7M)	88h
Scratch SRAM 7 Address High Byte Register (SCAR7H)	89h
Scratch SRAM 8 Address Low Byte Register (SCAR8L)	8Ah
Scratch SRAM 8 Address Middle Byte Register (SCAR8M)	8Bh
Scratch SRAM 8 Address High Byte Register (SCAR8H)	8Ch
Scratch SRAM 9 Address Low Byte Register (SCAR9L)	8Dh
Scratch SRAM 9 Address Middle Byte Register (SCAR9M)	8Eh
Scratch SRAM 9 Address High Byte Register (SCAR9H)	8Fh
Scratch SRAM 10 Address Low Byte Register (SCAR10L)	90h
Scratch SRAM 10 Address Middle Byte Register (SCAR10M)	91h
Scratch SRAM 10 Address High Byte Register (SCAR10H)	92h
Scratch SRAM 11 Address Low Byte Register (SCAR11L)	93h
Scratch SRAM 11 Address Middle Byte Register (SCAR11M)	94h
Scratch SRAM 11 Address High Byte Register (SCAR11H)	95h
Scratch SRAM 12 Address Low Byte Register (SCAR12L)	96h
Scratch SRAM 12 Address Middle Byte Register (SCAR12M)	97h
Scratch SRAM 12 Address High Byte Register (SCAR12H)	98h
ROM Address Low Byte Register (ROMARL)	99h
ROM Address Middle Byte Register (ROMARM)	9Ah
ROM Address High Byte Register (ROMARH)	9Bh
SPI Extend Mode Base Address Low Byte Register (SEMBARL)	9Ch
SPI Extend Mode Base Address Middle Byte Register (SEMBARM)	9Dh
SPI Extend Mode Base Address High Byte Register (SEMBARH)	9Eh
Scratch SRAM 13 Address Low Byte Register (SCAR13L)	B0h
Scratch SRAM 13 Address Middle Byte Register (SCAR13M)	B1h
Scratch SRAM 13 Address High Byte Register (SCAR13H)	B2h
Scratch SRAM 14 Address Low Byte Register (SCAR14L)	B3h
Scratch SRAM 14 Address Middle Byte Register (SCAR14M)	B4h
Scratch SRAM 14 Address High Byte Register (SCAR14H)	B5h
Scratch SRAM 15 Address Low Byte Register (SCAR15L)	B6h
Scratch SRAM 15 Address Middle Byte Register (SCAR15M)	B7h

7	0	Offset
Scratch SRAM 15 Address High Byte Register (SCAR15H)		B8h
Scratch SRAM 16 Address Low Byte Register (SCAR16L)		B9h
Scratch SRAM 16 Address Middle Byte Register (SCAR16M)		BAh
Scratch SRAM 16 Address High Byte Register (SCAR16H)		BBh
Scratch SRAM 17 Address Low Byte Register (SCAR17L)		BCh
Scratch SRAM 17 Address Middle Byte Register (SCAR17M)		BDh
Scratch SRAM 17 Address High Byte Register (SCAR17H)		BEh
Scratch SRAM 18 Address Low Byte Register (SCAR18L)		BFh
Scratch SRAM 18 Address Middle Byte Register (SCAR18M)		C0h
Scratch SRAM 18 Address High Byte Register (SCAR18H)		C1h
Scratch SRAM 19 Address Low Byte Register (SCAR19L)		C2h
Scratch SRAM 19 Address Middle Byte Register (SCAR19M)		C3h
Scratch SRAM 19 Address High Byte Register (SCAR19H)		C4h
Scratch SRAM 20 Address Low Byte Register (SCAR20L)		C5h
Scratch SRAM 20 Address Middle Byte Register (SCAR20M)		C6h
Scratch SRAM 20 Address High Byte Register (SCAR20H)		C7h
Scratch SRAM 21 Address Low Byte Register (SCAR21L)		C8h
Scratch SRAM 21 Address Middle Byte Register (SCAR21M)		C9h
Scratch SRAM 21 Address High Byte Register (SCAR21H)		CAh
Scratch SRAM 22 Address Low Byte Register (SCAR22L)		CBh
Scratch SRAM 22 Address Middle Byte Register (SCAR22M)		CCh
Scratch SRAM 22 Address High Byte Register (SCAR22H)		CDh
Scratch SRAM 23 Address Low Byte Register (SCAR23L)		CEh
Scratch SRAM 23 Address Middle Byte Register (SCAR23M)		CFh
Scratch SRAM 23 Address High Byte Register (SCAR23H)		D0h

6.4.4.1 FBIU Configuration Register (FBCFG)

The FBIU (Flash Bus Interface Unit) directly interfaces with the flash device. The FBIU also defines the access time to the flash base address from 00_0000h to 3F_FFFFh (4M bytes).

Address Offset: 00h

Bit	R/W	Default	Description
7	-	0b	**Scratch SRAM Map Control (SSMC)** 0: Normal 1: Scratch SRAM No. 0, whose size is 2K bytes, is mapped into F800h-FFFFh in code space and overrides the settings in SCAR0H/SCAR0M/SCAR0L register. This bit is OBSOLETE and is only used to be compatible with old IT8510 firmware and should not be used in new firmware. Note that the following is the definition of this register field in IT8510. 0: Scratch RAM (data space). 1: Scratch ROM (code space).
6-0	-	-	**Reserved**

6.4.4.2 Flash Programming Configuration Register (FPCFG)

This register provides general control on banking and flash standby.

Address Offset: 01h

Bit	R/W	Default	Description
7	R/W	1b	**Reserved**
6	R/W	Serial flash: 0b	**Auto Flash Standby (AFSTBY)** Serial flash: 1: Stop flash access in Doze/Deep Doze/Sleep mode and issue “Deep Power Down (B9h)” instruction before entering Sleep mode and issue “Release Deep Power Down (ABh)” instruction after waking up from Sleep mode. 0: Prevent the flash from entering the standby mode.
5	R/W	1b	**Reserved**
4	-	-	**Reserved**
3-0	R/W	1111b	**Reserved**

6.4.4.3 Shared Memory EC Control and Status Register (SMECCS)

The following set of registers is accessible only by the EC. The registers are applied to VSTBY.
This register provides the flash control and status of a restricted access.

Address Offset: 20h

Bit	R/W	Default	Description
7	R/W	0b	**Host Semaphore Interrupt Enable (HSEMIE)** It enables interrupt to CPU via INT22 of INTC. 0: Disable the host semaphore (write) interrupt to the EC. 1: The interrupt is set (level high) if HSEMW bit is set.
6	R/WC	0b	**Host Semaphore Write (HSEMW)** 0: Host has not written data to HSEM3-0 field in SMHSR register. 1: Host has written data to HSEM3-0 field in SMHSR register. Writing 1 to this bit to clear itself and clear internal detect logic. Writing 0 has no effect.

Bit	R/W	Default	Description
5	R/W	0b	**Host Write Allow (HOSTWA)** This bit is for HLPC only. 0: The SMFI does not generate write transactions on M-bus. 1: The SMFI can generate write transactions on M-bus. The read performance on M-bus will be very poor for Host LPC if write transaction is allowed.
4-3	R	01b	**Host Error Response (HERES)** These bits control response types on read/write translation from/to a protected address. 01b: Read back FFh; ignoring write Otherwise: Reserved
2-0	-	-	**Reserved**

6.4.4.4 Shared Memory Host Semaphore Register (SMHSR)

This register provides eight semaphore bits between the EC and the host. Bits 3-0 may be set by the host and Bits 7-4 may be set by the EC. The register is reset on host domain hardware reset.
This register is the same as the one in section 6.4.5.6 but they are in different views.

Address Offset: 22h

Bit	R/W	Default	Description
7-4	R/W	0h	**EC Semaphore (CSEM3-0)** These four bits may be written data by the EC and read by both the host and the EC
3-0	R	0h	**Host Semaphore (HSEM3-0)** These four bits may be written data by the host and read by both the host and the EC.

6.4.4.5 Flash Control 1 Register (FLHCTRL1R)

Address Offset: 31h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	001b	**SPI Flash Read Mode (SPIFR)** For serial flash: 100b: Uses “Quad Read Input/Output (QIOFR)” cycle (instruction = EBh) 011b: Uses “Fast Read Dual Input/Output (DIOFR)” cycle (instruction = BBh) 010b: Uses “Fast Read Dual Output (DOFR)” cycle (instruction = 3Bh) 001b: Uses “Fast Read (FREAD)” cycle (instruction = 0Bh) 000b: Uses “Read” cycle (instruction = 03h) The performance of “Read” cycle is better than “Fast Read” cycle in the same frequency since “Fast Read” cycle request 8 dummy clock ticks in each cycle. The attached must support “Fast Read” cycle since it’s the default read instruction to serial flash. Instruction A3h of SPI flash isn’t supported. A few flash types can not achieve their documented frequencies without issuing this instruction.
3	R/W	1b	**Serial Wait 1T (LFSW1T)** For serial flash: Always write 1 to it.

Bit	R/W	Default	Description
2-0	-	-	**Reserved**

6.4.4.6 Flash Control 2 Register (FLHCTRL2R)

For serial flash only.

Address Offset: 32h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-4	R/W	00b	**FSCE# Min Read High Width (SCEMINRHW)** 00b: Disabled 01b: Reserved 10b: 1.5T 11b: Reserved It is similar to SCEMINHW; however, it only applies to the width after all read instructions and overrides SCEMINHW.
3	-	-	**Reserved**
2-0	R/W	011b	**FSCE# Min High Width (SCEMINHW)** 000b: Reserved 001b: 1.5T 010b: 2.5T 011b: 3.5T 100b: 4.5T 101b: 5.5T 110b: 6.5T It depends on the "FSCE# High Time" on flash specification. The smaller the value, the better the performance. This register may needs to be modified before the PLL frequency is changed.

6.4.4.7 Host Control 2 Register (HCTRL2R)

Address Offset: 36h

Bit	R/W	Default	Description
7	R/W	1b	**Host Bridge Enable (HBREN)** 1: The host memory cycle is decoded 0: Otherwise This bit can be modified only before VCC power is supplied.
6	-	-	**Reserved**
5	R/W	0b	**HLPC Follow Mode 1 Enable (HFW1EN)** 1: Enable HLPC Follow Mode 1 if HOSTWA bit in SMECCS register isn't set. 0: Otherwise This bit can be modified only before VCC power is supplied.
4-0	-	-	**Reserved**

6.4.4.8 EC-Indirect Memory Address Register 0 (ECINDAR0)

Address Offset: 3Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**EC-Indirect Memory Address (ECINDA7-0)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.4.4.9 EC-Indirect Memory Address Register 1 (ECINDAR1)

Address Offset: 3Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**EC-Indirect Memory Address (ECINDA15-8)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.4.4.10 EC-Indirect Memory Address Register 2 (ECINDAR2)

Address Offset: 3Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**EC-Indirect Memory Address (ECINDA23-16)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.4.4.11 EC-Indirect Memory Address Register 3 (ECINDAR3)

Address Offset: 3Eh

Bit	R/W	Default	Description
7-6	W	-	**EC-Indirect Memory Address (ECINDA31-30)** 00b/11b: Select SPI 01b: Select e-flash 10b: Reserved
5-4	R	00b	**EC-Indirect Memory Address (ECINDA29-28)** Read only.
3-0	R/W	0h	**EC-Indirect Memory Address (ECINDA27-24)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.4.4.12 EC-Indirect Memory Data Register (ECINDDR)

Address Offset: 3Fh

Bit	R/W	Default	Description
7-0	R/W	-	**EC-Indirect Memory Data (ECINDD7-0)** Read/Write to this register will access one byte on the flash with the 32-bit flash address defined in ECINDAR3-0.

6.4.4.13 Scratch SRAM 0 Address Low Byte Register (SCAR0L)

Address Offset: 40h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 0 Address (SC0A7-0)**

6.4.4.14 Scratch SRAM 0 Address Middle Byte Register (SCAR0M)

Address Offset: 41h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 0 Address (SC0A15-8)**

6.4.4.15 Scratch SRAM 0 Address High Byte Register (SCAR0H)

Address Offset: 42h

Bit	R/W	Default	Description
7	R/W	0b	**Scratch SRAM 0 Address (SC0A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 0 Address (SC0A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.16 Scratch SRAM 1 Address Low Byte Register (SCAR1L)

Address Offset: 43h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 1 Address (SC1A7-0)**

6.4.4.17 Scratch SRAM 1 Address Middle Byte Register (SCAR1M)

Address Offset: 44h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 1 Address (SC1A15-8)**

6.4.4.18 Scratch SRAM 1 Address High Byte Register (SCAR1H)

Address Offset: 45h

Bit	R/W	Default	Description
7	R/W	0b	**Scratch SRAM 1 Address (SC1A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 1 Address (SC1A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.19 Scratch SRAM 2 Address Low Byte Register (SCAR2L)

Address Offset: 46h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 2 Address (SC2A7-0)**

6.4.4.20 Scratch SRAM 2 Address Middle Byte Register (SCAR2M)

Address Offset: 47h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 2 Address (SC2A15-8)**

6.4.4.21 Scratch SRAM 2 Address High Byte Register (SCAR2H)

Address Offset: 48h

Bit	R/W	Default	Description
7	R/W	0b	**Scratch SRAM 2 Address (SC2A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 2 Address (SC2A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.22 Scratch SRAM 3 Address Low Byte Register (SCAR3L)

Address Offset: 49h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 3 Address (SC3A7-0)**

6.4.4.23 Scratch SRAM 3 Address Middle Byte Register (SCAR3M)

Address Offset: 4Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 3 Address (SC3A15-8)**

6.4.4.24 Scratch SRAM 3 Address High Byte Register (SCAR3H)

Address Offset: 4Bh

Bit	R/W	Default	Description
7	R/W	0b	**Scratch SRAM 3 Address (SC3A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 3 Address (SC3A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.25 Scratch SRAM 4 Address Low Byte Register (SCAR4L)

Address Offset: 4Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 4 Address (SC4A7-0)**

6.4.4.26 Scratch SRAM 4 Address Middle Byte Register (SCAR4M)

Address Offset: 4Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 4 Address (SC4A15-8)**

6.4.4.27 Scratch SRAM 4 Address High Byte Register (SCAR4H)

Address Offset: 4Eh

Bit	R/W	Default	Description
7	R/W	0b	**Scratch SRAM 4 Address (SC4A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 4 Address (SC4A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.28 Deferred SPI Instruction (DSINST)

For SPI flash only.

Address Offset: 55h

Bit	R/W	Default	Description
7-0	R	-	**Deferred SPI Instruction (DSINST)** The 8-bit instruction code of deferred SPI WIP instruction.

6.4.4.29 Deferred SPI Address 15-12 (DSADR1)

For SPI flash only.

Address Offset: 56h

Bit	R/W	Default	Description
7-4	R	-	**Deferred SPI Address 15-12 (DSA15-12)** The SPI address of deferred SPI WIP instruction.
3-0	-	-	**Reserved**

6.4.4.30 Deferred SPI Address 23-16 (DSADR2)

Address Offset: 57h

Bit	R/W	Default	Description
7-0	R	-	**Deferred SPI Address 23-16 (DSA23-16)** The SPI address of deferred SPI WIP instruction.

6.4.4.31 Host Instruction Control 2 (HINSTC2)

This register is only valid when LPC hardware protection is enabled by setting P0ZR and P1ZR register.

Some SPI flashes provide two or more sector/block ERASE instructions, e.g. 4K and 64K ERASE instruction. If one specified 4K block is set as hardware protection, it may be erased by 64K ERASE instruction.

To accomplish the hardware protectin on the SPI flash, the size defined in P0Z/P1Z field in P0ZR/P1ZR register must be equal to or greater than the allowed sector/block size of ERASE instruction.

For the above example, if an SPI flash provides the 4K ERASE instruction (code 20h) and 64K ERASE instruction (code D8h), the write protection can work well if the size defined in P0Z/P1Z field is equal to or greater than 64K; otherwise, the 64K ERASE instruction should be inhibited by setting the DISEID8 bit.

Address Offset: 59h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**Host Indirect Cycle Target Select (HICTS)** 0b: SPI flash 1b: e-flash
4	R/W	0b	**LPC Memory Cycle Target Select (LMCTS)** 0b: SPI flash 1b: e-flash
3	R/W	0b	**Disable Erase Instruction D8h (DISEID8)** (For SPI flash only) Erasing sector/block instruction D8h will be inhibited.
2	R/W	0b	**Disable Erase Instruction D7h (DISEID7)** (For SPI flash only) Erasing sector/block instruction D7h will be inhibited.
1	R/W	0b	**Disable Erase Instruction 52h (DISEI52)** (For SPI flash only) Erasing sector/block instruction 52h will be inhibited.
0	R/W	0b	**Disable Erase Instruction 20h (DISEI20)** (For SPI flash only) Erasing sector/block instruction 20h will be inhibited.

6.4.4.32 Flash Control Register 3 (FLHCTRL3R)

Address Offset: 63h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**SPI Flash I/F Enable (SIFE)** 0b: Disable 1b: Enable
2-1	-	-	**Reserved**
0	R/W	0b	**Force FSPI I/F Tri-state (FFSPITRI)** 1: FSCK/FSCE#/FMISO/FMOSI are tri-state. 0: FSCK/FSCE#/FMISO/FMOSI are normal operation.

6.4.4.33 Host RAM Window Control (HRAMWC)

Address Offset: 5Ah

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**H2RAM Path Select (H2RAMPS)** 0b: H2RAM through LPC Memory/FWH cycle. 1b: H2RAM through LPC IO cycle.
3	R/W	0b	**H2RAM Window 3 Enable (H2RAMW3E)** 0b: Disable 1b: H2RAM window 3 enabled.
2	R/W	0b	**H2RAM Window 2 Enable (H2RAMW2E)** 0b: Disable 1b: H2RAM window 2 enabled.
1	R/W	0b	**H2RAM Window 1 Enable (H2RAMW1E)** 0b: Disable 1b: H2RAM window 1 enabled.
0	R/W	0b	**H2RAM Window 0 Enable (H2RAMW0E)** 0b: Disable 1b: H2RAM window 0 enabled.

6.4.4.34 Host RAM Window 0 Base Address (HRAMW0BA[11:4])

Address Offset: 5Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Host RAM Window 0 Base Address Bits [11:4] (HRAMW0BA[11:4])** Define RAM window 0 base address.

6.4.4.35 Host RAM Window 1 Base Address (HRAMW1BA[11:4])

Address Offset: 5Ch

Bit	R/W	Default	Description
0	R/W	00h	**Host RAM Window 1 Base Address Bits [11:4] (HRAMW1BA[11:4])** Define RAM window 1 base address.

6.4.4.36 Host RAM Window 0 Access Allow Size (HRAMW0AAS)

Address Offset: 5Dh

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7-6	R/W	0h	**Host RAM Window 0 Read Protect Enable (HRAMW0RPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	**Host RAM Window 0 Write Protect Enable (HRAMW0WPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	**Reserved**
2-0	R/W	0h	**Host RAM Window 0 Size (HRAMW0S)** 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

6.4.4.37 Host RAM Window 1 Access Allow Size (HRAMW1AAS)

Address Offset: 5Eh

Bit	R/W	Default	Description
7-6	R/W	0h	**Host RAM Window 1 Read Protect Enable (HRAMW1RPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	**Host RAM Window 1 Write Protect Enable (HRAMW1WPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	**Reserved**
2-0	R/W	0h	**Host RAM Window 1 Size (HRAMW1S)** 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

6.4.4.38 Host RAM Window 2 Base Address (HRAMW2BA[11:4])

Address Offset: 76h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host RAM Window 2 Base Address Bits [11:4] (HRAMW2BA[11:4])** Define RAM window 2 base address.

6.4.4.39 Host RAM Window 3 Base Address (HRAMW3BA[11:4])

Address Offset: 77h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host RAM Window 3 Base Address Bits [11:4] (HRAMW3BA[11:4])** Define RAM window 3 base address.

6.4.4.40 Host RAM Window 2 Access Allow Size (HRAMW2AAS)

Address Offset: 78h

Bit	R/W	Default	Description
7-6	R/W	0h	**Host RAM Window 2 Read Protect Enable (HRAMW2RPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	**Host RAM Window 2 Write Protect Enable (HRAMW2WPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	**Reserved**
2-0	R/W	0h	**Host RAM Window 2 Size (HRAMW2S)** 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

6.4.4.41 Host RAM Window 3 Access Allow Size (HRAMW3AAS)

Address Offset: 79h

Bit	R/W	Default	Description
7-6	R/W	0h	**Host RAM Window 3 Read Protect Enable (HRAMW3RPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	**Host RAM Window 3 Write Protect Enable (HRAMW3WPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	**Reserved**

Bit	R/W	Default	Description
2-0	R/W	0h	**Host RAM Window 3 Size (HRAMW3S)** 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

6.4.4.42 H2RAM EC Semaphore Interrupt Enable (H2RAMECSIE)

Address Offset: 7Ah

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**H2RAM EC Semaphore 3 Interrupt Enable (H2RAMECS3IE)** 0b: Disable 1b: A Data-Write instruction executed on H2RAM EC semaphore 3 will produce an IRQ to the host.
2	R/W	0b	**H2RAM EC Semaphore 2 Interrupt Enable (H2RAMECS2IE)** 0b: Disable 1b: A Data-Write instruction executed on H2RAM EC semaphore 2 will produce an IRQ to the host.
1	R/W	0b	**H2RAM EC Semaphore 1 Interrupt Enable (H2RAMECS1IE)** 0b: Disable 1b: A Data-Write instruction executed on H2RAM EC semaphore 1 will produce an IRQ to the host.
0	R/W	0b	**H2RAM EC Semaphore 0 Interrupt Enable (H2RAMECS0IE)** 0b: Disable 1b: A Data-Write instruction executed on H2RAM EC semaphore 0 will produce an IRQ to the host.

6.4.4.43 Static DMA Control Register (STCDMACR)

Address Offset: 80h

Bit	R/W	Default	Description
7	R/WC	0b	**Static DMA Interrupt Status** 0b: No Interrupt. 1b: Interrupt occurs.
6	R/W	0b	**Static DMA Interrupt Mask** 0b: No mask. 1b: Mask.
5	R	0b	**Auto Load Code from SPI to Eflash Cycle** 0b: No cycle. 1b: Load code cycle.

Bit	R/W	Default	Description
4-1	R/W	0b	**Static DMA SRAM select** 0000b: 0k~4k sram. 0001b: 4k~8k sram. 0010b: 8k~12k sram. 0011b: 12k~16k sram. 0100b: 16k~20k sram. 0101b: 20k~24k sram. 0110b: 24k~28k sram. 0111b: 28k~32k sram. 1000b: 32k~36k sram. 1001b: 36k~40k sram. 1010b: 40k~44k sram. 1011b: 44k~48k sram. 1100b: 48k~52k sram. Else: Reserved
0	R/W	0b	**Static DMA Enable** 0b: Disable 1b: Enable

6.4.4.44 Scratch SRAM 5 Address Low Byte Register (SCAR5L)

Address Offset: 81h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 5 Address (SC5A7-0)**

6.4.4.45 Scratch SRAM 5 Address Middle Byte Register (SCAR5M)

Address Offset: 82h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 5 Address (SC5A15-8)**

6.4.4.46 Scratch SRAM 5 Address High Byte Register (SCAR5H)

Address Offset: 83h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 5 Address (SC5A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 5 Address (SC5A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.47 Scratch SRAM 6 Address Low Byte Register (SCAR6L)

Address Offset: 84h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 6 Address (SC6A7-0)**

6.4.4.48 Scratch SRAM 6 Address Middle Byte Register (SCAR6M)

Address Offset: 85h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 6 Address (SC6A15-8)**

6.4.4.49 Scratch SRAM 6 Address High Byte Register (SCAR6H)

Address Offset: 86h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 6 Address (SC6A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 6 Address (SC6A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.50 Scratch SRAM 7 Address Low Byte Register (SCAR7L)

Address Offset: 87h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 7 Address (SC7A7-0)**

6.4.4.51 Scratch SRAM 7 Address Middle Byte Register (SCAR7M)

Address Offset: 88h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 7 Address (SC7A15-8)**

6.4.4.52 Scratch SRAM 7 Address High Byte Register (SCAR7H)

Address Offset: 89h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 7 Address (SC7A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 7 Address (SC7A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.53 Scratch SRAM 8 Address Low Byte Register (SCAR8L)

Address Offset: 8Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 8 Address (SC8A7-0)**

6.4.4.54 Scratch SRAM 8 Address Middle Byte Register (SCAR8M)

Address Offset: 8Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 8 Address (SC8A15-8)**

6.4.4.55 Scratch SRAM 8 Address High Byte Register (SCAR8H)

Address Offset: 8Ch

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 8 Address (SC8A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 8 Address (SC8A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.56 Scratch SRAM 9 Address Low Byte Register (SCAR9L)

Address Offset: 8Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 9 Address (SC9A7-0)**

6.4.4.57 Scratch SRAM 9 Address Middle Byte Register (SCAR9M)

Address Offset: 8Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 9 Address (SC9A15-8)**

6.4.4.58 Scratch SRAM 9 Address High Byte Register (SCAR9H)

Address Offset: 8Fh

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 9 Address (SC9A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 9 Address (SC9A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.59 Scratch SRAM 10 Address Low Byte Register (SCAR10L)

Address Offset: 90h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 10 Address (SC10A7-0)**

6.4.4.60 Scratch SRAM 10 Address Middle Byte Register (SCAR10M)

Address Offset: 91h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 10 Address (SC10A15-8)**

6.4.4.61 Scratch SRAM 10 Address High Byte Register (SCAR10H)

Address Offset: 92h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 10 Address (SC10A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 10 Address (SC10A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.62 Scratch SRAM 11 Address Low Byte Register (SCAR11L)

Address Offset: 93h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 11 Address (SC11A7-0)**

6.4.4.63 Scratch SRAM 11 Address Middle Byte Register (SCAR11M)

Address Offset: 94h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 11 Address (SC11A15-8)**

6.4.4.64 Scratch SRAM 11 Address High Byte Register (SCAR11H)

Address Offset: 95h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 11 Address (SC11A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 11 Address (SC11A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.65 Scratch SRAM 12 Address Low Byte Register (SCAR12L)

Address Offset: 96h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 12 Address (SC12A7-0)**

6.4.4.66 Scratch SRAM 12 Address Middle Byte Register (SCAR12M)

Address Offset: 97h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 12 Address (SC12A15-8)**

6.4.4.67 Scratch SRAM 12 Address High Byte Register (SCAR12H)

Address Offset: 98h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 12 Address (SC12A19)**
6-3	-	-	**Reserved**
2-0	R/W	000b	**Scratch SRAM 12 Address (SC12A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.68 ROM Address Low Byte Register (ROMARL)

Address Offset: 99h

Bit	R/W	Default	Description
7-0	R/W	00h	**ROM Address (ROMA7-0)**

6.4.4.69 ROM Address Middle Byte Register (ROMARM)

Address Offset: 9Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**ROM Address (ROMA15-8)**

6.4.4.70 ROM Address High Byte Register (ROMARH)

Address Offset: 9Bh

Bit	R/W	Default	Description
7-4	R/W	0h	**Reserved**
3-0	R/W	0111b	**ROM Address (ROMA19-16)** The {ROMARH, ROMARM, ROMARL} defines the address of the ROM. The default value is 448KB.

6.4.4.71 SPI Extend Mode Base Address Low Byte Register (SEMBARL)

Address Offset: 9Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**SPI Extend Mode Base Address (A7-0)**

6.4.4.72 SPI Extend Mode Base Address Middle Byte Register (SEMBARM)

Address Offset: 9Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**SPI Extend Mode Base Address (A15-8)**

6.4.4.73 SPI Extend Mode Base Address High Byte Register (SEMBARH)

Address Offset: 9Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**SPI Extend Mode Base Address (A23-16)**

6.4.4.74 Flash Control 5 Register (FLHCTRL5R)

Address Offset: A3h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	RW	0	ESPI/Eflash select register 0: Eflash 1: ESPI
2-0	-	-	Reserved

6.4.4.75 Flash Control 6 Register (FLHCTRL6R)

Address Offset: A2h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**Enable EC-Indirect Page Program (ECINDPP)** 1b: If the embedded flash's size of this part number is larger than 256K-byte, enable the page program cycle constructed by EC-Indirect Follow Mode. 0b: Otherwise
2	-	-	**Reserved**

Bit	R/W	Default	Description
1-0	R	01b	**Limit e-flash size (LFS)** 00b: No e-flash available; Always fetch from the SPI flash. 01b: Treat e-flash size as 2K-byte; uC address 0-7FFh will be fetched from the e-flash, otherwise will be fetched from the SPI flash. 10b: Treat e-flash size as 4K-byte; uC address 0-FFFh will be fetched from the e-flash, otherwise will be fetched from the SPI flash. 11b: Treat e-flash size as 128K-byte

6.4.4.76 Scratch SRAM 13 Address Low Byte Register (SCAR13L)

Address Offset: B0h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 13 Address (SC13A7-0)**

6.4.4.77 Scratch SRAM 13 Address Middle Byte Register (SCAR13M)

Address Offset: B1h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 13 Address (SC13A15-8)**

6.4.4.78 Scratch SRAM 13 Address High Byte Register (SCAR13H)

Address Offset: B2h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 13 Address (SC13A19)**
6-3	-	-	**Reserved**
2-0	R/W	1000b	**Scratch SRAM 13 Address (SC13A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.79 Scratch SRAM 14 Address Low Byte Register (SCAR14L)

Address Offset: B3h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 14 Address (SC14A7-0)**

6.4.4.80 Scratch SRAM 14 Address Middle Byte Register (SCAR14M)

Address Offset: B4h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 14 Address (SC14A15-8)**

6.4.4.81 Scratch SRAM 14 Address High Byte Register (SCAR14H)

Address Offset: B5h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 14 Address (SC14A19)**
6-3	-	-	**Reserved**
2-0	R/W	1000b	**Scratch SRAM 14 Address (SC14A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.82 Scratch SRAM 15 Address Low Byte Register (SCAR15L)

Address Offset: B6h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 15 Address (SC15A7-0)**

6.4.4.83 Scratch SRAM 15 Address Middle Byte Register (SCAR15M)

Address Offset: B7h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 15 Address (SC15A15-8)**

6.4.4.84 Scratch SRAM 15 Address High Byte Register (SCAR15H)

Address Offset: B8h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 15 Address (SC15A19)**
6-3	-	-	**Reserved**
2-0	R/W	1000b	**Scratch SRAM 15 Address (SC15A18-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.4.4.85 Scratch SRAM 16 Address Low Byte Register (SCAR16L)

Address Offset: B9h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 16 Address (SC16A7-0)**

6.4.4.86 Scratch SRAM 16 Address Middle Byte Register (SCAR16M)

Address Offset: BAh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 16 Address (SC16A15-8)**

6.4.4.87 Scratch SRAM 16 Address High Byte Register (SCAR16H)

Address Offset: BBh

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 16 enable**
6-4	-	-	**Reserved**
3-0	R/W	0000b	**Scratch SRAM 16 Address (SC16A19-16)**

6.4.4.88 Scratch SRAM 17 Address Low Byte Register (SCAR17L)

Address Offset: BCh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 17 Address (SC17A7-0)**

6.4.4.89 Scratch SRAM 17 Address Middle Byte Register (SCAR17M)

Address Offset: BDh

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 17 Address (SC17A15-8)**

6.4.4.90 Scratch SRAM 17 Address High Byte Register (SCAR17H)

Address Offset: BEh

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 17 enable**
6-4	-	-	**Reserved**
3-0	R/W	0000b	**Scratch SRAM 17 Address (SC17A19-16)**

6.4.4.91 Scratch SRAM 18 Address Low Byte Register (SCAR18L)

Address Offset: BFh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 18 Address (SC18A7-0)**

6.4.4.92 Scratch SRAM 18 Address Middle Byte Register (SCAR18M)

Address Offset: C0h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 18 Address (SC18A15-8)**

6.4.4.93 Scratch SRAM 18 Address High Byte Register (SCAR18H)

Address Offset: C1h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 18 enable**
6-4	-	-	**Reserved**
3-0	R/W	0000b	**Scratch SRAM 18 Address (SC18A19-16)**

6.4.4.94 Scratch SRAM 19 Address Low Byte Register (SCAR19L)

Address Offset: C2h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 19 Address (SC19A7-0)**

6.4.4.95 Scratch SRAM 19 Address Middle Byte Register (SCAR19M)

Address Offset: C3h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 19 Address (SC19A15-8)**

6.4.4.96 Scratch SRAM 19 Address High Byte Register (SCAR19H)

Address Offset: C4h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 19 enable**
6-4	-	-	**Reserved**
3-0	R/W	0000b	**Scratch SRAM 19 Address (SC19A19-16)**

6.4.4.97 Scratch SRAM 20 Address Low Byte Register (SCAR20L)

Address Offset: C5h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 20 Address (SC20A7-0)**

6.4.4.98 Scratch SRAM 20 Address Middle Byte Register (SCAR20M)

Address Offset: C6h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 2 Address (SC20A15-8)**

6.4.4.99 Scratch SRAM 20 Address High Byte Register (SCAR20H)

Address Offset: C7h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 20 Enable**
6-4	-	-	**Reserved**
3-0	R/W	0000b	**Scratch SRAM 20 Address (SC20A19-16)**

6.4.4.100 Scratch SRAM 21 Address Low Byte Register (SCAR21L)

Address Offset: C8h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 21 Address (SC21A7-0)**

6.4.4.101 Scratch SRAM 21 Address Middle Byte Register (SCAR21M)

Address Offset: C9h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 21 Address (SC21A15-8)**

6.4.4.102 Scratch SRAM 21 Address High Byte Register (SCAR21H)

Address Offset: CAh

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 21 Enable**
6-4	-	-	**Reserved**
3-0	R/W	0000b	**Scratch SRAM 21 Address (SC21A19-16)**

6.4.4.103 Scratch SRAM 22 Address Low Byte Register (SCAR22L)

Address Offset: CBh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 22 Address (SC22A7-0)**

6.4.4.104 Scratch SRAM 22 Address Middle Byte Register (SCAR22M)

Address Offset: CCh

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 22 Address (SC22A15-8)**

6.4.4.105 Scratch SRAM 22 Address High Byte Register (SCAR22H)

Address Offset: CDh

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 22 Enable**
6-4	-	-	**Reserved**
3-0	R/W	0000b	**Scratch SRAM 22 Address (SC22A19-16)**

6.4.4.106 Scratch SRAM 23 Address Low Byte Register (SCAR23L)

Address Offset: CEh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 23 Address (SC23A7-0)**

6.4.4.107 Scratch SRAM 23 Address Middle Byte Register (SCAR23M)

Address Offset: CFh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 23 Address (SC23A15-8)**

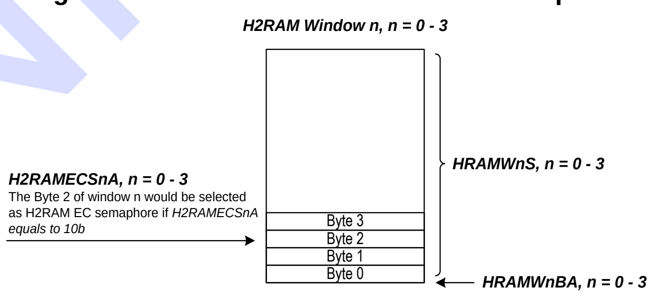
6.4.4.108 Scratch SRAM 23 Address High Byte Register (SCAR23H)

Address Offset: D0h

Bit	R/W	Default	Description
7	R/W	0h	**Scratch SRAM 23 Enable**
6-4	-	-	**Reserved**
3-0	R/W	0000b	**Scratch SRAM 23 Address (SC23A19-16)**

6.4.4.109 H2RAM EC Semaphore Address (H2RAMECSA)

Figure 6-22. Location of H2RAM EC Semaphore



Address Offset: 7Bh

Bit	R/W	Default	Description
7-6	R/W	00b	**H2RAM EC Semaphore 3 Address (H2RAMECS3A)** 00b: H2RAM EC semaphore 3 locates at (HRAMW3BA[11:0] + 0). 01b: H2RAM EC semaphore 3 locates at (HRAMW3BA[11:0] + 1). 10b: H2RAM EC semaphore 3 locates at (HRAMW3BA[11:0] + 2). 11b: H2RAM EC semaphore 3 locates at (HRAMW3BA[11:0] + 3). This field is available only when H2RAM window 3 is enabled.

Bit	R/W	Default	Description
5-4	R/W	00b	**H2RAM EC Semaphore 2 Address (H2RAMECS2A)** 00b: H2RAM EC semaphore 2 locates at (HRAMW2BA[11:0] + 0). 01b: H2RAM EC semaphore 2 locates at (HRAMW2BA[11:0] + 1). 10b: H2RAM EC semaphore 2 locates at (HRAMW2BA[11:0] + 2). 11b: H2RAM EC semaphore 2 locates at (HRAMW2BA[11:0] + 3). This field is available only when H2RAM window 2 is enabled.
3-2	R/W	00b	**H2RAM EC Semaphore 1 Address (H2RAMECS1A)** 00b: H2RAM EC semaphore 1 locates at (HRAMW1BA[11:0] + 0). 01b: H2RAM EC semaphore 1 locates at (HRAMW1BA[11:0] + 1). 10b: H2RAM EC semaphore 1 locates at (HRAMW1BA[11:0] + 2). 11b: H2RAM EC semaphore 1 locates at (HRAMW1BA[11:0] + 3). This field is available only when H2RAM window 1 is enabled.
1-0	R/W	00b	**H2RAM EC Semaphore 0 Address (H2RAMECS0A)** 00b: H2RAM EC semaphore 0 locates at (HRAMW0BA[11:0] + 0). 01b: H2RAM EC semaphore 0 locates at (HRAMW0BA[11:0] + 1). 10b: H2RAM EC semaphore 0 locates at (HRAMW0BA[11:0] + 2). 11b: H2RAM EC semaphore 0 locates at (HRAMW0BA[11:0] + 3). This field is available only when H2RAM window 0 is enabled.

6.4.4.110 H2RAM Host Semaphore Status (H2RAMHSS)

EC can know H2RAM host semaphore status by reading this register.

Address Offset: 7Ch

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/WC	0b	**H2RAM Host Semaphore 3 Status (H2RAMHS3S)** This bit is automatically set to 1b while H2RAM host semaphore 3 is written. 0b: H2RAM host semaphore 3 is not written. 1b: H2RAM host semaphore 3 is written. Writng 1 to clear this bit.
2	R/WC	0b	**H2RAM Host Semaphore 2 Status (H2RAMHS2S)** This bit is automatically set to 1b while H2RAM host semaphore 2 is written. 0b: H2RAM host semaphore 2 is not written. 1b: H2RAM host semaphore 2 is written. Writing 1 clears this bit.
1	R/WC	0b	**H2RAM Host Semaphore 1 Status (H2RAMHS1S)** This bit is automatically set to 1b while H2RAM host semaphore 1 is written. 0b: H2RAM host semaphore 1 is not written. 1b: H2RAM host semaphore 1 is written. Writing 1 clears this bit.
0	R/WC	0b	**H2RAM Host Semaphore 0 Status (H2RAMHS0S)** This bit is automatically set to 1b while H2RAM host semaphore 0 is written. 0b: H2RAM host semaphore 0 is not written. 1b: H2RAM host semaphore 0 is written. Writing 1 clears this bit.

6.4.5 Host Interface Registers

The registers of SMFI can be divided into two parts, Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. The SMFI resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below

Table 6-29. Host View Register Map, SMFI

7 ... 0	Offset
Shared Memory Indirect Memory Address (SMIMAR0-3)	00h-03H
Shared Memory Indirect Memory Data (SMIMDR)	04h
Shared Memory Host Semaphore (SMHSR)	0Ch

6.4.5.1 Shared Memory Indirect Memory Address Register 0 (SMIMAR0)

The following set of registers is accessible only by the host. The registers are applied to VCC.
This register defines the addresses 7-0 for a read or write transaction to the memory.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR7-0)**

6.4.5.2 Shared Memory Indirect Memory Address Register 1 (SMIMAR1)

This register defines the addresses 15-8 for a read or write transaction to the memory.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR15-8)**

6.4.5.3 Shared Memory Indirect Memory Address Register 2 (SMIMAR2)

This register defines the addresses 23-16 for a read or write transaction to the memory.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR23-16)**

6.4.5.4 Shared Memory Indirect Memory Address Register 3 (SMIMAR3)

This register defines the addresses 31-24 for a read or write transaction to the memory.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR31-24)**

6.4.5.5 Shared Memory Indirect Memory Data Register (SMIMDR)

This register defines the Data bits 7-0 for a read or write transaction to the memory.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Data (IMDA7-0)**

6.4.5.6 Shared Memory Host Semaphore Register (SMHSR)

This register provides eight semaphore bits between the EC and the host. Bits 3-0 may be set by the host and Bits 7-4 may be set by the EC. The register reset on host domain hardware reset.
This register is the same as the one in section 6.4.4.4 on page 121 but they are in different views.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-4	R	0h	**EC Semaphore (CSEM3-0)** Four bits that may be updated by the EC and read by both the host and EC.
3-0	R/W	0b	**Host Semaphore (HSEM3-0)** Four bits that may be updated by the host and read by both the host and EC.

6.5 System Wake-Up Control (SWUC)

6.5.1 Overview

SWUC detects wakeup events and generates SCI#, SMI# and PWUREQ# signals to the host side, or alerts EC by interrupts to WUC.

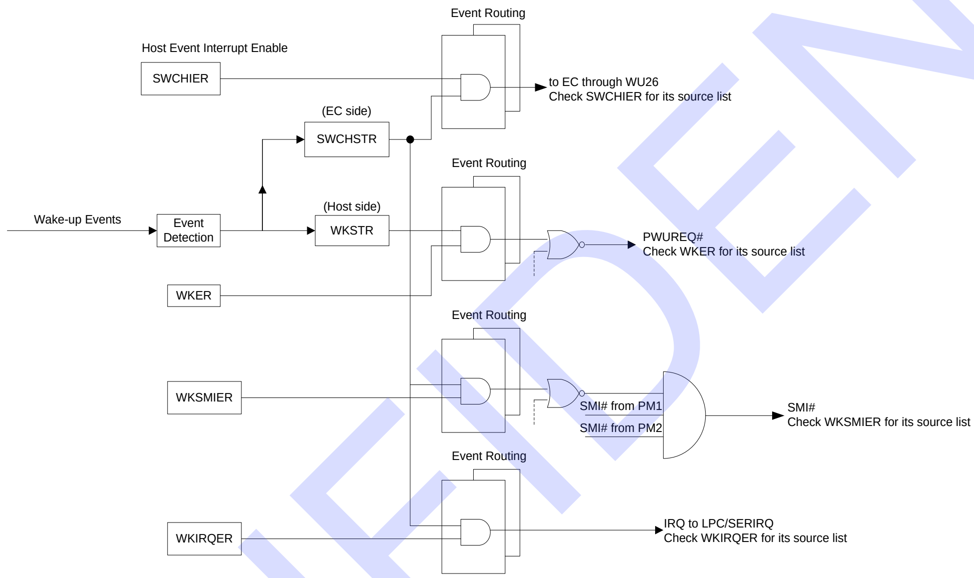
6.5.2 Features

- Supports programmable wake-up events source from the host controlled modules.
- Generates SMI# or PWUREQ# interrupt to the host to wake-up system.

6.5.3 Functional Description

The wakeup event and gathering scheme is shown in Figure 6-23. Wakeup Event and Gathering Scheme on page 144.

Figure 6-23. Wakeup Event and Gathering Scheme



6.5.3.1 Wake-Up Status

When the wake-up event is detected, the related status bit is set to 1 in both host and EC status registers no matter whether there are any event enable bits set or not. A status bit is cleared by writing 1 to it. Writing 0 to a status bit does not change its value. Clearing the event enable bit does not affect the status bit, but prevents it from issuing an event to output. The host uses a mask register (WKSMIER) to decide what the status bits will respond to.

6.5.3.2 Wake-Up Events

When a wake-up event is detected, it is recorded on a status bit in WKSTR (host view) register and SWCHSTR register (EC view), regardless of the enabled bit. Each event behavior is determined by a wake up control logic controlled by a set of dedicated registers.

Input events are detected by the SWUC shown below:
- Module IRQ Wake-up event
- Modem Ring (RI1# and RI2#)
- Software event
- Legacy off event
- ACPI state change Event

Module IRQ Wake-Up Event
A module IRQ wake-up event from each logical device is asserted when the leading edge of the module IRQ is detected.

The related enable bit (WKIRQEN) has to be set to 1 to enable and trigger a wake-up event. Refer to the IRQNUM and WKIRQEN fields in IRQNUMX register. When the event is detected, MIRQS bit in WKSTR register is set to 1. If MIRQE in WKER register is also set to 1, the PWUREQ# output is still asserted and until the status bit is cleared.

Modem Ring
If a transition from high to low on RI1# (or RI2#) is detected on the Serial Port 1 (or Serial Port 2) connected to a modem, and then when the signal goes high on RI1#(or RI2#), it will cause a ring wake-up event asserted if the RI1#(or RI2#) event enable bit is set to 1 in the WKER register (bit0 for RI1#, and bit1 for RI2#).

Telephone Ring
If a transition from high to low is detected on the Ring input pin, and then when the signal goes high on Ring input pin. It will cause a ring wake-up event asserted when the ring event enable bit is set to 1 in the WKER register (BIT3).

Software Event
This bit may trigger a wake event by software control. When the SIRQS (Software IRQ Event Status bit) in WKSTR register is set, a software event to the host is active. When the SIRQS bit in SWCHSTR register is set, a software event to the EC is active. The software event may be activated by the EC via access to the host Controlled Module bridge regardless of the VCC status.

The SIRQS bit in SWCHSTR may be set when the respective bit toggles in WKSTR from 0 to 1 and when HSECM=0 is in SWCTL1 register. When HSECM =1 t, the SIRQS bit in SWCHSTR is set on a write of a 1 to the respective bit in WKSTR. The SIRQS bit in SWCHSTR is cleared by writing 1 to it.

Legacy Off Events
The host supports either legacy or ACPI mode. The operation mode is assigned on PWRBTN bit in the Super I/O Power Mode Register (SIOPWR). When EISCRDPBM bit in SWCIER register is set, any change in this bit will generate an interrupt to the EC. The EC may read this bit, using SCRDPBM bit in SWCTL2 register, to determine the other power state. In the legacy mode, the PWRSLY bit in SIOPWR register represents a request to turn off power. When this bit is set and SCRDPSO bit in SWCTL2 register is set, an interrupt is generated to EC if EISCRDPSO bit in SWCIER register is also set.

ACPI State Change Events
The bits (S1-S5) in WKACPIR register are used to provide a set of 'system power state change request'. The host uses these bits to issue an ACPI state change request. A write of 1 to any of these bits represents a state change request to the EC,and the request may be also read out in SWCTL2 register even ACPIRS0 is represented when all bits in WKACPIR is cleared to 0. When any of ACPIRS0 -S5 bits in SWCTL2 is set and the respective mask bit in SWCIER register is set, an interrupt is generated to EC. All interrupt outputs may be

cleared either writing 1 to the status bit or clearing the masking interrupt enable register.

6.5.3.3 Wake-Up Output Events

The SWUC output four types of wake-up events:
IRQ Interrupt through SERIRQ to the host side, activated by SWUC logical device of PNPCFG.
PWUREQ# Routing as an SCI# event.
SMI# Routing as an SMI# event.
WU26 An interrupt to the WUC module in the EC domain, which is handled by EC firmware.

Output events are generated to the host when their status bit is set (1 in WKSTR). The output event to the EC through the WUC is generated when their EC status bit is set (1 in SWCHSTR). The host can program three Event Routing Control registers (WKSTR, WKSMIER and WKIRQER) to handle each of the host events to be asserted. This allows selective routing of these events output to PWUREQ#, SMI# and/or SWUC interrupt request (IRQ). After an output event is asserted, it can be cleared either by clearing its status bit or being masked. The current status of the event may be read out at the Wake-Up Event Status Register(WKSTR), and Wake-Up Signals Monitor Register (WKSMR). The SWUC also handles the wake-up event coming from the PMC 1 and 2 for SMI# event. In the EC domain, Wake-Up Event Interrupt Enable register (SWCHIER) holds an enable bit to allow selective routing of the event to output the EC wake-up interrupt (WU26) to the WUC.

6.5.3.4 Other SWUC Controlled Options

Additionally, the SWUC handles the following system control signals:
Host Keyboard Reset (KBRST#)
GA20 Signal
Host Configuration Address Option

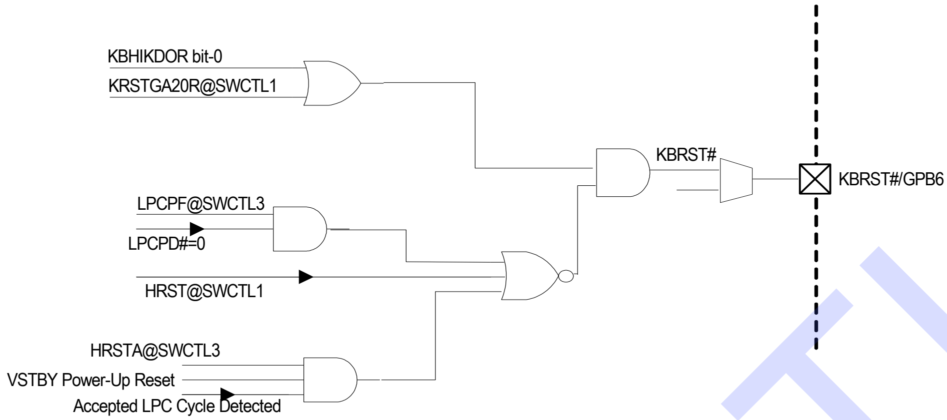
- **Host Keyboard Reset (KBRST#)**

The Host Keyboard Reset output (KBRST#) can be asserted either by software or hardware:
Software: KBRST# will be asserted when the EC firmware issues a reset command by writing 1 to HRST in SWCTL1 register. Clear this bit to de-assert the KBRST#.
Hardware: KBRST# will be asserted during VSTBY Power-Up reset if HRSTA bit in SWCTL3 register is set and a LPC transaction is started.

The KBRST# signal will be active in the following conditions:
(1) HRSTA bit in the SWUC is enabled and LPC cycle is active when the VSTBY is powered on.
(2) LPCPF bit in the SWUC is enabled and LPCPD# signal is active.
(3) HRST bit in the SWUC is enabled.
(4) Bit 0 of KBHIKDOR in the KBC is enabled if KRSTGA20R is set.

The KBRST# output scheme is shown in Figure 6-24 on page 147.
Note it is another way to use GPIO output function to send KBRST# signal.

Figure 6-24. KBRST# Output Scheme



- **GA20 Signal**

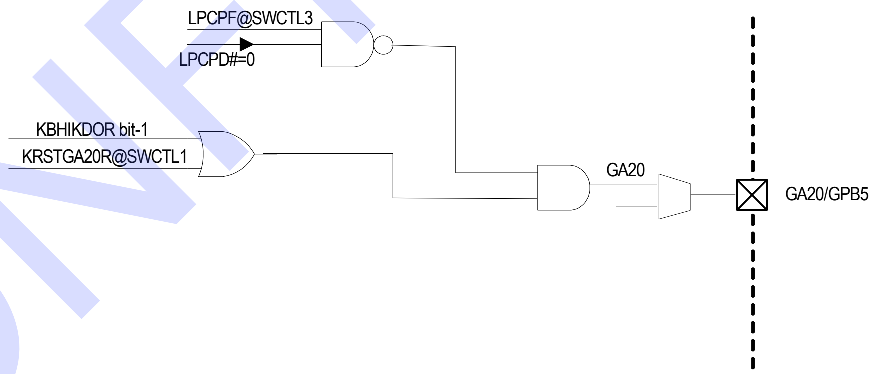
In the chip, the GA20 is connected to a GPIO signal that is configured as output. Port GPB5 is recommended to be used as GA20 since its initial state is output driving high.
EC can assert the GA20 signal state by

1. modifying GPB5 in GPIO register.
2. writing 1 to LPCPF in SWCTL3 register and GA20 signal will be asserted while LPCPD# signal is active.

The GA20 signal will be active in the following conditions:
(1) LPCPF bit in the SWUC is enabled and LPCPD# signal is active.
(2) Bit 1 of KBHIKDOR in the KBC is enabled if KRSTGA20R is set.

The GA20 output scheme is shown in Figure 6-25 on page 147.
Note it is another way to use GPIO output function to send GA20 signal.

Figure 6-25. GA20 Output Scheme



- **Host Configuration Address Option**

The contents of SWCBAHR and SWCBALR change only during VSTBY Power-Up reset. To update the base address of the PNPCFG registers, refer to the followings for the detail:
1. Clear HCAV bit in SWCTL1 register by writing 1 to it.
2. Write the lower byte of the address to SWCBALR (LSB has to be cleared).
3. Write the higher byte of the address to SWCBAHR.
4. Set HCAL bit to prevent the unintended change in the SWCBALR and SWCBAHR register.

6.5.4 Host Interface Registers

The registers of SWUC can be divided into two parts, Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. SWUC resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The SWUC host interface registers are battery-backed. These registers are listed below.

Table 6-30. Host View Register Map, SWUC

7 0	Offset
Wake-Up Event Status Register (WKSTR)	00h
Wake-Up Enable Register (WKER)	02h
Wake-Up Signals Monitor Register (WKSMR)	06h
Wake-Up ACPI Status Register (WKACPIR)	07h
Wake-Up SMI# Enable Register (WKSMIER)	13h
Wake-Up Interrupt Enable Register (WKIRQER)	15h

6.5.4.1 Wake-Up Event Status Register (WKSTR)

The register is used to monitor the status of wake-up events. The register will be cleared when the VSTBY power is powered up, or the host domain software reset occurs.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/WC	0b	**Module IRQ Event Status (MIRQS)** 0: Event is not active. 1: Event is active.
6	R/WC	0b	**Software IRQ Event Status (SIRQS)** The function of this bit can be changed by programming the HSECM bit in SWUC Control Status Register (SWCTL1). When HSECM=0 and writing 1 to this bit, the value of this bit will be inverted. When HSECM=1 and writing 1 to this bit, the bit is set to 1. The bit will be cleared when the SIRQS bit in SWUC Host Event Status Register (SWCHSTR) is written to 1. 0: Event is not active. 1: Event is active.
5-4	R	00b	**Reserved**
3	R/WC	0b	**RING# Event Status (RINGS)** If the RING detection mode is disabled, the bit is always 0. 0: Event is not active. 1: Event is active.
2	R	0b	**Reserved**
1	R/WC	0b	**RI2# Event Status (RI2S)** 0: Event is not active. 1: Event is active.
0	R/WC	0b	**RI1# Event Status (RI1S)** 0: Event is not active. 1: Event is active.

6.5.4.2 Wake-Up Event Enable Register (WKER)

The register is used to enable the individual wake-up events to generate PWUREQ# interrupt. The register will be cleared when the VSTBY power is powered up, or the host domain software reset occurs.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/W	0b	**Module IRQ Event Enable (MIRQE)** 0: Disable 1: Enable
6	R/W	0b	**Software IRQ Event Enable (SIRQE)** 0: Disable 1: Enable
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event Enable (RINGE)** 0: Disable. 1: Enable.
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event Enable (RI2E)** 0: Disable 1: Enable
0	R/W	0b	**RI1# Event Enable (RI1E)** 0: Disable 1: Enable

6.5.4.3 Wake-Up Signals Monitor Register (WKSMR)

The register is used to monitor the value of the SMI# and PWUREQ# signals and identify the generated source. This register is a read-only register.

Address Offset: 06h

Bit	R/W	Default	Description
7-6	R	00b	**Reserved**
5	R	0b	**PWUREQ# Output from SWUC (PWUREQOS)** 0: PWUREQ# output from SWUC is low. 1: PWUREQ# output from SWUC is high.
4	R	0b	**PWUREQ# Signal Status (PWUREQS)** 0: PWUREQ# signal is low. 1: PWUREQ# signal is high.
3	R	0b	**SMI# Output from PMC2 (PM2SMI)** 0: SMI# output from PM channel 2 is low. 1: SMI# output from PM channel 2 is high.
2	R	0b	**SMI# Output from PMC1 (PM1SMI)** 0: SMI# output from PM channel 1 is low. 1: SMI# output from PM channel 1 is high.
1	R	0b	**SMI# Output from SWUC (SWCSMI)** 0: SMI# output from SWUC is low. 1: SMI# output from SWUC is high.
0	R	0	**SMI# Signal Status (SMIS)** 0: SMI# signal is low. 1: SMI# signal is high.

6.5.4.4 Wake-Up ACPI Status Register (WKACPIR)

The register is used to monitor the status of ACPI. When this register is read, its value always returns 00h.

Address Offset: 07h

Bit	R/W	Default	Description
7-6	R	00b	**Reserved**
5	R/W	0b	**Change to S5 State (S5)** The host uses this bit to request the EC to change the ACPI S5 state. 0: Not request to change S5 state. 1: Request to change S5 state.
4	R/W	0b	**Change to S4 State (S4)** The host uses this bit to request the EC to change the ACPI S4 state. 0: Not request to change S4 state. 1: Request to change S4 state.
3	R/W	0b	**Change to S3 State (S3)** The host uses this bit to request the EC to change the ACPI S3 state. 0: Not request to change S3 state. 1: Request to change S3 state.
2	R/W	0b	**Change to S2 State (S2)** The host uses this bit to request the EC to change the ACPI S2 state. 0: Not request to change S2 state. 1: Request to change S2 state.
1	R/W	0b	**Change to S1 State (S1)** The host uses this bit to request the EC to change the ACPI S1 state. 0: Not request to change S1 state. 1: Request to change S1 state.
0	R	0b	**Reserved**

6.5.4.5 Wake-Up SMI# Enable Register (WKSMIER)

The register is used to enable the individual wake-up events to generate SMI# interrupt. The register will be cleared when the VSTBY power is powered up, or the host domain software reset occurs.

Address Offset: 13h

Bit	R/W	Default	Description
7	R/W	0b	**Reserved**
6	R/W	0b	**Software IRQ Event to SMI# Enable (SSMIE)** 0: Disable 1: Enable
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event to SMI# Enable (RINGSMIE)** 0: Disable. 1: Enable.
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event to SMI# Enable (RI2SMIE)** 0: Disable 1: Enable
0	R/W	0b	**RI1# Event to SMI# Enable (RI1SMIE)** 0: Disable 1: Enable

6.5.4.6 Wake-Up IRQ Enable Register (WKIRQER)

The register is used to enable the individual wake-up events to generate the interrupt signal that is assigned by SWUC. The register will be cleared when the VSTBY power is powered up, or the host domain software reset occurs.

Address Offset: 15h

Bit	R/W	Default	Description
7	R/W	0b	**Reserved**
6	R/W	0b	**Software IRQ Event to IRQ Enable (SIRQE)** 0: Disable 1: Enable
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event to IRQ Enable (RINGIRQE)** 0: Disable. 1: Enable.
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event to IRQ Enable (RI2IRQE)** 0: Disable 1: Enable
0	R/W	0b	**RI1# Event to IRQ Enable (RI1IRQE)** 0: Disable 1: Enable

6.5.5 EC Interface Registers

The registers of SWUC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the EC interface. The EC interface can only be accessed by the internal processor. The base address for SWUC is 1400h.

These registers are listed below.

Table 6-31. EC View Register Map, SWUC

7 0	Offset
SWUC Control Status 1 Register (SWCTL1)	00h
SWUC Control Status 2 Register (SWCTL2)	02h
SWUC Control Status 3 Register (SWCTL3)	04h
SWUC Host Configuration Base Address Low Byte Register (SWCBALR)	08h
SWUC Host Configuration Base Address High Byte Register (SWCBAHR)	0Ah
SWUC Interrupt Enable Register (SWCIER)	0Ch
SWUC Host Event Status Register (SWCHSTR)	0Eh
SWUC Host Event Interrupt Enable Register (SWCHIER)	10h

6.5.5.1 SWUC Control Status 1 Register (SWCTL1)

The register is used to control the individual wake-up action on SWUC. The register will be cleared when the VSTBY power is powered up. Bit 0 is only cleared when the warm reset occurs.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	1b	**KB Reset/GA20 Routing (KRSTGA20R)** 0: Enable routing bit-0 of KBHIKDOR as KBRST# source. Enable routing bit-1 of KBHIKDOR as GA20 source . 1: Disable above.
6	R/W	0b	**Reserved**
5	R/W	0b	**Host Software Event Clear Mode (HSECM)** This bit is used to control the clear mode of SIRQS bit at the Wake-Up Event Status Register (WKSTR).
4	R/W	0b	**Host Configuration Address Lock (HCAL)** When the bit is written to 1, the Host Configuration Address and the bit will be locked. The bit is only cleared under the condition of VSTBY power-up or watchdog reset.
3	R/WC	0b	**Host Configuration Address Valid (HCAV)** This bit is set after writing SWCBAHR register. 1: Indicate Host Configuration Base Address stored in SWCBALR and SWCBAHR registers are valid. 0: SWCBALR and SWCBAHR registers are not valid. The bit can be cleared by writing to 1.
2	R	0b	**LPC Reset Active (LPCRST)** 0: LPCRST# is inactive. 1: LPCRST# is active.
1	R	-	**VCC Power On (VCCPO)** 0: VCC is powered off. 1: VCC is powered on. See also VCCDO bit in RSTS register in 7.15.4.6 on page 429.
0	R/W	-	**Host Reset Active (HRST)** When this bit is 1, the KBRST# is active to generate one host software reset.

6.5.5.2 SWUC Control Status 2 Register (SWCTL2)

The register is used to control the individual wake-up action on SWUC. The register will be cleared when the VSTBY power is powered up and LPCRST# is active.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/WC	0b	**Super I/O Configuration SIOPWR Power Supply Off (SCRDPSO)** The bit is used to monitor the Power Supply Off (PWRSLY) bit in SIOPWR register of PNPCFG. When the bit is written to 1, clear the bit and the interrupt signal caused by the value change in this bit. A write of 0 to this bit is ignored.
6	R/WC	0b	**Super I/O Configuration SIOPWR Power Button Mode (SCRDPBM)** The bit is used to monitor the Power Button Mode (PWRBTN) bit in SIOPWR register of PNPCFG. When the bit is written to 1, clear the interrupt signal caused by the value change in this bit. A write of 0 to this bit is ignored.

Bit	R/W	Default	Description
5-1	R/WC	00000b	**ACPI request S5-1 (ACPIRS5-1)** These bits are used to monitor the S5-1 bit at the Wake-Up ACPI Status Register (WKACPIR). When the bit is written to 1, clear the bit and the interrupt signal caused by ACPI. A write of 0 to this bit is ignored.
0	R/WC	0b	**ACPI request S0 (ACPIRS0)** If all S5-1 bits at the WKACPIR are written to 0, the bit will be set to 1. The bit will be cleared if the bit is written to 1.

6.5.5.3 SWUC Control Status 3 Register (SWCTL3)

The register is used to control the individual wake-up action on SWUC. The register will only be cleared when the VSTBY power is powered up.

Address Offset: 04h

Bit	R/W	Default	Description
7-2	R	00h	**Reserved**
1	R/W	0b	**LPC Power Fail Turn Off KBRST# and GA20 (LPCPF)** If the bit is set to 1, the KBRST# and GA20 will be forced to low when the LPCPD# signal is active.
0	R/W	1b	**Host Reset Active During VSTBY Power-Up (HRSTA)** If the bit is set to 1, the KBRST# signal will be active when the LPC cycle is active until VSTBY Power-Up Reset is finished. Writing to this bit is ignored if HCAL bit is set.

6.5.5.4 SWUC Host Configuration Base Address Low Byte Register (SWCBALR)

The register is used to program the base address of the SWUC Host Interface registers.
See also Table 6-6 on page 73 and HCAL/HCAV bit in SWCTL1 register.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00h	**Base Address Low Byte (BALB)**

6.5.5.5 SWUC Host Configuration Base Address High Byte Register (SWCBAHR)

The register is used to program the base address of the SWUC Host Interface registers.
See also Table 6-6 on page 73 and HCAL/HCAV bit in SWCTL1 register.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Base Address High Byte (BAHB)**

6.5.5.6 SWUC Interrupt Enable Register (SWCIER)

The register is used to enable the individual interrupt source on SWUC. The interrupt can be cleared by clearing the status bit or masking the source. On the other hand, the register will be cleared when the warm reset is active.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/W	0b	**Enable Interrupt from Super I/O Configuration SIOPWR Power Supply Off (EISCRDPSO)** 1: Generate high-level interrupt when the SCRDPSO bit in SWUC Control Status 2 Register (SWCTL2) is changed. 0: Disable the interrupt source.
6	R/W	0b	**Enable Interrupt from Super I/O Configuration SIOPWR Power Button Mode (EISCRDPBM)** 1: Generate high-level interrupt when the SCRDPBM bit in SWUC Control Status 2 Register (SWCTL2) is changed. 0: Disable the interrupt source.
5-1	R/W	00000b	**Enable Interrupt from ACPI Request S5-1 (EIACPIRS5-1)** 1: Generate high-level interrupt when the ACPIRS5-1 bit in SWUC Control Status 2 Register (SWCTL2) is changed. 0: Disable the interrupt source.
0	-	-	**Reserved**

6.5.5.7 SWUC Host Event Status Register (SWCHSTR)

The information of this register is mirror as the Wake-Up Event Status Register (WKSTR). The status bits can be cleared by writing to the corresponding bit in the two registers. The register will be cleared when the VSTBY power is powered up, or the host software reset occurs.

Address Offset: 0Eh

Bit	R/W	Default	Description
7	R/WC	0b	**Module IRQ Event Status (MIRQS)** 0: Event is not active. 1: Event is active.
6	R/WC	0b	**Software IRQ Event Status (SIRQS)** The function of this bit can be changed by programming HSECM bit in SWUC Control Status Register (SWCTL1). When HSECM=0, this bit is set to 1 when SIRQS toggles to 1 in WKSTR register. When HSECM=1 and this bit is set to 1 while writing 1 to SIRQS in WKSTR register. This bit will be cleared by writing 1 to it. 0: Event is not active. 1: Event is active.
5-4	R	00b	**Reserved**
3	R/WC	0b	**RING# Event Status (RINGS)** If the RING detection mode is disabled, the bit is always 0. 0: Event is not active. 1: Event is active.
2	R	0b	**Reserved**
1	R/WC	0b	**RI2# Event Status (RI2S)** 0: Event is not active. 1: Event is active.

Bit	R/W	Default	Description
0	R/WC	0b	**RI1# Event Status (RI1S)** 0: Event is not active. 1: Event is active.

6.5.5.8 SWUC Host Event Interrupt Enable Register (SWCHIER)

The register is used to enable the individual wake-up events to generate one interrupt to the CPU via WU26 of WUC. The register will be cleared when the warm reset occurs.

Address Offset: 10h

Bit	R/W	Default	Description
7	R/W	0b	**Module IRQ Event Enable (MIRQEE)** 0: Disable 1: Enable
6	R/W	0b	**Software IRQ Event Enable (SIRQEE)** 0: Disable 1: Enable
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event Enable (RINGEE)** 0: Disable. 1: Enable.
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event Enable (RI2EE)** 0: Disable 1: Enable
0	R/W	0b	**RI1# Event Enable (RI1EE)** 0: Disable 1: Enable

6.6 Keyboard Controller (KBC)

6.6.1 Overview

This Keyboard Controller supports a standard keyboard and mouse controller interface.

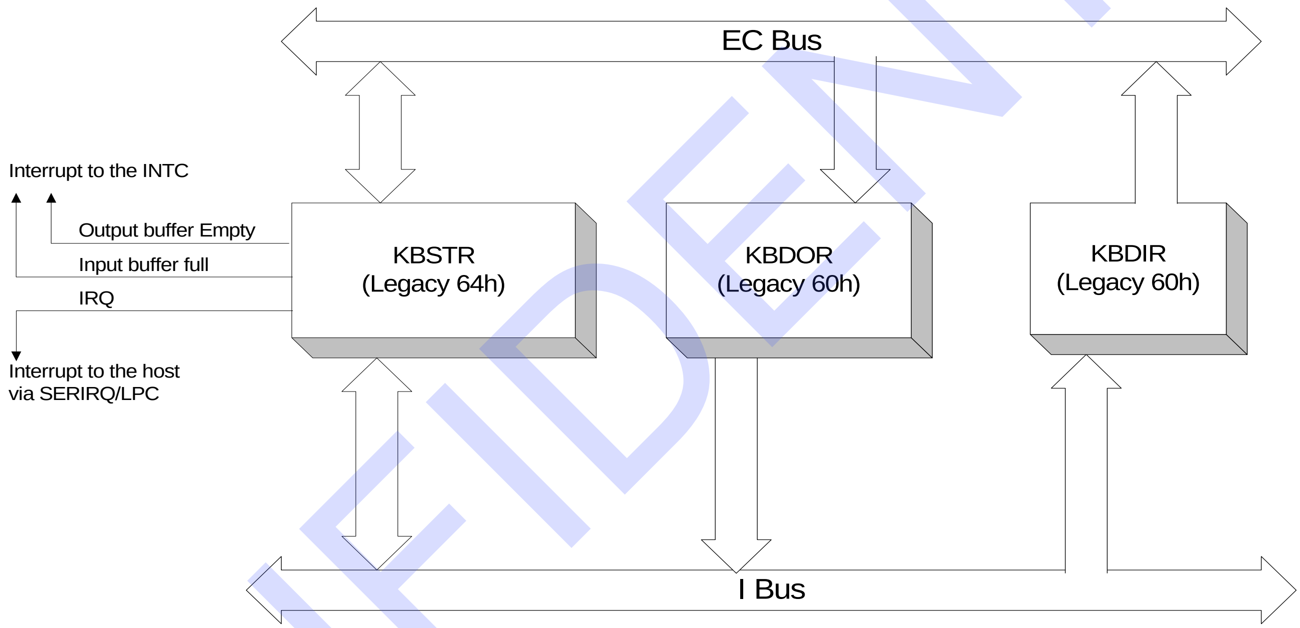
6.6.2 Features

- Compatible with the legacy 8042 interface keyboard controller.
- Supports two standard registers for programming: Command/Data Register and Status Register.
- Automatically generates interrupts to the host side and EC side when the KBC status is changed.

6.6.3 Functional Description

This Keyboard Controller is compatible with the legacy 8042 interface keyboard controller.

Figure 6-26. KBC Host Interface Block Diagram



Status

The host processor can read the status of KBC from the KBC Status Register. The internal CPU can read the status of KBC from the KBC Host Interface Keyboard/Mouse Status Register.

Host Write Data to KBC Interface

When writing to address 60h or 64h (programmable), the IBF bit in the KBC Status Register is set and A2 bit in the KBC Status Register indicates the CPU whose address was written. When writing to address 60h, A2 bit is 0. When writing to address 64h, A2 bit is 1.

EC CPU can identify that the input buffer is full by either polling IBF bit in the Status register or detecting an interrupt (INT24) if the interrupt is enabled. EC CPU can read the data from the KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR), and the IBF bit in the Status Register is cleared.

EC CPU Write Data to KBC Interface

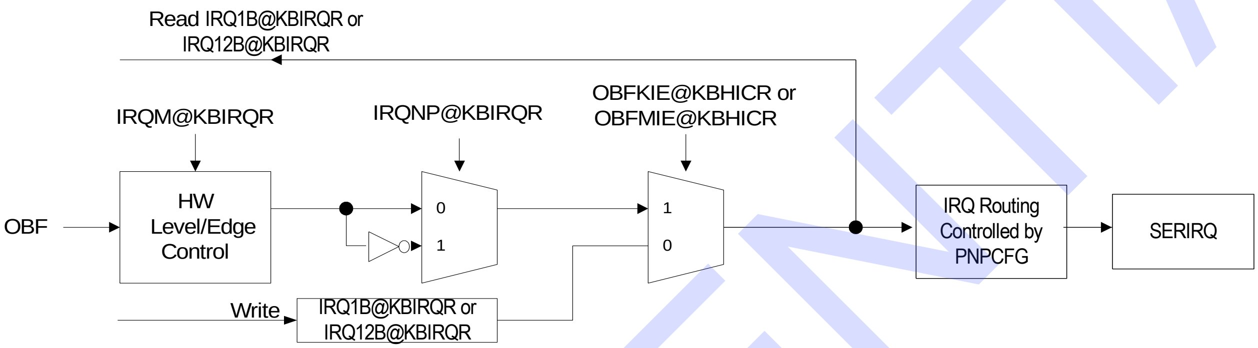
EC CPU can write data to the KBC when it needs to send data to the host. When EC CPU writes data to the KBC Host Interface Keyboard Data Output Register (KBHIKDOR), the OBF bit in the Status Register is set. If the IRQ1 interrupt is enabled, the IRQ1 will be sent to the host. The host can read the Data Output Register when it detects the Output Buffer Full condition. When EC CPU writes data to the KBC Host Interface Mouse

Data Output Register (KBHIMDOR), the OBF bit in the Status Register is set. If the IRQ12 interrupt is enabled, the IRQ12 will be sent to the host. The host can read the Data Output Register when it detects the Output Buffer Full condition. When the Output Buffer Empty interrupt to INTC (INT2) is enabled, the interrupt signal is set high if the output buffer is empty.

Interrupts

There are two interrupts (Input Buffer Full Interrupt and Output Buffer Empty) connected to the INTC.
There are two interrupts (IRQ1 and IRQ12) connected to the host side (SERIRQ).
The IRQ numbers of KBC are programmable and use IRQ1 and IRQ12 as abbreviations in this section.

Figure 6-27. IRQ Control in KBC Module



GA20 and KBRST#

Refer to section 6.5.3.4 on page 146.

6.6.4 Host Interface Registers

The registers of KBC can be divided into two parts, Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor.

The KBC resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. For compatibility issue, the two I/O Port Base Addresses of KBC/Keyboard are suggested to configure at 60h and 64h.

These registers are listed below.

Table 6-32. Host View Register Map, KBC

7 — 0	Offset
KBC Data Input Register (KBDIR)	Legacy 60h
KBC Data Output Register (KBDOR)	Legacy 60h
KBC Command Register (KBCMDR)	Legacy 64h
KBC Status Register (KBSTR)	Legacy 64h

Legacy 60h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 64h represents (I/O Port Base Address 1) + (Offset 0h)
See also Table 6-7 on page 73.

6.6.4.1 KBC Data Input Register (KBDIR)

When the host processor is writing this register, the IBF bit in KBC Status Register (KBSTR) will be set and the A2 bit will be cleared. If the IBFCIE bit in KBC Host Interface Control Register (KBHICR) is enabled, the write action will cause one interrupt to the CPU via INT24 of INTC.

Address Offset: 00h for I/O Port Base Address 0, Legacy 60h

Bit	R/W	Default	Description
7-0	W	-	**KBC Data Input (KBDI)** The data is used to output for Keyboard/Mouse.

6.6.4.2 KBC Data Output Register (KBDOR)

When the host processor is reading this register, The OBF bit in KBC Status Register (KBSTR) will be cleared. The reading access will also clear the interrupt for the host processor when the IRQM bits of KBC Interrupt Control Register (KBIRQR) are programmed to be at level mode. If the OBECIE bit in KBC Host Interface Control Register (KBHICR) is enabled, the read action will cause one interrupt to the CPU via INT2 of INTC.

Address Offset: 00h for I/O Port Base Address 0, Legacy 60h

Bit	R/W	Default	Description
7-0	R	-	**KBC Data Output (KBDO)** The data comes from the Keyboard/Mouse source.

6.6.4.3 KBC Command Register (KBCMDR)

When the register is written, the IBF bit in KBC Status Register (KBSTR) will be set and the A2 bit will be set.

Address Offset: 00h for I/O Port Base Address 1, Legacy 64h

Bit	R/W	Default	Description
7-0	W	-	**KBC Command (KBCMD)** The command data is used to output for Keyboard/Mouse.

6.6.4.4 KBC Status Register (KBSTR)

The host processor uses the register to monitor the status of KBC. The same information is similar to the KBC Host Interface Keyboard/Mouse Status Register (KBHISR). It is used by the internal CPU.

Address Offset: 01h for I/O Port Base Address 0, Legacy 64h

Bit	R/W	Default	Description
7-4	R	0h	**Programming Data 3-0 (PD3-0)** The data is used by the EC firmware to be the general-purpose setting.
3	R	0b	**A2 Address (A2)** The bit is used to keep the A2 address information of the last write operation that the host processor accessed the KBC.
2	R	0b	**Programming Data II (PDII)** The function is the same as that of the PD3-0.
1	R	0b	**Input Buffer Full (IBF)** When the host processor is writing data to KBDIR or KBCMDR, the bit is set. On the other hand, the bit will be cleared when the KBDIR or KBCMDR is read by the EC firmware.
0	R	0b	**Output Buffer Full (OBF)** When the EC CPU is writing data to KBDOR, the bit is set. On the other hand, the bit will be cleared when the KBDOR is read by the host processor.

6.6.5 EC Interface Registers

The registers of KBC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the EC interface. The EC interface can only be accessed by the internal processor. The base address for KBC is 1300h.

These registers are listed below

Table 6-33. EC View Register Map, KBC

7 0	Offset
KBC Host Interface Control Register (KBHICR)	00h
KBC Interrupt Control Register (KBIRQR)	02h
KBC Host Interface Keyboard/Mouse Status Register (KBHISR)	04h
KBC Host Interface Keyboard Data Output Register (KBHIKDOR)	06h
KBC Host Interface Mouse Data Output Register (KBHIMDOR)	08h
KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR)	0Ah

6.6.5.1 KBC Host Interface Control Register (KBHICR)

Address Offset: 00h

Bit	R/W	Default	Description
7	W	-	**Clear Input Buffer Full (CIBF)** When IBFOBFCME is enabled, write 1 to this bit to clear KBC IBF.
6	W	-	**Clear Output Buffer Full (COBF)** When IBFOBFCME is enabled, write 1 to this bit to clear KBC OBF.
5	R/W	0b	**IBF/OBF Clear Mode Enable (IBFOBFCME)** 0: Disable clear mode. 1: Enable IBF/OBF clear mode. Write 1 to this bit to clear by individual KBC/PMC register.
4	R/W	0b	**PM Channel 1 Host Interface Interrupt Enable (PM1HIE)** 0: The IRQ11 is controlled by the IRQ11B bit in KBC Interrupt Control Register (KBIRQR). 1: Enable the interrupt to the host side via SERIRQ for PM channel 1 when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.
3	R/W	0b	**Input Buffer Full CPU Interrupt Enable (IBFCIE)** The bit is used to enable the interrupt to CPU for Keyboard/Mouse when the input buffer is full via INT24 of INTC.
2	R/W	0b	**Output Buffer Empty CPU Interrupt Enable (OBECIE)** The bit is used to enable the interrupt to CPU for Keyboard/Mouse when the output buffer is empty via INT2 of INTC.
1	R/W	0b	**Output Buffer Full Mouse Interrupt Enable (OBFMIE)** 0: The IRQ12 is controlled by the IRQ12B bit in KBIRQR. 1: Enable the interrupt to mouse driver in the host processor via SERIRQ when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.
0	R/W	0b	**Output Buffer Full Keyboard Interrupt Enable (OBFKIE)** 0: The IRQ1 is controlled by the IRQ1B bit in KBIRQR. 1: Enable the interrupt to keyboard driver in the host processor via SERIRQ when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.

6.6.5.2 KBC Interrupt Control Register (KBIRQR)

Address Offset: 02h

Bit	R/W	Default	Description
7	R	0b	**Reserved**
6	R/W	0b	**Interrupt Negative Polarity (IRQNP)** The bit is enabled, and then the interrupt level is inverted.
5-3	R/W	0b	**Interrupt Mode (IRQM)** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is high and a negative pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from SCIPM field in PMCTL register and SMIPM field in PMIC register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Others: Reserved
2	R/W	1b	**IRQ11 Control Bit (IRQ11B)** When the PM1HIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ11 signal. The bit can be used to monitor the status of IRQ11 signal. Reading this bit returns the status of IRQ11 signal, so the read value is not equal to the written value directly.
1	R/W	1b	**IRQ12 Control Bit (IRQ12B)** When the OBFMIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ12 signal. The bit can be used to monitor the status of IRQ12 signal. Reading this bit returns the status of IRQ12 signal, so the read value is not equal to the written value directly.
0	R/W	1b	**IRQ1 Control Bit (IRQ1B)** When the OBFKIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ1 signal. The bit can be used to monitor the status of IRQ1 signal. Reading this bit returns the status of IRQ1 signal, so the read value is not equal to the written value directly.

6.6.5.3 KBC Host Interface Keyboard/Mouse Status Register (KBHISR)

The EC firmware uses the register to monitor the status of KBC. It can use bit 7-4 and bit 2 to send the information to the host processor. The data of this register is the same as that of KBC Status Register (KBSTR).

Address Offset: 04h

Bit	R/W	Default	Description
7-4	R/W	0h	**Programming Data 3-0 (PD3-0)** The data is used by the EC firmware to be the general-purpose setting.
3	R	0b	**A2 Address (A2)** The bit is used to keep the A2 address information of the write operation while the host processor accesses the KBC.
2	R/W	0b	**Programming Data II (PDII)** The function is the same as that of PD3-0.

Bit	R/W	Default	Description
1	R	0b	**Input Buffer Full (IBF)** When the host processor is writing data to KBDIR or KBCMDR, the bit is set. On the other hand, the bit will be cleared when KBHIDIR is read by the EC firmware.
0	R	0b	**Output Buffer Full (OBF)** When EC CPU is writing data to KBHIKDOR and KBHIMDOR, the bit is set. On the other hand, the bit will be cleared when the KBDOR is read by the host.

6.6.5.4 KBC Host Interface Keyboard Data Output Register (KBHIKDOR)

The EC firmware can write the register to send the data of the KBC Data Output Register (KBDOR). Besides, the action will set the OBF bit in the KBC Status Register (KBSTR). If the OBECIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 06h

Bit	R/W	Default	Description
7-0	W	-	**KBC Keyboard Data Output (KBKDO)** The data output to the KBC Data Output Register (KBDOR).

6.6.5.5 KBC Host Interface Mouse Data Output Register (KBHIMDOR)

The EC firmware can write the register to send the data of the KBC Data Output Register (KBDOR). Besides, the action will set the OBF bit in the KBC Status Register (KBSTR). If the OBECIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	W	-	**KBC Mouse Data Output (KBKDO)** The data output to the KBC Data Output Register (KBDOR).

6.6.5.6 KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR)

The EC firmware can read the register to get the data of the KBC Data Input Register (KBDIR). Besides, the action will clear the IBF bit in the KBC Status Register (KBSTR). If the IBFCIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R	-	**KBC Keyboard/Mouse Data Input (KBKMDI)** The data is the same as the data of KBC Data Input Register (KBDIR).

6.7 Power Management Channel (PMC)

6.7.1 Overview

The power management channel is defined in ACPI specification and used as a communication channel between the host processor and embedded controller.

6.7.2 Features

- Supports five PM channels
- Supports compatible mode for channel 1
- Supports enhanced mode for all channels
- Supports shared and private interface
- Supports Command/Status and Data ports
- Supports IRQ/SMI#/SCI# generation

6.7.3 Functional Description

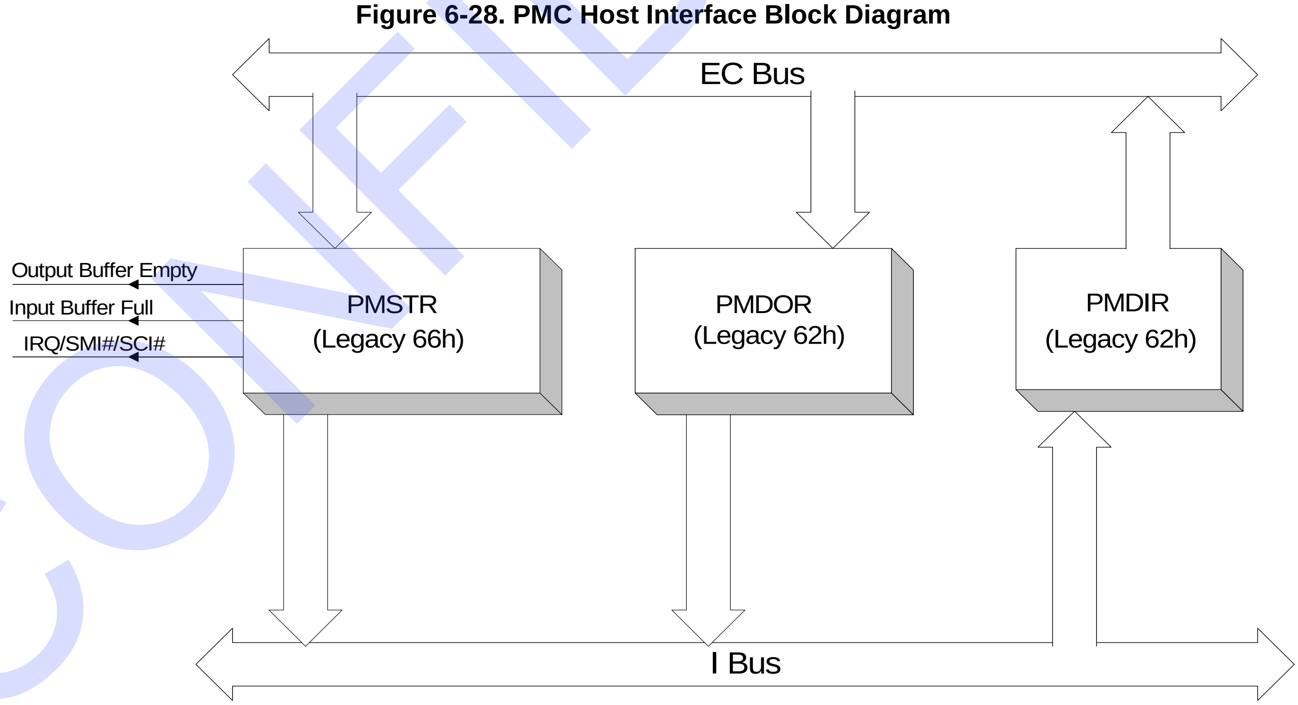
To generate the SCI# and SMI# interrupts to the host

6.7.3.1 General Description

The PM channel supports two operation modes. One is called Compatible mode that is available for channel 1 only. The other is called Enhanced mode. PMC is available for all channels. The PM channel provides four registers, PMDIR, PMDOR, PMCMDR and PMSTR, for communication between the EC and host side. The PMDIR register can be written to by the host and read by the EC. The PMDOR register can be written to by the EC and read by the host. The PMCMDR/PMSTR register can be read by both the EC and Host side.

The PMC host interface block diagram is shown below.

Figure 6-28. PMC Host Interface Block Diagram

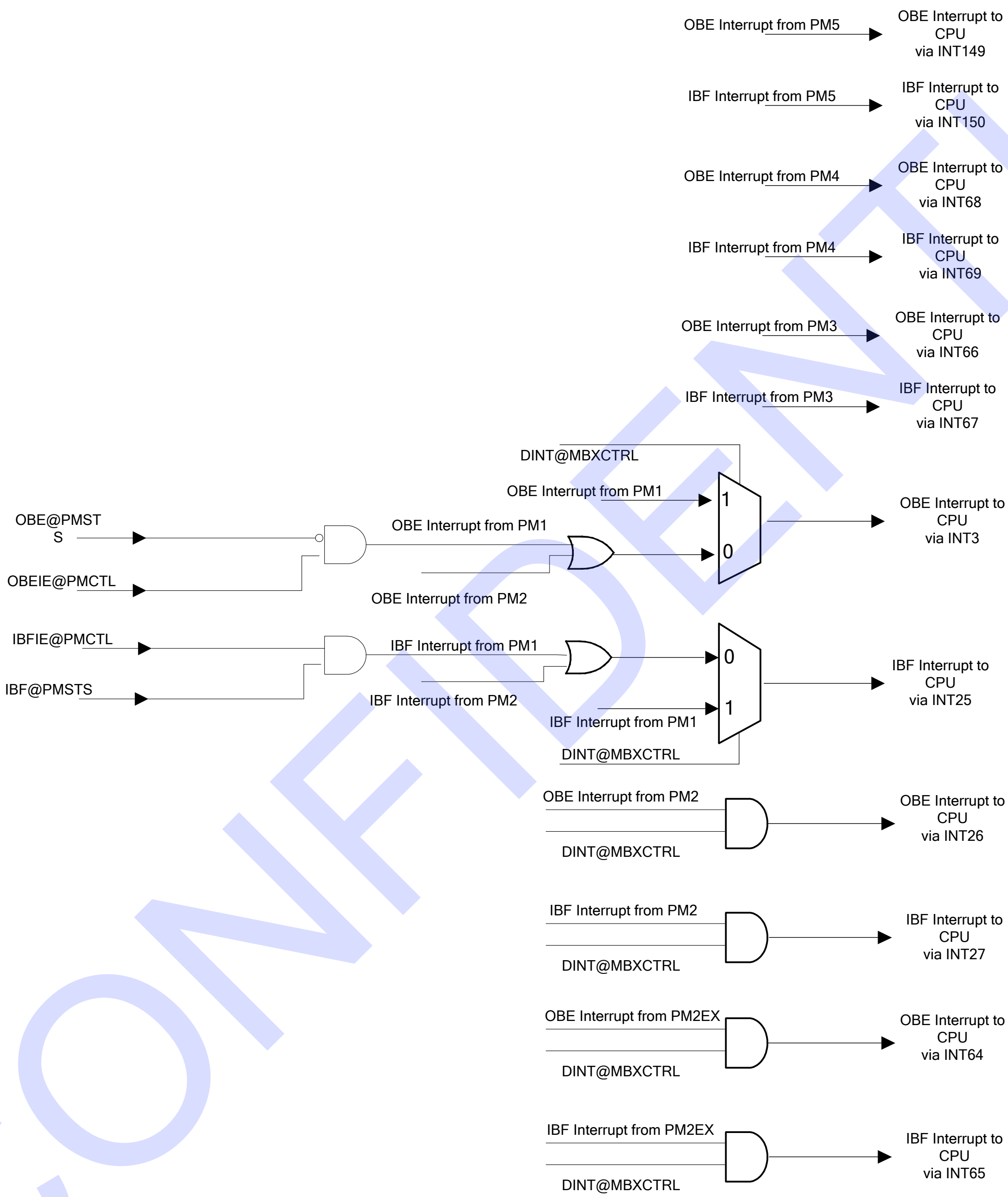


EC Interrupts

Two interrupts (IBF and OBF) are connected to INTC. These interrupts are enabled by OBEIE and IBFIE in PMnCTL register respectively.

The diagram of PMC interrupt to EC CPU via INT3/INT25/INT26/INT27/INT64-INT69/INT149/INT150 of INTC is show below.

Figure 6-29. EC Interrupt Request for PMC



Host Interrupt

The EC can select to access to different address space to generate IRQ, SMI# or SCI# interrupt when either IBF or OBF is set.

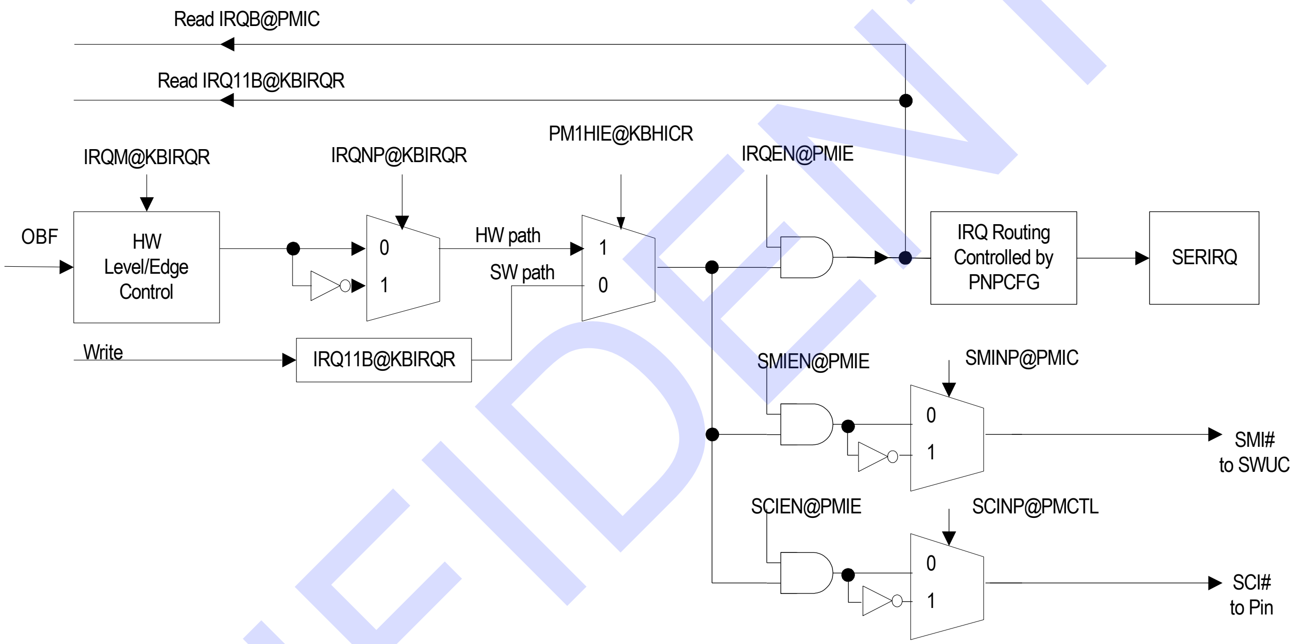
The IRQ numbers of PMC are programmable and use IRQ11 as the abbreviation in the following section. The abbreviation, n, represents channel 1 and/or channel 2 of this register.

6.7.3.2 Compatible Mode

When IRQ numbers in host configuration register are assigned by host software, the interrupt can be generated either by hardware via PM1HIE in KBHICR register or by programming KBIRQR register. In Normal Polarity mode (IRQNP in KBIRQR register is cleared), IT81202 supports legacy level for PM compatible mode interrupt. When a level interrupt is selected (IRQM in KBIRQR register is cleared), the interrupt signal is asserted when the OBF flag has been set, which is still asserted until the output buffer is read (i.e.,OBF flag is cleared). The EC can control the interrupts generated by the PM channel to the one as the following:
IRQ signal to LPC/SERIRQ, when IRQEN bit in PMnIE register is set.
SMI# output to SWUC, when SMIEN bit in PMnIE register is set.
SCI# signal, using the SCI# output, when SCIEN bit in PMnIE register is set.

The IRQ/SCI#/SMI# control diagram in PMC compatible mode is shown below.

Figure 6-30. IRQ/SCI#/SMI# Control in PMC Compatible Mode



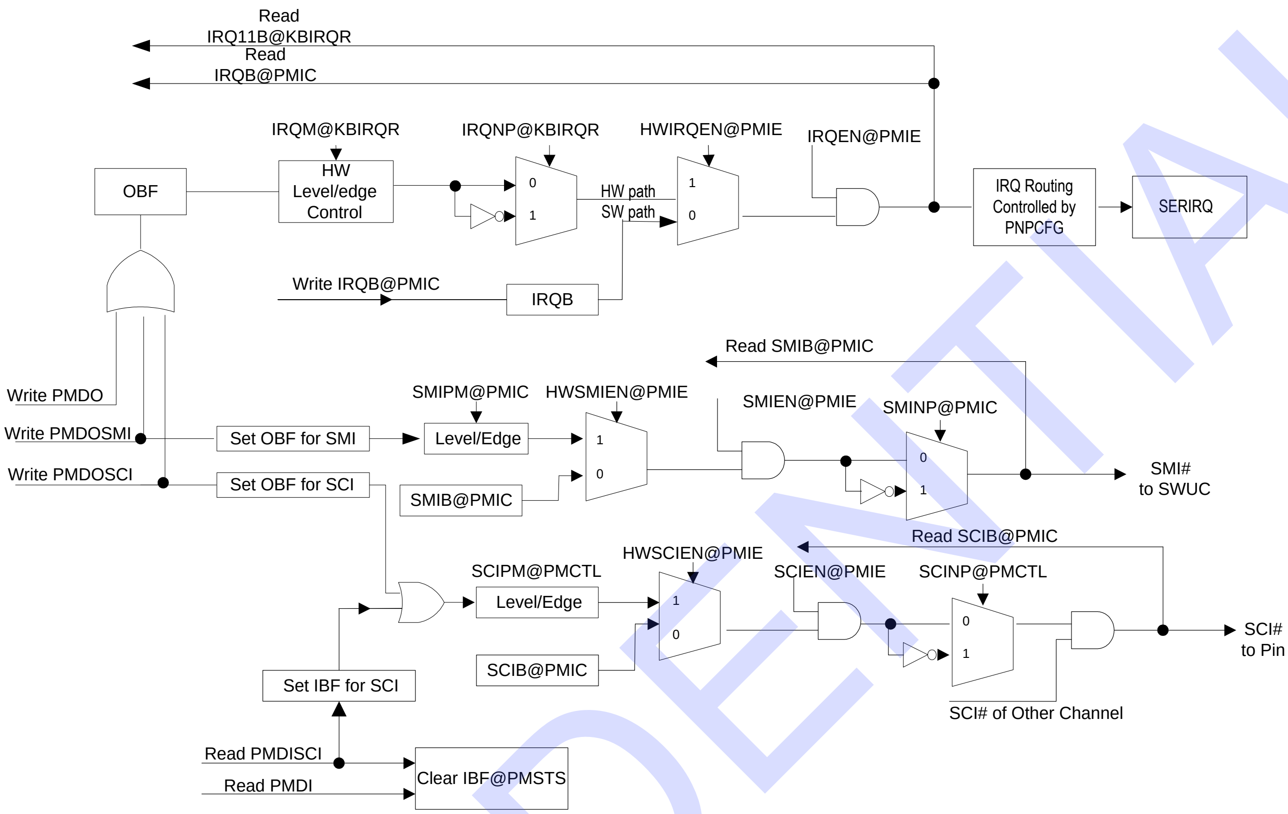
6.7.3.3 Enhanced PM mode

Enhanced PM mode is activated when APM is set to 1 in PMnCTL register. The generated IRQ, SMI# or SCI# interrupt can be selected to output via software control or hardware, which is determined by programming IRQEN bit in PMnIE register. SCI# and SMI# are generated when EC writes to the Data output buffer. SCI# is generated when EC reads the Data Input buffer. Different data register generates different interrupt. The OBF flag in PMnSTS register is set and both SMI# and SCI# interrupts are deasserted when data is written to PMnDO register. The OBF interrupt of SMI# is generated when PMnDOSMI register is written into data. The internal OBF flag of SMI# is cleared when OBF flag is cleared. The OBF interrupt of SCI# is generated When PMnDOSCI register is written into data.OBF_SCI# which is cleared when OBF is cleared.

The IBF flag is cleared and SCI# interrupt is generated when PMnDISCI register is read out data. The IBF flag is cleared and SCI# interrupt is not asserted when PMnDI register is read out data.

The IRQ/SCI#/SMI# control diagram in PMC enhanced mode is shown below.

Figure 6-31. IRQ/SCI#/SMI# Control in PMC Enhanced Mode



6.7.3.4 PMC2EX

There is a channel 2 extended (PMC2EX) mailbox (MBX) function based on PMC channel 2, which is constructed by a 16-byte mailbox shared with BRAM. See also Figure 7-23 on page 458.

This 16-byte mailbox can be accessed from both the EC side (named MBXEC0-15) and host side (MBXH0-15). In the EC side, MBXEC0-15 is always located in PMC module offset F0h-FFh and shared with the topmost 16-byte in BRAM.
In the host side, MBXH0-15 address is based on the descriptor 2 of Power Management I/F Channel 2 logic device inside LPC I/O space. (Refer to section 6.3.11.6 and 6.3.11.7 on page 97)

The PMC2EX (channel 2 extended) shares the same interrupt generation resource and registers (offset 10h-18h).

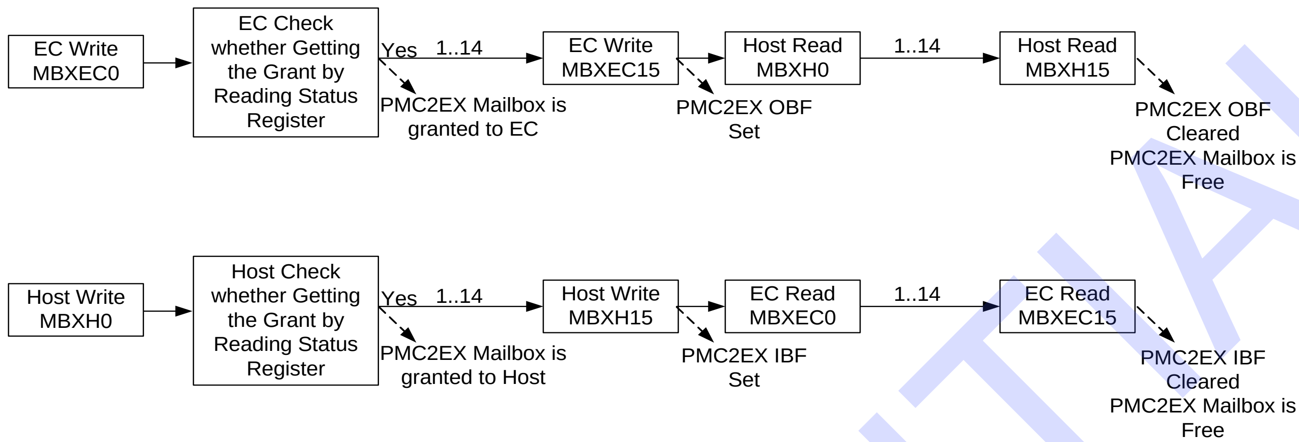
For registers, PMC2EX shares the same regi
sters (offset 10h-18h) and has its dedicated MBXCTRL register (offset 19h).

For interrupt generation, PMC2EX shares the same interrupt logic with channel 2. If MBXEN is set, IBF/OBF interrupt source of PMC2EX is ORed with channel 2.

The EC/host side should check whether to get the grant from the internal arbiter after writing to MBXEC0/MBXH0 (respectively).

The typical PMC2EX mailbox operation is described below.

Figure 6-32. Typical PMC2EX Mailbox Operation

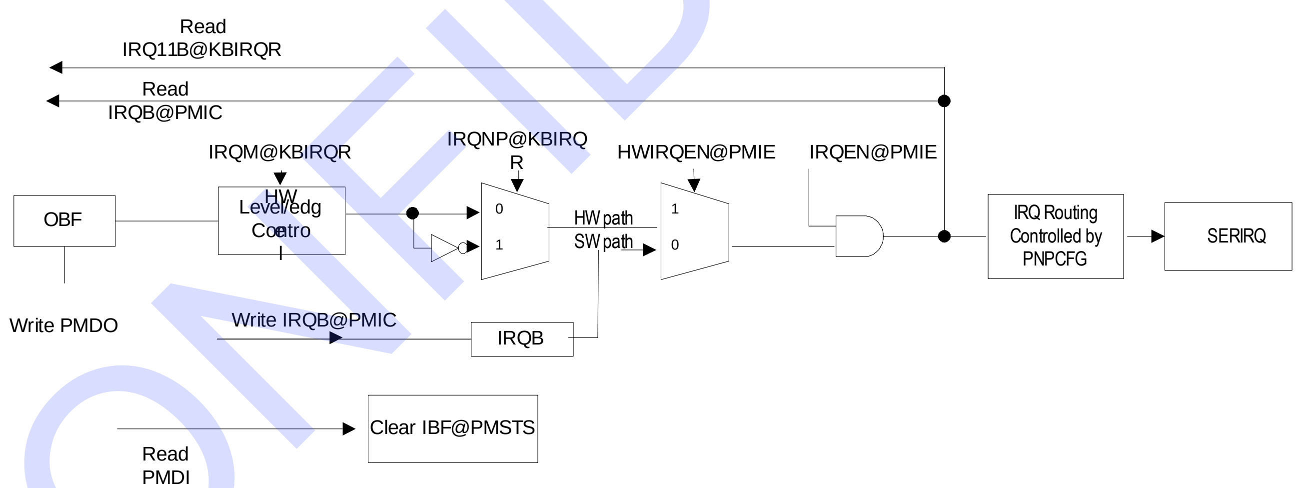


6.7.3.5 PMC3/4/5

Only Enhanced PM mode is activated in PM channel 3/4/5 and only IRQ interrupt is generated. The generated IRQ interrupt can be selected to output via software control or hardware, which is determined by programming IRQEN bit in PM3IE/PM4IE/PM5IE register.The OBF flag in PM3STS/PM4STS/PM5STS register is set when data is written to PM3DO/PM4DO/PM5DO register. The IBF flag is cleared when PMnDI register is read out data.

The IRQ control diagram in PMC3/PMC4/PMC5 is shown below.

Figure 6-33. IRQ Control in PM Channel 3/4/5



6.7.4 Host Interface Registers

The registers of PMC can be divided into two parts, Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. The PMC Channel 1 and 2 reside at LPC I/O space and the base address can be configured through LPC PNPCFG registers. For compatibility issue, the two I/O Port Base Addresses of channel 1 are suggested to configure at 62h and 66h.

These registers are listed below.

Table 6-34. Host View Register Map, PMC

7 ... 0	Offset
PMC Data Input Register (PMDIR)	Legacy 62h
PMC Data Output Register (PMDOR)	Legacy 62h
PMC Command Register (PMCMDR)	Legacy 66h
PMC Status Register (PMSTR)	Legacy 66h

Legacy 62h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 66h represents (I/O Port Base Address 1) + (Offset 0h)
See also Table 6-7 on page 73.

6.7.4.1 PMC Data Input Register (PMDIR)

Address Offset: 00h for I/O Port Base Address 0, Legacy 62h for Channel 1

Bit	R/W	Default	Description
7-0	W	00h	**Data Input Register Bit [7:0] (DIRB)** This is the data input register for power management channel data communication between the host and EC side. When the host writes this port, data is written to PMDIR register and EC CPU can read it. Notice that when the Command/Status register is written, the data is also stored into PMDIR register. Users must read A2 to decide whether the PMDIR data is data or command.

6.7.4.2 PMC Data Output Register (PMDOR)

Address Offset: 00h for I/O Port Base Address 0, Legacy 62h for Channel 1

Bit	R/W	Default	Description
7-0	R	00h	**Data Output Register Bit [7:0] (DORB)** This is the data output register for power management channel data communication between the host and EC. When the host reads this port, data is read from PMDOR register and EC CPU can write it.

6.7.4.3 PMC Command Register (PMCMDR)

Address Offset: 00h for I/O Port Base Address 1, Legacy 66h for Channel 1

Bit	R/W	Default	Description
7-0	W	00h	**Command Register Bit [7:0] (CRB)** The port is written by the host when A2 = 1 in PMSTR register.

6.7.4.4 Status Register (PMSTR)

Address Offset: 00h for I/O Port Base Address 1, Legacy 66h for Channel 1

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 1 and channel 2 with MBXEN cleared: This is a general purpose flag used for signaling between the host and EC side. When used as ACPI PM channel, the predefined meaning is burst, SCI# event and SMI# event. For channel 2 with MBXEN set: Bit 7: IBF of PMC channel 2 extended (PMC2EX) Bit 6: OBF of PMC channel 2 extended (PMC2EX) Bits 5-4: 00b: PMC2EX mailbox is not granted to both sides. 01b: PMC2EX mailbox is granted to the EC side. 10b: PMC2EX mailbox is granted to the host side. 11b: Reserved
3	R	0b	**A2 (A2)** This bit is used to indicate the last written (by host) address bit A2. If the bit is 0, it represents that what is written by the host is data. If this bit is 1, it represents that what is written by the host is command.
2	R/W	0b	**General Purpose flag (GPF)** This bit is used as a general-purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data input register or command register and is cleared when the EC CPU reads the data input register. Notice that the write to data input register or command register by the host all trigger this flag and EC must use A2 to distinguish whether the write is a command or data.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes the data output port and is cleared when the host reads the data out buffer.

6.7.5 EC Interface Registers

The registers of PMC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the EC interface. The EC interface can only be accessed by the internal processor. The base address is 1500h.

These registers are listed below.

Table 6-35. EC View Register Map, PMC

7 0	Offset
Host Interface PM Channel 1 Status (PM1STS)	00h
Host Interface PM Channel 1 Data Out Port (PM1DO)	01h
Host Interface PM Channel 1 Data Out Port with SCI# (PM1DOSCI)	02h
Host Interface PM Channel 1 Data Out Port with SMI# (PM1DOSMI)	03h
Host Interface PM Channel 1 Data In Port (PM1DI)	04h
Host Interface PM Channel 1 Data In Port with SCI# (PM1DISCI)	05h
Host Interface PM Channel 1 Control (PM1CTL)	06h
Host Interface PM Channel 1 Interrupt Control (PM1IC)	07h
Host Interface PM Channel 1 Interrupt Enable (PM1IE)	08h

7 ... 0	Offset
Host Interface PM Channel 2 Status (PM2STS)	10h
Host Interface PM Channel 2 Data Out Port (PM2DO)	11h
Host Interface PM Channel 2 Data Out Port with SCI# (PM2DOSCI)	12h
Host Interface PM Channel 2 Data Out Port with SMI# (PM2DOSMI)	13h
Host Interface PM Channel 2 Data In Port (PM2DI)	14h
Host Interface PM Channel 2 Data In Port with SCI# (PM2DISCI)	15h
Host Interface PM Channel 2 Control (PM2CTL)	16h
Host Interface PM Channel 2 Interrupt Control (PM2IC)	17h
Host Interface PM Channel 2 Interrupt Enable (PM2IE)	18h
Mailbox Control (MBXCTRL)	19h
Host Interface PM Channel 3 Status (PM3STS)	20h
Host Interface PM Channel 3 Data Out Port (PM3DO)	21h
Host Interface PM Channel 3 Data In Port (PM3DI)	22h
Host Interface PM Channel 3 Control (PM3CTL)	23h
Host Interface PM Channel 3 Interrupt Control (PM3IC)	24h
Host Interface PM Channel 3 Interrupt Enable (PM3IE)	25h
Host Interface PM Channel 4 Status (PM4STS)	30h
Host Interface PM Channel 4 Data Out Port (PM4DO)	31h
Host Interface PM Channel 4 Data In Port (PM4DI)	32h
Host Interface PM Channel 4 Control (PM4CTL)	33h
Host Interface PM Channel 4 Interrupt Control (PM4IC)	34h
Host Interface PM Channel 4 Interrupt Enable (PM4IE)	35h
Host Interface PM Channel 5 Status (PM5STS)	40h
Host Interface PM Channel 5 Data Out Port (PM5DO)	41h
Host Interface PM Channel 5 Data In Port (PM5DI)	42h
Host Interface PM Channel 5 Control (PM5CTL)	43h
Host Interface PM Channel 5 Interrupt Control (PM5IC)	44h
Host Interface PM Channel 5 Interrupt Enable (PM5IE)	45h
16-byte PMC2EX Mailbox 0 (MBXEC0)	F0h
…	…
16-byte PMC2EX Mailbox 15 (MBXEC15)	FFh

6.7.5.1 PM Status Register (PMSTS)

This register is the same as the Status register in host side but reside in the EC side.

Address Offset: 00h/10h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 1 and channel 2 with MBXEN cleared: This is a general-purpose flag used for signaling between the host and EC. When used as ACPI PM channel, the predefined meaning is burst, SCI# event and SMI# event. For channel 2 with MBXEN set: Bit 7: IBF of PMC channel 2 extended (PMC2EX) Bit 6: OBF of PMC channel 2 extended (PMC2EX) Bits 5-4: 00b: PMC2EX mailbox is not granted to both sides. 01b: PMC2EX mailbox is granted to the EC side. 10b: PMC2EX mailbox is granted to the host side. 11b: Reserved

Bit	R/W	Default	Description
3	R	0b	**A2 (A2)** This bit is used to indicate the last written (by host) address bit A2. If the bit is 0, it represents that what is written to the data port is data. If this bit is 1, it represents that what is written to the data port is command.
2	R/W	0b	**General Purpose Flag (GPF)** This bit is used as a general-purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data port or command port whereas cleared when the EC read the data in the buffer.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes data port whereascleared when the host reads the data output buffer.

6.7.5.2 PM Data Out Port (PMDO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 01h/11h

Bit	R/W	Default	Description
7-0	W	00h	**PM Data Out (PMDO[7:0])** This is the data output buffer.

6.7.5.3 PM Data Out Port with SCI# (PMDOSCI)

This register is the PMDOR buffer with SCI#. The data written to this register is stored in PMDOR. SCI# is generated upon write.

Address Offset: 02h/12h

Bit	R/W	Default	Description
7-0	W	00h	**PM Data Out with SCI# (PMDOSCI[7:0])** This is the data output buffer with SCI#. Writing to this port will generate hardware SCI# if enabled.

6.7.5.4 PM Data Out Port with SMI# (PMDOSMI)

This register is the PMDOR buffer with SMI#. The data written to this register is stored in PMDOR. SMI# is generated upon write.

Address Offset: 03h/13h

Bit	R/W	Default	Description
7-0	W	00h	**PM Data Out with SMI# (PMDOSMI[7:0])** This is the data output buffer with SMI#. Writing to this port will generate hardware SMI# if enabled.

6.7.5.5 PM Data In Port (PMDI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer.

Address Offset: 04h/14h

Bit	R/W	Default	Description
7-0	R	00h	**PM Data In (PMDI[7:0])** This is the data input buffer.

6.7.5.6 PM Data In Port with SCI# (PMDISCI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer. Reading this register (EC) generates SCI#.

Address Offset: 05h/15h

Bit	R/W	Default	Description
7-0	R	00h	**PM Data In with SCI# (PMDISCI[7:0])** This is the data input buffer with SCI#. Reading this port will generate SCI# when enabled.

6.7.5.7 PM Control (PMCTL)

Address Offset: 06h/16h

Bit	R/W	Default	Description
7	R/W	0b	**Enhance PM Mode (APM)** Setting this bit to ‘1’ enables the enhance PM mode. The interrupts (IRQ, SCI# or SMI#) are automatically generated by hardware operations if enabled.
6	R/W	1b	**SCI# Negative Polarity (SCINP)** Setting this bit to ‘1’ causes the SCI# polarity inversed (low active).
5-3	R/W	0h	**SCI# Pulse Mode (SCIPM[2:0])** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and a positive pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from IRQM field in KBIRQR register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Others: Reserved
2	-	0b	**Reserved**
1	R/W	0b	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to ‘1’ enables the EC interrupt generation when the output buffer full flag is cleared (by host reading the data port).

Bit	R/W	Default	Description
0	R/W	0b	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to ‘1’ enables the EC interrupt generation when the input buffer full flag is set (by host writing the data port or command port).

6.7.5.8 PM Interrupt Control (PMIC)

Address Offset: 07h/17h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6	R/W	1b	**SMI# Negative Polarity (SMINP)** Setting this bit to ‘1’ causes the SMI# polarity inversed.
5-3	R/W	000b	**SMI# Pulse Mode (SMIPM[2:0])** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and a positive pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from IRQM field in KBIRQR register. 000b: Level-triggered mode. 001b: Edge-triggered mode with 1-cycle pulse width. 010b: Edge-triggered mode with 2-cycle pulse width. 011b: Edge-triggered mode with 4-cycle pulse width. 100b: Edge-triggered mode with 8-cycle pulse width. 101b: Edge-triggered mode with 16-cycle pulse width. Others: Reserved
2	R/W	0b	**Host SCI# Control Bit (SCIB)** This bit is the SCI# generation bit when hardware SCI# is disabled. Read always returns the current value of SCI#.
1	R/W	0b	**Host SMI# Control Bit (SMIB)** This bit is the SMI# generation bit when hardware SMI# is disabled. Read always returns the current value of SMI#.
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.7.5.9 PM Interrupt Enable (PMIE)

Address Offset: 08h/18h

Bit	R/W	Default	Description
7	W	-	**Clear Input Buffer Full (CIBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC1/PMC2 IBF.
6	W	-	**Clear Output Buffer Full (COBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC1/PMC2 OBF.
5	R/W	0b	**Hardware SMI# Enable (HWSMIEN)** Setting this bit to ‘1’ enables the SMI# generated by hardware control. Writing to the SMIB bit generates the SMI# if this bit is set to ‘0’.

Bit	R/W	Default	Description
4	R/W	0b	**Hardware SCI# Enable (HWSCIEN)** Setting this bit to '1' enables the SCI# generated by hardware control. Writing to the SCIB bit generates the SCI# if this bit is set to '0'.
3	R/W	0b	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to '1' enables the IRQ generated by hardware control. Writing to the IRQB bit generates the IRQ if this bit is set to '0'.
2	R/W	0b	**SMI# Enable (SMIEN)** Setting this bit to '1' enables the SMI# generated by this module.
1	R/W	0b	**SCI# Enable (SCIEN)** Setting this bit to '1' enables the SCI# generated by this module.
0	R/W	0b	**IRQ Enable (IRQEN)** Setting this bit to '1' enables the IRQ generated by this module.

6.7.5.10 Mailbox Control (MBXCTRL)

Address Offset: 19h

Bit	R/W	Default	Description
7	R/W	0b	**Mailbox Enable (MBXEN)** 1b: Enable 16-byte PMC2EX mailbox 0b: Otherwise
6	-	-	**Reserved**
5	R/W	0b	**Dedicated Interrupt (DINT)** 0b: INT3: PMC Output Buffer Empty Int INT25: PMC Input Buffer Full Int 1b: INT3: PMC1 Output Buffer Empty Int INT25: PMC1 Input Buffer Full Int INT26: PMC2 Output Buffer Empty Int INT27: PMC2 Input Buffer Full Int (All are High Level Trig)
4-0	-	-	**Reserved**

6.7.5.11 PMC3 Status Register (PM3STS)

This register is the same as the Status register in host side but resides in the EC side.

Address Offset: 20h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 3: This is a general-purpose flag used for signaling between the host and EC.
3	R	0b	**A2 (A2)** This bit is used to indicate the last written (by host) address bit A2. If the bit is 0, it represents what is written to the data port is data. If this bit is 1, it represents what is written to the data port is command.
2	R/W	0b	**General Purpose Flag (GPF)** This bit is used as a general purpose flag.

Bit	R/W	Default	Description
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data port or command port whereas cleared when the EC read the data in the buffer.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes data port whereas cleared when the host reads the data output buffer.

6.7.5.12 PMC3 Data Out Port (PM3DO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 21h

Bit	R/W	Default	Description
7-0	W	00h	**PM 3 Data Out (PM3DO[7:0])** This is the data output buffer.

6.7.5.13 PMC3 Data In Port (PM3DI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer.

Address Offset: 22h

Bit	R/W	Default	Description
7-0	R	00h	**PMC3 Data In (PM3DI[7:0])** This is the data input buffer.

6.7.5.14 PMC3 Control (PM3CTL)

Address Offset: 23h

Bit	R/W	Default	Description
7-2	-	0b	**Reserved**
1	R/W	0b	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to '1' enables the EC interrupt generation when the output buffer full flag is cleared (by host reading the data port).
0	R/W	0b	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to '1' enables the EC interrupt generation when the input buffer full flag is set (by host writing the data port or command port).

6.7.5.15 PMC3 Interrupt Control (PM3IC)

Address Offset: 24h

Bit	R/W	Default	Description
7-1	-	0b	**Reserved**
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.7.5.16 PMC3 Interrupt Enable (PM3IE)

Address Offset: 25h

Bit	R/W	Default	Description
7	W	-	**Clear Input Buffer Full (CIBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC3 IBF.
6	W	-	**Clear Output Buffer Full (COBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC3 OBF.
5-4	-	00b	**Reserved**
3	R/W	0b	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to '1' enables the IRQ generated by hardware control. Writing data to the IRQB bit generates the IRQ if this bit is set to '0'.
2-1	-	0b	**Reserved**
0	R/W	0b	**IRQ Enable (IRQEN)** Setting this bit to '1' enables the IRQ generated by this module.

6.7.5.17 PMC4 Status Register (PM4STS)

This register is the same as the Status register in the host side but resides in the EC side.

Address Offset: 30h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 4: This is a general-purpose flag used for signaling between the host and EC.
3	R	0b	**A2 (A2)** This bit is used to indicate the last written (by host) address bit A2. If the bit is 0, it represents what is written to the data port is data. If this bit is 1, it represents what is written to the data port is command.
2	R/W	0b	**General Purpose Flag (GPF)** This bit is used as a general purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes the data port or command port whereas cleared when the EC reads the data in the buffer.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes the data port whereas cleared when the host reads the data output buffer.

6.7.5.18 PMC4 Data Out Port (PM4DO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 31h

Bit	R/W	Default	Description
7-0	W	00h	**PM 4 Data Out (PM4DO[7:0])** This is the data output buffer.

6.7.5.19 PMC4 Data In Port (PM4DI)

This register is the PMDIR buffer. The written data or command by the host is stored in this buffer.

Address Offset: 32h

Bit	R/W	Default	Description
7-0	R	00h	**PMC4 Data In (PM4DI[7:0])** This is the data input buffer.

6.7.5.20 PMC4 Control (PM4CTL)

Address Offset: 33h

Bit	R/W	Default	Description
7-2	-	0b	**Reserved**
1	R/W	0b	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to ‘1’ enables the EC interrupt generation when the output buffer full flag is cleared (by host’s reading the data port).
0	R/W	0b	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to ‘1’ enables the EC interrupt generation when the input buffer full flag is set (by host’s writing the data port or command port).

6.7.5.21 PMC4 Interrupt Control (PM4IC)

Address Offset: 34h

Bit	R/W	Default	Description
7-1	-	0b	**Reserved**
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.7.5.22 PMC4 Interrupt Enable (PM4IE)

Address Offset: 35h

Bit	R/W	Default	Description
7	W	-	**Clear Input Buffer Full (CIBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC4 IBF.
6	W	-	**Clear Output Buffer Full (COBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC4 OBF.
5-4	-	00b	**Reserved**
3	R/W	0b	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to ‘1’ enables the IRQ generated by hardware control. Writing data to the IRQB bit generates the IRQ if this bit is set to ‘0’.
2-1	-	0b	**Reserved**
0	R/W	0b	**IRQ Enable (IRQEN)** Setting this bit to ‘1’ enables the IRQ generated by this module.

6.7.5.23 PMC5 Status Register (PM5STS)

This register is the same as the Status register in the host side but resides in the EC side.

Address Offset: 40h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 5: This is a general-purpose flag used for signaling between the host and EC.
3	R	0b	**A2 (A2)** This bit is used to indicate the last written (by host) address bit A2. If the bit is 0, it represents what is written to the data port is data. If this bit is 1, it represents what is written to the data port is command.
2	R/W	0b	**General Purpose Flag (GPF)** This bit is used as a general purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes the data port or command port whereas cleared when the EC reads the data in the buffer.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes the data port whereas cleared when the host reads the data output buffer.

6.7.5.24 PMC5 Data Out Port (PM5DO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 41h

Bit	R/W	Default	Description
7-0	W	00h	**PM 5 Data Out (PM5DO[7:0])** This is the data output buffer.

6.7.5.25 PMC5 Data In Port (PM5DI)

This register is the PMDIR buffer. The written data or command by the host is stored in this buffer.

Address Offset: 42h

Bit	R/W	Default	Description
7-0	R	00h	**PMC5 Data In (PM5DI[7:0])** This is the data input buffer.

6.7.5.26 PMC5 Control (PM5CTL)

Address Offset: 43h

Bit	R/W	Default	Description
7-2	-	0b	**Reserved**
1	R/W	0b	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to ‘1’ enables the EC interrupt generation when the output buffer full flag is cleared (by host’s reading the data port).
0	R/W	0b	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to ‘1’ enables the EC interrupt generation when the input buffer full flag is set (by host’s writing the data port or command port).

6.7.5.27 PMC5 Interrupt Control (PM5IC)

Address Offset: 44h

Bit	R/W	Default	Description
7-1	-	0b	**Reserved**
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.7.5.28 PMC5 Interrupt Enable (PM5IE)

Address Offset: 45h

Bit	R/W	Default	Description
7	W	-	**Clear Input Buffer Full (CIBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC5 IBF.
6	W	-	**Clear Output Buffer Full (COBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC5 OBF.
5-4	-	00b	**Reserved**
3	R/W	0b	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to ‘1’ enables the IRQ generated by hardware control. Writing data to the IRQB bit generates the IRQ if this bit is set to ‘0’.
2-1	-	0b	**Reserved**
0	R/W	0b	**IRQ Enable (IRQEN)** Setting this bit to ‘1’ enables the IRQ generated by this module.

6.7.5.29 16-byte PMC2EX Mailbox 0-15 (MBXEC0-15)

Address Offset: F0h-FFh

Bit	R/W	Default	Description
7-0	R/W	-	**Mailbox Byte Content** This byte is the 16-byte PMC2EX mailbox in the EC side.

6.8 Serial Peripheral Interface (SSPI) in Host Domain

6.8.1 Overview

SSPI module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 7.17 Serial Peripheral Interface (SSPI) for the EC domain function description on page 461.

SSPI can be accessed by the software in the host or EC side; however, the SSPI function should be controlled by a side only. See also section 7.15.4.11 Reset Control DMM (RSTDMMC) on page 431 and section 7.7.3.5 Auto Clock Gating (AUTOCG) on page 263.

6.9 Platform Environment Control Interface (PECI) in Host Domain

6.9.1 Overview

PECI module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 7.10 on page 344 for the EC domain function description.

PECI can be accessed by the software in the host or EC side; however, the PECI function should be controlled by a side only. See also section 7.15.4.11 Reset Control DMM (RSTDMMC) on page 431.

6.10 Serial Port 1/2 (UART1/UART2) in Host Domain

6.10.1 Overview

UART1 module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 7.19 Serial Port (UART) on page 481 for the EC domain function description.

UART1 can be accessed by the software in the host or EC side; however, the UART1 function should be controlled by a side only. See also section 7.15.4.11 Reset Control DMM (RSTDMMC) on page 431 and section 7.7.3.5 Auto Clock Gating (AUTOCG) on page 263.

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7. EC Domain Functions

7.1 32-bit Embedded Controller (EC)

7.1.1 Overview

The embedded 32-bit controller is a low-power and small-sized micro processor which is fully compliant with RISC-V RV32I instruction set and MAFC extensions.

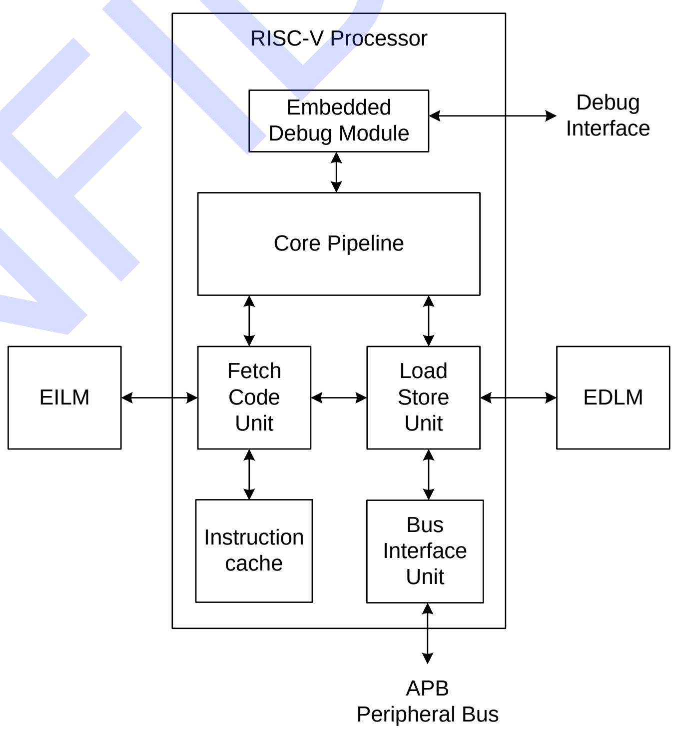
7.1.2 Features

- RISC-V RV32I architecture
- 5-stage pipeline
- 4KB instruction cache
- “M” standard extension for integer multiplication and division
- “A” standard extension for atomic instructions
- “F” standard extension for single-precision floating-point
- “C” standard extension for compressed instructions

7.1.3 General Description

The RISC-V compliant core is a low-power and small-sized RV32I architecture micro-processor with 4KB instruction and is able to run up to 96Mhz. With instruction-local-memory(ILM) and data-local-memory(DLM) interface, the processor can access to the code/data directly in one cycle without any bus latency and achieve the optimal performance against the core clock frequency. Besides, the processor also supports standard RISC-V JTAG debug interface to support on-system-debug.

Figure 7-1. RISC-V Processor Block Diagram



7.1.4 Functional Description

Memory

Local memory is for storing instructions and/or data that might be accessed frequently in a system such as interrupt service routine, system call, sensor fusion data, etc. The processor supports load memories through its external local memory interfaces. Both instruction local memory and data local memory are supported.

I/O ports

The processor has three types of bus interfaces, ILM, DLM and APB. For the instruaction access, the code is read first from the instruction cache if it misses, then it checks the ILM (Instruction Local Memory) controlled by the memory management unit. If the issued address is not in the ILM range, it accesses the embedded flash to fetch the code. For the data access, the variables or DMA data are read/written from/to the DLM (Data Local Memory). All the EC side peripheral I/Os are accessed through the APB bus. All these 3 types of interfaces have 24-bit addressing capability.

Interrupts

An interruption is a control flow change of normal instruction execution generated by an Interrupt or an Exception. When an interruption happens, the processor stops processing the current flow of instructions, saves enough states for later resuming of the interrupted flow, disables interrupts, and starts executing a software interruption handler. In the RISC-V architecture, there are 3 types of interrupt – External, Timer, Software. All peripheral modules except the ETWD issue the interrupt by an external interrupt. The ETWD can issue an interrupt by the external or timer type.

Power Management

The RISC-V ISA provides a STANDBY instruction for the core to enter a reduced power mode. Once entering the reduced power mode, the CPU clock is fully gated-off. Only external interrupt events can wake up the CPU and restore the process routing.

Embedded Debug Module (EDM)

Embedded Debug Module (EDM) is a hardware module, which directly interfaces with the processor core, provides functionalities of the register access, memory access and hardware breakpoint to help users debug software on the target system. It uses a standard JTAG interface to connect the EC processor core and the external debug host.

7.2 Memory Controller

7.2.1 Overview

The memory controller is used to manage the system memory and handles the requests from CPU and pheripheral DMAs.

7.2.2 Features

- Total 60KB SRAM
- Configurable instruction-local-memory(ILM) size from 0KB~60KB
- Configurable data-local-memory(DLM) size from 0KB~60KB

7.2.3 General Description

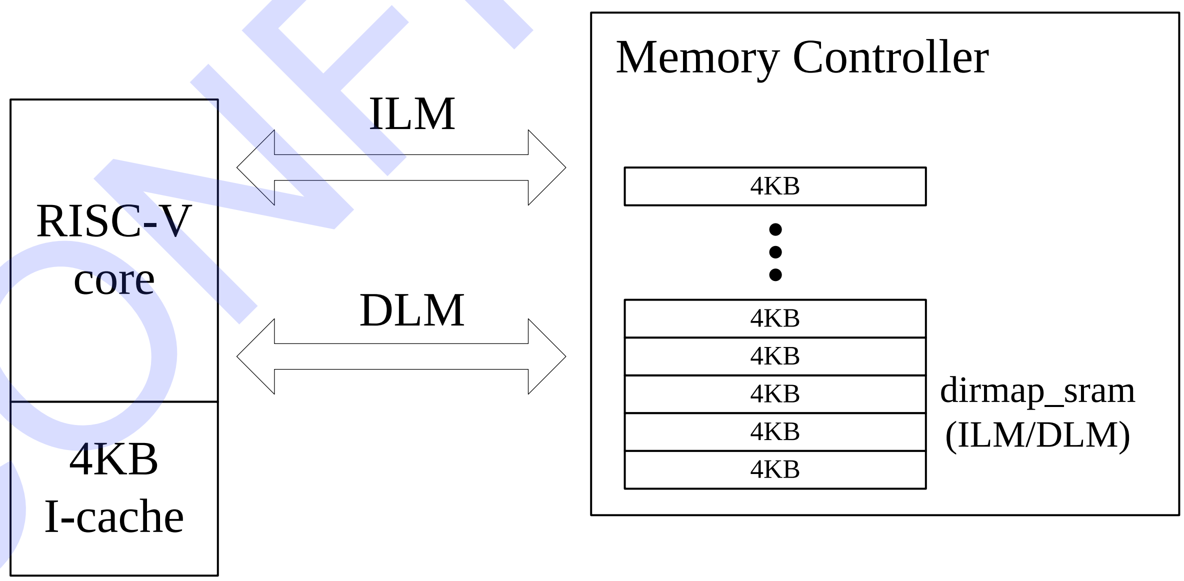
The memory controller is used to cache the code or store the data. The total SRAM size in the memory controller is 60k byte. The processor fetches code through the ILM bus and access data through the DLM bus from the memory controller. Figure 7-2 is a simple concept of the memory controller.

When the processor starts to fetch code through the ILM bus, the memory controller first checks whether the desired code is in dirmap_sram or not. If the code is avalible, the memory controller returns the code directly from dirmap_sram. If the code is missing, the memory controller starts the DMA cycle to load code from the embedded flash into the processor.

After the load code DMA cycle, the memory controller then returns the desired code to the processor. The time of the load code DMA cycle is the missing penalty time. It sacrifices the processor's fetch code performance.

The dirmap_sram can be configured to store the data, following the application. However, any dirmap_sram can only be configured as either data or code.

Figure 7-2. Memory Controller Block Diagram



7.3 Interrupt Controller (INTC)

7.3.1 Overview

INTC mainly collects several interrupts from modules. The performance of the interrupt-driven design is better than that of the polling-driven design.

External interrupts can wakeup CPU from Doze/Deep Doze/Sleep mode.

7.3.2 Features

- Configurable level-triggered and edge-triggered mode
- Configurable interrupt polarity of triggered mode
- Clears registers for edge-triggered interrupts
- Each interrupt source able to enabled/masked individually

7.3.3 Functional Description

7.3.3.1 Power Fail Interrupt

The INTC collects interrupt sources from internal. The detailed group information is listed in Table 7-2. INTC Interrupt Assignments.

To implement a power-fail application, connect GPB7 to external circuit. Firmware puts the GPB7 in alternative function, enables the Schmitt Trigger of GPB7 to receive an asynchronous external input, and generates an external interrupt event to CPU.

There are two methods to trap a power-fail event: “Trap Enabled” and “Trap Enabled and Locked”. Users select “Trap Enabled” by setting TREN bit in PFAILR and select “Trap Enabled and Locked” by setting TRENL bit in PFAILR. If both bits are selected, TREN bit is ignored. If “Trap Enabled” is used, power-fail event is detected by falling edge transition of PWRFAIL#, and an external interrupt to CPU is asserted. After the interrupt is set, TREN bit is cleared. “Trap Enabled and Locked” method is similar to “Trap Enabled” method but TRENL will not be cleared after the interrupt is set.

7.3.3.2 Programmable Interrupts

INTC also collects all maskable interrupt sources and make a request on EINT of CPU if triggered. Each channel can be individually enabled or masked by IERx. If an interrupt channel is masked and one interrupt request is triggered, the request is masked (inhibited, not canceled), and will be asserted on EINT if it is enabled.

The ISRx indicates the status of interrupt regardless of IERx. In the level-triggered mode, ISRx is affected by corresponding interrupt sources, and firmware should clear the interrupt status on interrupt sources after its request is handled. In the edge-triggered mode, ISRx is set by selected edge transition (determined by IELMRx) of corresponding interrupts sources, and firmware should write 1 to clear ISRx after this request is handled.

Firmware may use the AIVECT to determine which channel is to be serviced first or have its priority rule by reading ISRx and IERx. AIVECT treats INT1 as the lowest priority interrupt.

The CPU always wakes up from Doze/Deep Doze/Sleep mode when it detects an enabled external interrupt. Firmware should disable unwanted interrupt sources to prevent them from waking up unexpectedly.

Normally interrupts from WUC are high level-triggered. Note that interrupts from WUC are not always level-triggered interrupts since they may be just throughout WUC if the corresponding channels at WUC are disabled (bypassed). If an edge-triggered interrupt passes through WUC and INTC with WUC corresponding channel is disabled and INTC corresponding channel is level-triggered mode, it may cause CPU interrupt routine to be called but finds no interrupt source to service, or it may cause CPU to wake up from Doze/Deep

Doze/Sleep mode and enters interrupt routine but finds no interrupt source to service.

7.3.4 EC Interface Registers

The EC interface registers are listed below. The base address for INTC is 3F00h.

Table 7-1. EC View Register Map, INTC

7 0	Offset
Interrupt Status Register 0 (ISR0)	00h
Interrupt Status Register 1 (ISR1)	01h
Interrupt Status Register 2 (ISR2)	02h
Interrupt Status Register 3 (ISR3)	03h
Interrupt Status Register 4 (ISR4)	14h
Interrupt Status Register 5 (ISR5)	18h
Interrupt Status Register 6 (ISR6)	1Ch
Interrupt Status Register 7 (ISR7)	20h
Interrupt Status Register 8 (ISR8)	24h
Interrupt Status Register 9 (ISR9)	28h
Interrupt Status Register 10 (ISR10)	2Ch
Interrupt Status Register 11 (ISR11)	30h
Interrupt Status Register 12 (ISR12)	34h
Interrupt Status Register 13 (ISR13)	38h
Interrupt Status Register 14 (ISR14)	3Ch
Interrupt Status Register 15 (ISR15)	40h
Interrupt Status Register 16 (ISR16)	44h
Interrupt Status Register 17 (ISR17)	48h
Interrupt Status Register 18 (ISR18)	4Ch
Interrupt Status Register 19 (ISR19)	50h
Interrupt Status Register 20 (ISR20)	54h
Interrupt Status Register 21 (ISR21)	58h
Interrupt Status Register 22 (ISR22)	5Ch
Interrupt Status Register 23 (ISR23)	90h
Interrupt Enable Register 0 (IER0)	04h
Interrupt Enable Register 1 (IER1)	05h
Interrupt Enable Register 2 (IER2)	06h
Interrupt Enable Register 3 (IER3)	07h
Interrupt Enable Register 4 (IER4)	15h
Interrupt Enable Register 5 (IER5)	19h
Interrupt Enable Register 6 (IER6)	1Dh
Interrupt Enable Register 7 (IER7)	21h
Interrupt Enable Register 8 (IER8)	25h
Interrupt Enable Register 9 (IER9)	29h
Interrupt Enable Register 10 (IER10)	2Dh
Interrupt Enable Register 11 (IER11)	31h
Interrupt Enable Register 12 (IER12)	35h
Interrupt Enable Register 13 (IER13)	39h
Interrupt Enable Register 14 (IER14)	3Dh
Interrupt Enable Register 15 (IER15)	41h
Interrupt Enable Register 16 (IER16)	45h
Interrupt Enable Register 17 (IER17)	49h
Interrupt Enable Register 18 (IER18)	4Dh
Interrupt Enable Register 19 (IER19)	51h
Interrupt Enable Register 20 (IER20)	55h
Interrupt Enable Register 21 (IER21)	59h

7 0	Offset
Interrupt Enable Register 22 (IER22)	5Dh
Interrupt Enable Register 23 (IER23)	91h
Interrupt Edge/Level-Triggered Mode Register 0 (IELMR0)	08h
Interrupt Edge/Level-Triggered Mode Register 1 (IELMR1)	09h
Interrupt Edge/Level-Triggered Mode Register 2 (IELMR2)	0Ah
Interrupt Edge/Level-Triggered Mode Register 3 (IELMR3)	0Bh
Interrupt Edge/Level-Triggered Mode Register 4 (IELMR4)	16h
Interrupt Edge/Level-Triggered Mode Register 5 (IELMR5)	1Ah
Interrupt Edge/Level-Triggered Mode Register 6 (IELMR6)	1Eh
Interrupt Edge/Level-Triggered Mode Register 7 (IELMR7)	22h
Interrupt Edge/Level-Triggered Mode Register 8 (IELMR8)	26h
Interrupt Edge/Level-Triggered Mode Register 9 (IELMR9)	2Ah
Interrupt Edge/Level-Triggered Mode Register 10 (IELMR10)	2Eh
Interrupt Edge/Level-Triggered Mode Register 11 (IELMR11)	32h
Interrupt Edge/Level-Triggered Mode Register 12 (IELMR12)	36h
Interrupt Edge/Level-Triggered Mode Register 13 (IELMR13)	3Ah
Interrupt Edge/Level-Triggered Mode Register 14 (IELMR14)	3Eh
Interrupt Edge/Level-Triggered Mode Register 15 (IELMR15)	42h
Interrupt Edge/Level-Triggered Mode Register 16 (IELMR16)	46h
Interrupt Edge/Level-Triggered Mode Register 17 (IELMR17)	4Ah
Interrupt Edge/Level-Triggered Mode Register 18 (IELMR18)	4Eh
Interrupt Edge/Level-Triggered Mode Register 19 (IELMR19)	52h
Interrupt Edge/Level-Triggered Mode Register 20 (IELMR20)	56h
Interrupt Edge/Level-Triggered Mode Register 21 (IELMR21)	5Ah
Interrupt Edge/Level-Triggered Mode Register 22 (IELMR22)	5Eh
Interrupt Edge/Level-Triggered Mode Register 23 (IELMR23)	92h
Interrupt Polarity Register 0 (IPOLR0)	0Ch
Interrupt Polarity Register 1 (IPOLR1)	0Dh
Interrupt Polarity Register 2 (IPOLR2)	0Eh
Interrupt Polarity Register 3 (IPOLR3)	0Fh
Interrupt Polarity Register 4 (IPOLR4)	17h
Interrupt Polarity Register 5 (IPOLR5)	1Bh
Interrupt Polarity Register 6 (IPOLR6)	1Fh
Interrupt Polarity Register 7 (IPOLR7)	23h
Interrupt Polarity Register 8 (IPOLR8)	27h
Interrupt Polarity Register 9 (IPOLR9)	2Bh
Interrupt Polarity Register 10 (IPOLR10)	2Fh
Interrupt Polarity Register 11 (IPOLR11)	33h
Interrupt Polarity Register 12 (IPOLR12)	37h
Interrupt Polarity Register 13 (IPOLR13)	3Bh
Interrupt Polarity Register 14 (IPOLR14)	3Fh
Interrupt Polarity Register 15 (IPOLR15)	43h
Interrupt Polarity Register 16 (IPOLR16)	47h
Interrupt Polarity Register 17 (IPOLR17)	4Bh
Interrupt Polarity Register 18 (IPOLR18)	4Fh
Interrupt Polarity Register 19 (IPOLR19)	53h
Interrupt Polarity Register 20 (IPOLR20)	57h
Interrupt Polarity Register 21 (IPOLR21)	5Bh
Interrupt Polarity Register 22 (IPOLR22)	5Fh
Interrupt Polarity Register 23 (IPOLR23)	93h
All Interrupt Vector Register (AIVECT)	10h
Interrupt Control Register (ICR)	13h
Power Fail Status (PFAILS)	11h

7		0	Offset
Power Fail Register (PFAILR)			12h

7.3.4.1 Interrupt Status Register 0-23 (ISR0 - ISR23)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

ISR0 defined in Group 0
ISR1 defined in Group 1
ISR2 defined in Group 2
ISR3 defined in Group 3
ISR4 defined in Group 4
ISR5 defined in Group 5
ISR6 defined in Group 6
ISR7 defined in Group 7
ISR8 defined in Group 8
ISR9 defined in Group 9
ISR10 defined in Group 10
ISR11 defined in Group 11
ISR12 defined in Group 12
ISR13 defined in Group 13
ISR14 defined in Group 14
ISR15 defined in Group 15
ISR16 defined in Group 16
ISR17 defined in Group 17
ISR18 defined in Group 18
ISR19 defined in Group 19
ISR20 defined in Group 20
ISR21 defined in Group 21
ISR22 defined in Group 22
ISR23 defined in Group 23

Note: Where Group 0-23 (Refer to Table 7-2 on page 196).

Address Offset: 00h

Bit	R/W	Default	Description
7-1	R/WC Or R	-	**Interrupt Status Group 0 (ISGR0 7:1)** It indicates the interrupt input status of INTx. INTST7 to INTST1 correspond to INT7 to INT1 respectively. Each bit is R/WC if the corresponding bit in IELMRx register indicates edge-triggered mode, while R if it indicates level-triggered mode. For each bit: Read 0: Interrupt input to INTC is not pending. Read 1: Interrupt input to INTC is pending. For each bit: Write 0: No action Write 1: Clear this bit when it is in the edge-triggered mode, and writing 1 is ignored when it is in the level-triggered mode.
0	R	0b	**Reserved**

Address Offset: 01h, 02h, 03h, 14h, 18h, 1Ch, 20h, 24h, 28h, 2Ch, 30h, 34h, 38h, 3Ch, 40h, 44h, 48h, 4Ch, 50h, 54h, 58h, 5Ch, 90h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status Group x (ISGRx 7:0)** It indicates the interrupt input status of (INTn).(where n means 0 - 7 regardless of its corresponding Group x) The same as ISGR0 **Note**: Where x means (1 – 23)

7.3.4.2 Interrupt Enable Register 0-23 (IER0 - IER23)

IER0 defined in Group 0
IER1 defined in Group 1
IER2 defined in Group 2
IER3 defined in Group 3
IER4 defined in Group 4
IER5 defined in Group 5
IER6 defined in Group 6
IER7 defined in Group 7
IER8 defined in Group 8
IER9 defined in Group 9
IER10 defined in Group 10
IER11 defined in Group 11
IER12 defined in Group 12
IER13 defined in Group 13
IER14 defined in Group 14
IER15 defined in Group 15
IER16 defined in Group 16
IER17 defined in Group 17
IER18 defined in Group 18
IER19 defined in Group 19
IER20 defined in Group 20
IER21 defined in Group 21
IER22 defined in Group 22
IER23 defined in Group 23

Note: Where Group 0-23 (Refer to Table 7-2 on page 196)

Address Offset: 04h

Bit	R/W	Default	Description
7-1	R/W	0h	**Interrupt Enable Group 0 (IEGR0 7:1)** Each bit determines whether its corresponding interrupt channel (INT7-0) is masked or enabled. Note that it has no effect on INT0 0: Masked 1: Enabled
0	-	0b	**Reserved**

Address Offset: 05h, 06h, 07h, 15h, 19h, 1Dh, 21h, 25h, 29h, 2Dh, 31h, 35h, 39h, 3Dh, 41h, 45h, 49h, 4Dh, 51h, 55h, 59h, 5Dh, 91h

Bit	R/W	Default	Description
7-0	R/W	00h	**Interrupt Enable Group x (IEGRx 7:0)** Each bit determines whether its corresponding interrupt channel (INTn) is masked or enabled. (where n means 0 - 7 regardless of its corresponding Group x) 0: Masked 1: Enabled **Note**: Where x means (1 – 23)

7.3.4.3 Interrupt Edge/Level-Triggered Mode Register 0-23 (IELMR0 – IELMR23)

It determines whether its corresponding interrupt channel is level-triggered or edge-triggered.

IELMR0 defined in Group 0
IELMR1 defined in Group 1
IELMR2 defined in Group 2
IELMR3 defined in Group 3
IELMR4 defined in Group 4
IELMR5 defined in Group 5
IELMR6 defined in Group 6
IELMR7 defined in Group 7
IELMR8 defined in Group 8
IELMR9 defined in Group 9
IELMR10 defined in Group 10
IELMR11 defined in Group 11
IELMR12 defined in Group 12
IELMR13 defined in Group 13
IELMR14 defined in Group 14
IELMR15 defined in Group 15
IELMR16 defined in Group 16
IELMR17 defined in Group 17
IELMR18 defined in Group 18
IELMR19 defined in Group 19
IELMR20 defined in Group 20
IELMR21 defined in Group 21
IELMR22 defined in Group 22
IELMR23 defined in Group 23

Note: Where Group 0-28 (Refer to Table 7-2 on page 196)

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00000000b	**Interrupt Edge/Level-Triggered Mode Group 0 (IELMGR0 7:0)** Each bit determines the triggered mode of the corresponding interrupt channel (INT7-0). 0: Level-triggered 1: Edge-triggered Always write-1-clear to the corresponding bit in ISR register after modifying these bits if edge-triggered is selected.

Address Offset: 09h, 0Ah, 0Bh, 16h, 1Ah, 1Eh, 22h, 26h, 2Ah, 2Eh, 32h, 36h, 3Ah, 3Eh, 42h, 46h, 4Ah,

4Eh, 52h, 56h, 5Ah, 5Eh, 92h

Bit	R/W	Default	Description
7-0	R/W (only for IELMR 1-3) R (only for IELMR 4-23)	Refer to Table 7-2 on page 196	**Interrupt Edge/Level-Triggered Mode Group x (IELMGRx 7:0)** Each bit determines the triggered mode of the corresponding interrupt channel (INTn). (where n means 0 - 7 regardless of its corresponding Group x) The same as IELMGR0 **Note**: Where x means (1 – 23)

7.3.4.4 Interrupt Polarity Register 0-23 (IPOLR0 – IPOLR23)

For level-triggered interrupt, it determines this interrupt is level-high-triggered or level-low-triggered.
For edge-triggered interrupt, it determines this interrupt is rising-edge-triggered or falling-edge-triggered.

IPOLR0 defined in Group 0
IPOLR1 defined in Group 1
IPOLR2 defined in Group 2
IPOLR3 defined in Group 3
IPOLR4 defined in Group 4
IPOLR5 defined in Group 5
IPOLR6 defined in Group 6
IPOLR7 defined in Group 7
IPOLR8 defined in Group 8
IPOLR9 defined in Group 9
IPOLR10 defined in Group 10
IPOLR11 defined in Group 11
IPOLR12 defined in Group 12
IPOLR13 defined in Group 13
IPOLR14 defined in Group 14
IPOLR15 defined in Group 15
IPOLR16 defined in Group 16
IPOLR17 defined in Group 17
IPOLR18 defined in Group 18
IPOLR19 defined in Group 19
IPOLR20 defined in Group 20
IPOLR21 defined in Group 21
IPOLR22 defined in Group 22
IPOLR23 defined in Group 23

Note: Where Group 0-23 (Refer to Table 7-2 on page 196)

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Polarity Group 0 (IPOLGR0 7:0)** Each bit determines the active high/low of the corresponding interrupt channel (INT7-0). 0: Level-high-triggered or rising-edge-triggered 1: Level-low-triggered or falling-edge-triggered Always write-1-clear to the corresponding bit in ISR register after modifying these bits if edge-triggered is selected.

Address Offset: 0Dh, 0Eh, 0Fh, 17h, 1Bh, 1Fh, 23h, 27h, 2Bh, 2Fh, 33h, 37h, 3Bh, 3Fh, 43h, 47h, 4Bh, 4Fh, 53h, 57h, 5Bh, 5Fh, 93h

Bit	R/W	Default	Description
7-0	R/W (only for IPOLR 1-3) R (only for IPOLR 4-23)	0h	**Interrupt Polarity Group x (IPOLGRx 7:0)** Each bit determines the active high/low of the corresponding interrupt channel (INTn). (where n means 0 - 7 regardless of its corresponding Group x) The same as IPOLGR0 **Note**: Where x means (1 – 23)

7.3.4.5 All Interrupt Vector Register (AIVCT)

Address Offset: 10h

Bit	R/W	Default	Description
7-0	R	10h	**All Interrupt Vector (AIVECT)** It contains the interrupt number of all interrupt sources, and which is the highest priority, enabled and pending interrupt. The valid value ranges from 10h. Note that INT1 has the lowest priority. If no enabled interrupt is pending, it returns 10h.

7.3.4.6 Interrupt Control Register (ICR)

Address Offset: 13h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Interrupt Vector Toggle Mode (IVTM)** When toggle mode is enable, write 1 to the bits of IER will make interrupt enable be inversed; Write 0 to the bits of IER will not change the interrupt enable. 0b: Disable 1b: Enable toggle mode.

7.3.4.7 Power Fail Status (PFAILS)

PFAILSTS is set when falling edge transition of PWRFAIL# with TREN or TRENL bit in PFAILR is set, and it is cleared when being reset or read its content.

Address Offset: 11h

Bit	R/W	Default	Description
7-1	-	00h	**Reserved**
0	R	-	**PWRFAIL# from PWRFAIL# Status (PFAILSTS)** 0: The PWRFAIL# status is not asserted. 1: The PWRFAIL# status is asserted by a power-fail event.

7.3.4.8 Power Fail Register (PFAILR)

It provides two methods to trap the PWRFAIL# event.
This register can't be reset by WDT Reset.

Address Offset: 12h

Bit	R/W	Default	Description
7-3	-	00h	**Reserved**
2	R/W	0b	**PWRFAIL# Trap Enabled and Locked (TRENL)** Firmware sets this bit to enable the PWRFAIL# trap. When the trap is enabled, PFAILSTS bit in PFAILS will be set if the falling edge transition of PWRFAIL# is detected. This bit can't be cleared by writing 0 to it until being reset. 0: No PWRFAIL# trap 1: PWRFAIL# trap
1	R	-	**PWRFAIL# Status (PFAILST)** 0: PWRFAIL# is low (asserted) 1: PWRFAIL# is high (deasserted)
0	R/W	0b	**PWRFAIL# Trap Enabled (TREN)** Firmware sets this bit to enable the PWRFAIL# trap. When the trap is enabled, PFAILSTS bit in PFAILS will be set if the falling edge transition of PWRFAIL# is detected, and TREN will be cleared. This bit is ignored when TRENL bit is set. 0: No PWRFAIL# trap 1: PWRFAIL# trap

7.3.5 INTC Interrupt Assignments

Table 7-2. INTC Interrupt Assignments

Group	Interrupt	Source	Default Type (Adjustable)	Description	Reference
0	INT0	-	-	Reserved	-
	INT1	External/ WUC	High-Level Trig	External Source from GPD0	Figure 7-5, p213
	INT2	Internal	High-Level Trig	KBC Output Buffer Empty Interrupt	Section 6.6.3, p156
	INT3	Internal	High-Level Trig	PMC Output Buffer Empty Intr. PMC1 Output Buffer Empty Intr.	Section 6.7.3.1, p162 Section 6.7.3.1, p162
	INT4	Internal	High-Level Trig	SMBus D Interrupt	Section 7.8.3.1, p272
	INT5	External/ WUC	High-Level Trig	WKINTAD (WKINTA or WKINTD)	Figure 7-5, p213
	INT6	External/ WUC	High-Level Trig	External Source from GPC6	Figure 7-5, p213
	INT7	Internal	High-Level Trig	PWM Interrupt	Section 7.12.4.18, p393
1	INT8	Internal	High-Level Trig	ADC Interrupt	Section 7.11.3.1, p354
	INT9	Internal	High-Level Trig	SMBus A Interrupt	Section 7.8.3.1, p272
	INT10	Internal	High-Level Trig	SMBus B Interrupt	Section 7.8.3.1, p272
	INT11	Internal	High-Level Trig	KB Matrix Scan Interrupt	Section 7.5.2, p215
	INT12	External/ WUC	High-Level Trig	From SWUC Module	Figure 7-5, p213
	INT13	External/ WUC	High-Level Trig	WKINTC	Figure 7-5, p213
	INT14	External/ WUC	High-Level Trig	External Source from PWRSW	-
	INT15	-	-	Reserved	-
2	INT16	Internal	High-Level Trig	SMBus C Interrupt	Section 7.8.3.1, p272
	INT17	External/ WUC	High-Level Trig	External Source from GPD2	Figure 7-5, p213
	INT18	-	-	Reserved	-
	INT19	-	-	Reserved	-
	INT20	-	-	Reserved	-
	INT21	External/ WUC	High-Level Trig	External Source from GPC4	Figure 7-5, p213
	INT22	Internal	High-Level Trig	SMFI Semaphore Interrupt	Section 6.4.4.4, p121
	INT23	-	-	Reserved	-

Group	Interrupt	Source	Default Type (Adjustable)	Description	Reference
3	INT24	Internal	High-Level Trig	KBC Input Buffer Full Interrupt	Section 6.6.3, p156
	INT25	Internal	High-Level Trig	PMC Input Buffer Full Interrupt PMC1 Input Buffer Full Interrupt	Section 6.7.3.1, p162 Section 6.7.3.1, p162
	INT26	Internal	High-Level Trig	PMC2 Output Buffer Empty Intr.	Section 6.7.3.1, p162
	INT27	Internal	High-Level Trig	PMC2 Input Buffer Full Intr.	Section 6.7.3.1, p162
	INT28	External	High-Level Trig	GINT from function 1 of GPD5	Table 5-16, p19
	INT29	-	-	Reserved	-
	INT30	Internal	Rising-Edge Trig	External Timer 1 Interrupt	Section 7.14.3, p407
	INT31	External/ WUC	High-Level Trig	External Source from GPD1	Figure 7-5, p213
4	INT32	Internal	Rising-Edge Trig	GPINT0	Section 6.3.11.10, p98
	INT33	Internal		GPINT1	Section 6.3.11.10, p98
	INT34	Internal		GPINT2	Section 6.3.11.10, p98
	INT35	Internal		GPINT3	Section 6.3.11.10, p98
	INT36	-	-	Reserved	-
	INT37	Internal		SSPI Interrupt	Section 7.17.5.2, p466
	INT38	Internal		UART1 Interrupt	Section 7.19.5.3, p482
	INT39	Internal		UART2 Interrupt	Section 7.19.5.3, p482
5	INT40	-	-	Reserved	-
	INT41	-	-	Reserved	-
	INT42	-	-	Reserved	-
	INT43	-	-	Reserved	-
	INT44	-	-	Reserved	-
	INT45	-	-	Reserved	-
	INT46	-	-	Reserved	-
	INT47	-	-	Reserved	-
6	INT48	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPH0	Figure 7-5, p213
	INT49			External Source from GPH1	
	INT50			External Source from GPH2	
	INT51			External Source from GPH3	
	INT52			External Source from GPF4	
	INT53			External Source from GPF5	
	INT54			External Source from GPF6	
	INT55			External Source from GPF7	

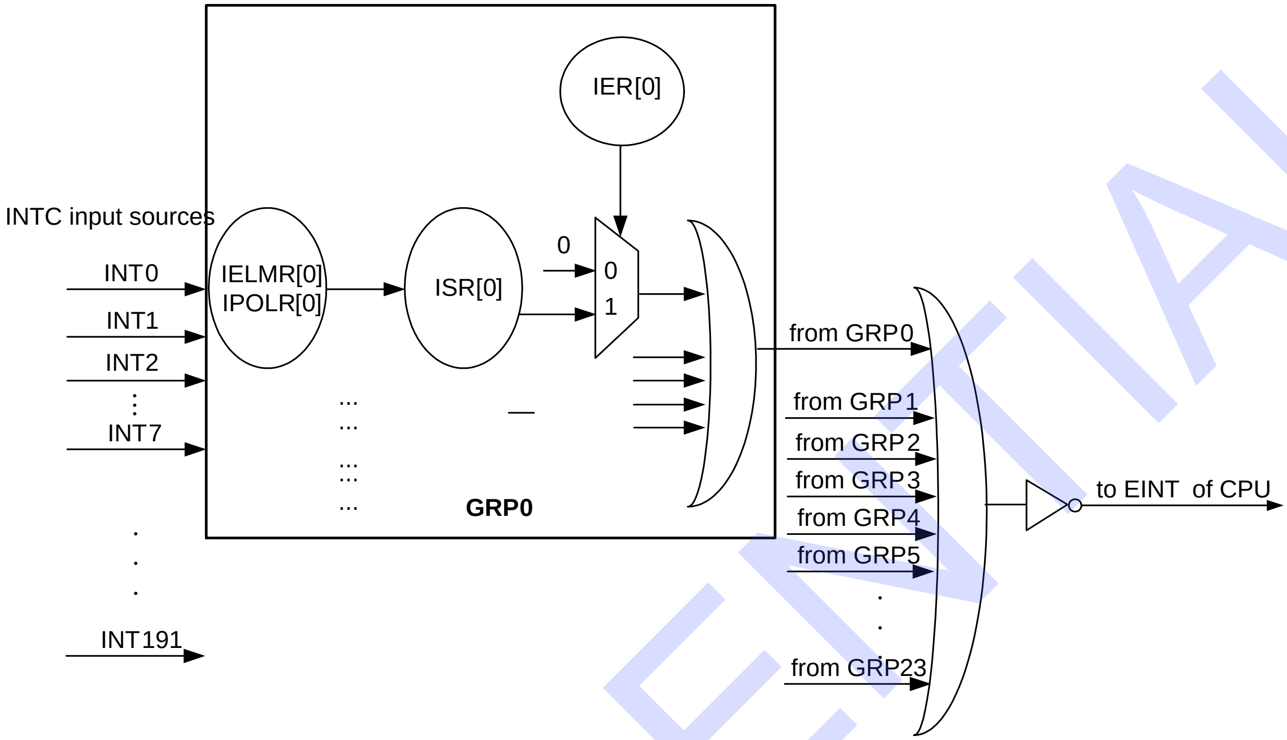
Group	Interrupt	Source	Default Type (Adjustable)	Description	Reference
7	INT56	-	Rising-Edge Trig (Not Adjustable)	Reserved	-
	INT57	-		Reserved	-
	INT58	Internal		External Timer 2 Interrupt	Section 7.14.3, p407
	INT59	Internal	High-Level Trig (Not Adjustable)	Deferred SPI Instruction Interrupt	-
	INT60	-	-	Reserved	-
	INT61	-	-	Reserved	-
	INT62	-	-	Reserved	-
	INT63	-	-	Reserved	-
8	INT64	Internal	High-Level Trig (Not Adjustable)	PMC2EX Output Buffer Empty Intr.	Section 6.7.3.1, p162
	INT65	Internal		PMC2EX Input Buffer Full Intr.	Section 6.7.3.1, p162
	INT66	Internal		PMC3 Output Buffer Empty Intr.	Section 6.7.3.1, p162
	INT67	Internal		PMC3 Input Buffer Full Intr.	Section 6.7.3.1, p162
	INT68	Internal		PMC4 Output Buffer Empty Intr.	Section 6.7.3.1, p162
	INT69	Internal		PMC4 Input Buffer Full Intr.	Section 6.7.3.1, p162
	INT70	-	-	Reserved	-
	INT71	Internal	High-Level Trig (Not Adjustable)	I2BRAM Interrupt	Section 7.15.4.21, p434
9	INT72	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPE0	Figure 7-5, p213
	INT73			External Source from GPE1	
	INT74			External Source from GPE2	
	INT75			External Source from GPE3	
	INT76			External Source from GPI4	
	INT77			External Source from GPI5	
	INT78			External Source from GPI6	
	INT79			External Source from GPI7	
10	INT80	Internal	Rising-Edge Trig	External Timer 8 Interrupt	Section 7.14.3, p407
	INT81	Internal	High-Level Trig (Not Adjustable)	SMbus Clock Held intr.	Section 7.8.3.2 , p274
	INT82	-	-	Reserved	-
	INT83	Internal	High-Level Trig (Not Adjustable)	H2RAM LPC Trigger	Section 6.4.4.42 , p130
	INT84	Internal		KB Scan Data Valid Interrupt	Section , 7.5.4.35, p227
	INT85	External/ WUC		External Source from GPH4	Figure 7-5, p213
	INT86	External/ WUC		External Source from GPH5	Figure 7-5, p213
	INT87	External/ WUC		External Source from GPH6	Figure 7-5, p213
	INT88			External Source from GPA3	

Group	Interrupt	Source	Default Type (Adjustable)	Description	Reference
11	INT89 INT90 INT91 INT92 INT93 INT94 INT95	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPA4 External Source from GPA5 External Source from GPA6 External Source from GPB2 External Source from GPC0 External Source from GPC7 External Source from GPD7	Figure 7-5, p213
12	INT96 INT97 INT98 INT99 INT100 INT101 INT102 INT103	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPA0 External Source from GPA1 External Source from GPA2 External Source from GPB4 External Source from GPC2 External Source from GPF0 External Source from GPF1 External Source from GPF2	Figure 7-5, p213
13	INT104 INT105 INT106 INT107 INT108 INT109 INT110 INT111	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPF3 External Source from GPA7 External Source from GPB0 External Source from GPB1 External Source from GPB3 External Source from GPB5 External Source from GPB6 External Source from GPB7	Figure 7-5, p213
14	INT112 INT113 INT114 INT115 INT116 INT117 INT118 INT119	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPC1 External Source from GPC3 External Source from GPC5 External Source from GPD3 External Source from GPD4 External Source from GPD5 External Source from GPD6 External Source from GPE4	Figure 7-5, p213
15	INT120 INT121 INT122 INT123 INT124 INT125 INT126 INT127	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPG0 External Source from GPG1 External Source from GPG2 External Source from GPG6 External Source from GPI0 External Source from GPI1 External Source from GPI2 External Source from GPI3	Figure 7-5, p213

Group	Interrupt	Source	Default Type (Adjustable)	Description	Reference
16	INT128	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPJ0	Figure 7-5, p213
	INT129			External Source from GPJ1	
	INT130			External Source from GPJ2	
	INT131			External Source from GPJ3	
	INT132			External Source from GPJ4	
	INT133			External Source from GPJ5	
	INT134			External Source from GPJ6	
	INT135			External Source from GPJ7	
17	INT136	-	-	Reserved	-
	INT137	-	-	Reserved	-
	INT138	-	-	Reserved	-
	INT139	-	-	Reserved	-
	INT140	-	-	Reserved	-
	INT141	-	-	Reserved	-
	INT142	-	-	Reserved	-
	INT143	-	-	Reserved	-
18	INT144	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPG3	Figure 7-5, p213
	INT145			External Source from GPG4	
	INT146			External Source from GPG5	
	INT147			External Source from GPG7	
	INT148	-	-	Reserved	-
	INT149	Internal	High-Level Trig (Not Adjustable)	PMC5 Output Buffer Empty Intr.	Section 6.7.3.1, p162
	INT150	Internal	High-Level Trig (Not Adjustable)	PMC5 Input Buffer Full Intr.	Section 6.7.3.1, p162
	INT151	Internal	High-Level Trig (Not Adjustable)	Voltage Comparator Interrupt	Section 7.11.3.1, p354
19	INT152	Internal	High-Level Trig	SMBus E Interrupt	Section 7.8.3.1, p272
	INT153	Internal	High-Level Trig	SMBus F Interrupt	Section 7.8.3.1, p272
	INT154	Internal	High-Level Trig	ILM DMA Interrupt	-
	INT155	Internal	Falling-Edge Trig	External Timer 3 Interrupt	Section 7.14.3, p407
	INT156	Internal		External Timer 4 Interrupt	
	INT157	Internal		External Timer 5 Interrupt	
	INT158	Internal		External Timer 6 Interrupt	
	INT159	Internal		External Timer 7 Interrupt	
20	INT160	Internal	High-Level Trig (Not Adjustable)	PECI Interrupt	Section 7.10, p344
	INT161	Internal	High-Level Trig	Software Interrupt	-
	INT162	Internal	High-Level Trig	ESPI Interrupt	Section 6.1, p37
	INT163	Internal	High-Level Trig	ESPI VW Interrupt	Section 6.1, p37
	INT164	Internal	High-Level Trig	PCH port80 Interrupt	-
	INT165	Internal	High-Level Trig	USBPD0 Interrupt	Section 7.20, p492
	INT166	Internal	High-Level Trig	USBPD1 Interrupt	Section 7.20, p492
	INT167	-	-	Reserved	-

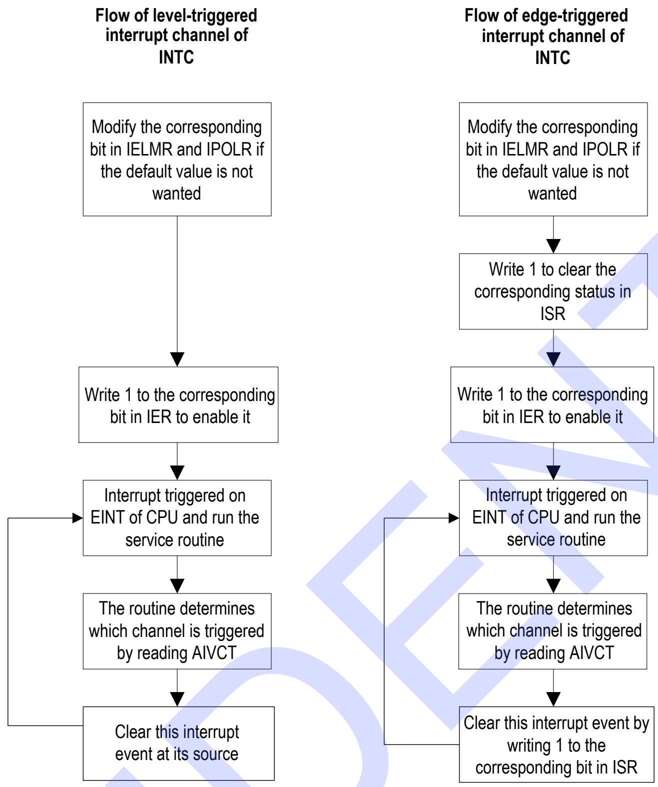
Group	Interrupt	Source	Default Type (Adjustable)	Description	Reference
21	INT168	-	-	Reserved	-
	INT169	-	-	Reserved	-
	INT170	-	-	Reserved	-
	INT171	Internal	High-Level Trig	SPI Slave Interrupt	Section 7.21, p522
	INT172	-	-	Reserved	-
	INT173	-	-	Reserved	-
	INT174	-	-	Reserved	-
	INT175	-	-	Reserved	-
22	INT176	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPE5	Figure 7-5, p213
	INT177			External Source from GPE6	Figure 7-5, p213
	INT178			External Source from GPE7	Figure 7-5, p213
	INT179			External Source from GPM0	Figure 7-5, p213
	INT180			External Source from GPM1	Figure 7-5, p213
	INT181			External Source from GPM2	Figure 7-5, p213
	INT182			External Source from GPM3	Figure 7-5, p213
	INT183			External Source from GPM4	Figure 7-5, p213
23	INT184	External/ WUC	High-Level Trig (Not Adjustable)	External Source from GPM5	Figure 7-5, p213
	INT185			External Source from GPM6	Figure 7-5, p213
	INT186	-	-	Reserved	-
	INT187	-	-	Reserved	-
	INT188	-	-	Reserved	-
	INT189	-	-	Reserved	-
	INT190	-	-	Reserved	-
	INT191	-	-	Reserved	-

Figure 7-3. INTC Simplified Diagram



7.3.6 Programming Guide

Figure 7-4. Program Flow Chart for INTC



Note: The routine may has its own interrupt priority by reading ISR register.
Note: If this channel source comes from WUC, the corresponding bit in WUESR needs to be cleared, too

7.4 Wake-Up Control (WUC)

7.4.1 Overview

WUC groups internal and external inputs, and asserts wake-up signals to INTC that allows the CPU to exit a Doze/Deep Doze/Sleep mode.

7.4.2 Features

- Supports internal and external interrupt inputs.
- Supports both the rising-edge and falling-edge triggered mode.
- Input can be connected to INTC directly.

7.4.3 Functional Description

Input sources of WUC are external inputs such as pins about GPIO and KB Matrix Scan, or inputs from internal module such as SWUC, LPC and SMBus that handle external inputs.

Each channel can be selected to be rising, falling edge or both edge triggered mode. If one channel is disabled, the input bypasses WUC pending logic and is connected directly to INTC.

7.4.4 EC Interface Registers

The EC interface registers are listed below. The base address for WUC is 1B00h.

Table 7-3. EC View Register Map, WUC

7 0	Offset
Wake-Up Edge Mode Register 1 (WUEMR1)	00h
Wake-Up Edge Mode Register 2 (WUEMR2)	01h
Wake-Up Edge Mode Register 3 (WUEMR3)	02h
Wake-Up Edge Mode Register 4 (WUEMR4)	03h
Wake-Up Edge Mode Register 5 (WUEMR5)	0Ch
Wake-Up Edge Mode Register 6 (WUEMR6)	10h
Wake-Up Edge Mode Register 7 (WUEMR7)	14h
Wake-Up Edge Mode Register 8 (WUEMR8)	18h
Wake-Up Edge Mode Register 9 (WUEMR9)	1Ch
Wake-Up Edge Mode Register 10 (WUEMR10)	20h
Wake-Up Edge Mode Register 11 (WUEMR11)	24h
Wake-Up Edge Mode Register 12 (WUEMR12)	28h
Wake-Up Edge Mode Register 13 (WUEMR13)	2Ch
Wake-Up Edge Mode Register 14 (WUEMR14)	30h
Wake-Up Edge Mode Register 15 (WUEMR15)	34h
Wake-Up Edge Mode Register 16 (WUEMR16)	38h
Wake-Up Edge Mode Register 19 (WUEMR19)	44h
Wake-Up Edge Mode Register 20 (WUEMR20)	48h
Wake-Up Edge Mode Register 21 (WUEMR21)	4Ch
Wake-Up Edge Mode Register 22 (WUEMR22)	50h
Wake-Up Edge Sense Register 1 (WUESR1)	04h
Wake-Up Edge Sense Register 2 (WUESR2)	05h
Wake-Up Edge Sense Register 3 (WUESR3)	06h
Wake-Up Edge Sense Register 4 (WUESR4)	07h
Wake-Up Edge Sense Register 5 (WUESR5)	0Dh
Wake-Up Edge Sense Register 6 (WUESR6)	11h
Wake-Up Edge Sense Register 7 (WUESR7)	15h
Wake-Up Edge Sense Register 8 (WUESR8)	19h

7 0	Offset
Wake-Up Edge Sense Register 9 (WUESR9)	1Dh
Wake-Up Edge Sense Register 10 (WUESR10)	21h
Wake-Up Edge Sense Register 11 (WUESR11)	25h
Wake-Up Edge Sense Register 12 (WUESR12)	29h
Wake-Up Edge Sense Register 13 (WUESR13)	2Dh
Wake-Up Edge Sense Register 14 (WUESR14)	31h
Wake-Up Edge Sense Register 15 (WUESR15)	35h
Wake-Up Edge Sense Register 16 (WUESR16)	39h
Wake-Up Edge Sense Register 19 (WUESR19)	45h
Wake-Up Edge Sense Register 20 (WUESR20)	49h
Wake-Up Edge Sense Register 21 (WUESR21)	4Dh
Wake-Up Edge Sense Register 22 (WUESR22)	51h
Wake-Up Enable Register 1 (WUENR1)	08h
Wake-Up Enable Register 3 (WUENR3)	0Ah
Wake-Up Enable Register 4 (WUENR4)	0Bh
Wake-Up Both Edge Mode Register 1 (WUBEMR1)	3Ch
Wake-Up Both Edge Mode Register 2 (WUBEMR2)	3Dh
Wake-Up Both Edge Mode Register 3 (WUBEMR3)	3Eh
Wake-Up Both Edge Mode Register 4 (WUBEMR4)	3Fh
Wake-Up Both Edge Mode Register 5 (WUBEMR5)	0Fh
Wake-Up Both Edge Mode Register 6 (WUBEMR6)	13h
Wake-Up Both Edge Mode Register 7 (WUBEMR7)	17h
Wake-Up Both Edge Mode Register 8 (WUBEMR8)	1Bh
Wake-Up Both Edge Mode Register 9 (WUBEMR9)	1Fh
Wake-Up Both Edge Mode Register 10 (WUBEMR10)	23h
Wake-Up Both Edge Mode Register 11 (WUBEMR11)	27h
Wake-Up Both Edge Mode Register 12 (WUBEMR12)	2Bh
Wake-Up Both Edge Mode Register 13 (WUBEMR13)	2Fh
Wake-Up Both Edge Mode Register 14 (WUBEMR14)	33h
Wake-Up Both Edge Mode Register 15 (WUBEMR15)	37h
Wake-Up Both Edge Mode Register 16 (WUBEMR16)	3Bh
Wake-Up Both Edge Mode Register 19 (WUBEMR19)	47h
Wake-Up Both Edge Mode Register 20 (WUBEMR20)	4Bh
Wake-Up Both Edge Mode Register 21 (WUBEMR21)	4Fh
Wake-Up Both Edge Mode Register 22 (WUBEMR22)	53h

7.4.4.1 Wake-Up Edge Mode Register 1-22 (WUEMR1-WUEMR22)

This register configures the trigger mode of input signals Group x. (Refer to Table 7-4 on page 209)

WUEMR1 defined in Group 1
WUEMR2 defined in Group 2
WUEMR3 defined in Group 3
WUEMR4 defined in Group 4
WUEMR6 defined in Group 6
WUEMR7 defined in Group 7
WUEMR8 defined in Group 8
WUEMR9 defined in Group 9
WUEMR10 defined in Group 10
WUEMR11 defined in Group 11
WUEMR12 defined in Group 12
WUEMR13 defined in Group 13
WUEMR14 defined in Group 14
WUEMR15 defined in Group 15
WUEMR16 defined in Group 16
WUEMR17 defined in Group 17 (Reserved)
WUEMR18 defined in Group 18 (Reserved)
WUEMR19 defined in Group 19
WUEMR20 defined in Group 20
WUEMR21 defined in Group 21
WUEMR22 defined in Group 22

Address Offset: 00h-03h,10h,14h,18h,1Ch,20h,24h,28h,2Ch,30h,34h,38h,3Ch,40h,44h,48h,4Ch,50h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Edge Mode Group x (WUEMGRx 7:0)** 0: Rising-edge triggered is selected.(for Group 1-22) 1: Falling-edge triggered is selected.(for Group 1-22) Always write-1-clear to the corresponding bit in WUESR register after modifying these bits. **Note**: Where x means (1 – 22)

7.4.4.2 Wake-Up Edge Sense Register 1-22 (WUESR1-WUESR22)

This register indicates the occurrence of a selected trigger condition and is associated with input signals Group x. (Refer to Table 7-4 on page 209).

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

WUESR1 defined in Group 1
WUESR2 defined in Group 2
WUESR3 defined in Group 3
WUESR4 defined in Group 4
WUESR6 defined in Group 6
WUESR7 defined in Group 7
WUESR8 defined in Group 8
WUESR9 defined in Group 9
WUESR10 defined in Group 10
WUESR11 defined in Group 11
WUESR12 defined in Group 12
WUESR13 defined in Group 13
WUESR14 defined in Group 14
WUESR15 defined in Group 15
WUESR16 defined in Group 16
WUESR17 defined in Group 17 (Reserved)
WUESR18 defined in Group 18 (Reserved)
WUESR19 defined in Group 19
WUESR20 defined in Group 20
WUESR21 defined in Group 21
WUESR22 defined in Group 22

Address Offset: 04h-07h,11h,15h,19h,1Dh,21h,25h,29h,2Dh,31h,35h,39h,3Dh,41h,45h,49h,4Dh,51h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense Group x (WUSGRx 7:0)** For each bit: Read 1: It indicates a trigger condition occurs on the corresponding input. Read 0: Otherwise For each bit: Write 1: Clear this bit Write 0: No action **Note**: Where x means (1 - 22)

7.4.4.3 Wake-Up Enable Register 1/3/4 (WUENR1, WUENR3, WUENR4)

This register enables a wake-up function of the corresponding input signal Group x. (Refer to Table 7-4 on page 209).

Note: Only for Group 1/3/4

WUENR1 defined in Group 1
WUENR3 defined in Group 3
WUENR4 defined in Group 4

Address Offset: 08h,0Ah,0Bh

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable Group x (WUENGRx 7:0)** 1: A trigger condition on the corresponding input generates a wake-up signal to the power management control of EC. 0: A trigger condition on the corresponding input doesn't assert the wake-up signal; it is canceled but not pending. **Note:** Where x means (1 / 3 / 4)

7.4.4.4 Wake-Up Both Edge Mode Register 1-22 (WUBEMR1-WUBEMR22)

This register configures the trigger mode of input signals Group x. (Refer to Table 7-4 on page 209)

WUBEMR1 defined in Group 1
WUBEMR2 defined in Group 2
WUBEMR3 defined in Group 3
WUBEMR4 defined in Group 4
WUBEMR6 defined in Group 6
WUBEMR7 defined in Group 7
WUBEMR8 defined in Group 8
WUBEMR9 defined in Group 9
WUBEMR10 defined in Group 10
WUBEMR11 defined in Group 11
WUBEMR12 defined in Group 12
WUBEMR13 defined in Group 13
WUBEMR14 defined in Group 14
WUBEMR15 defined in Group 15
WUBEMR16 defined in Group 16
WUBEMR17 defined in Group 17 (Reserved)
WUBEMR18 defined in Group 18 (Reserved)
WUBEMR19 defined in Group 19
WUBEMR20 defined in Group 20
WUBEMR21 defined in Group 21
WUBEMR22 defined in Group 22

Address Offset:
3Ch,3D,3Eh,3Fh,0Fh,13h,17h,1Bh,1Fh,23h,27h,2Bh,2Fh,33h,37h,3Bh,3Fh,43h,47h,4Bh,4Fh,53h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Both Edge Mode Group x (WUBEMGRx 7:0)** 0: Refer to WUEMGRx values. 1: Either-edge (rising-edge or falling-edge) triggered is selected. Always write-1-clear to the corresponding bit in WUESR register after modifying these bits. **Note**: Where x means (1 – 22)

7.4.5 WUC Input Assignments

Table 7-4. WUC Input Assignments

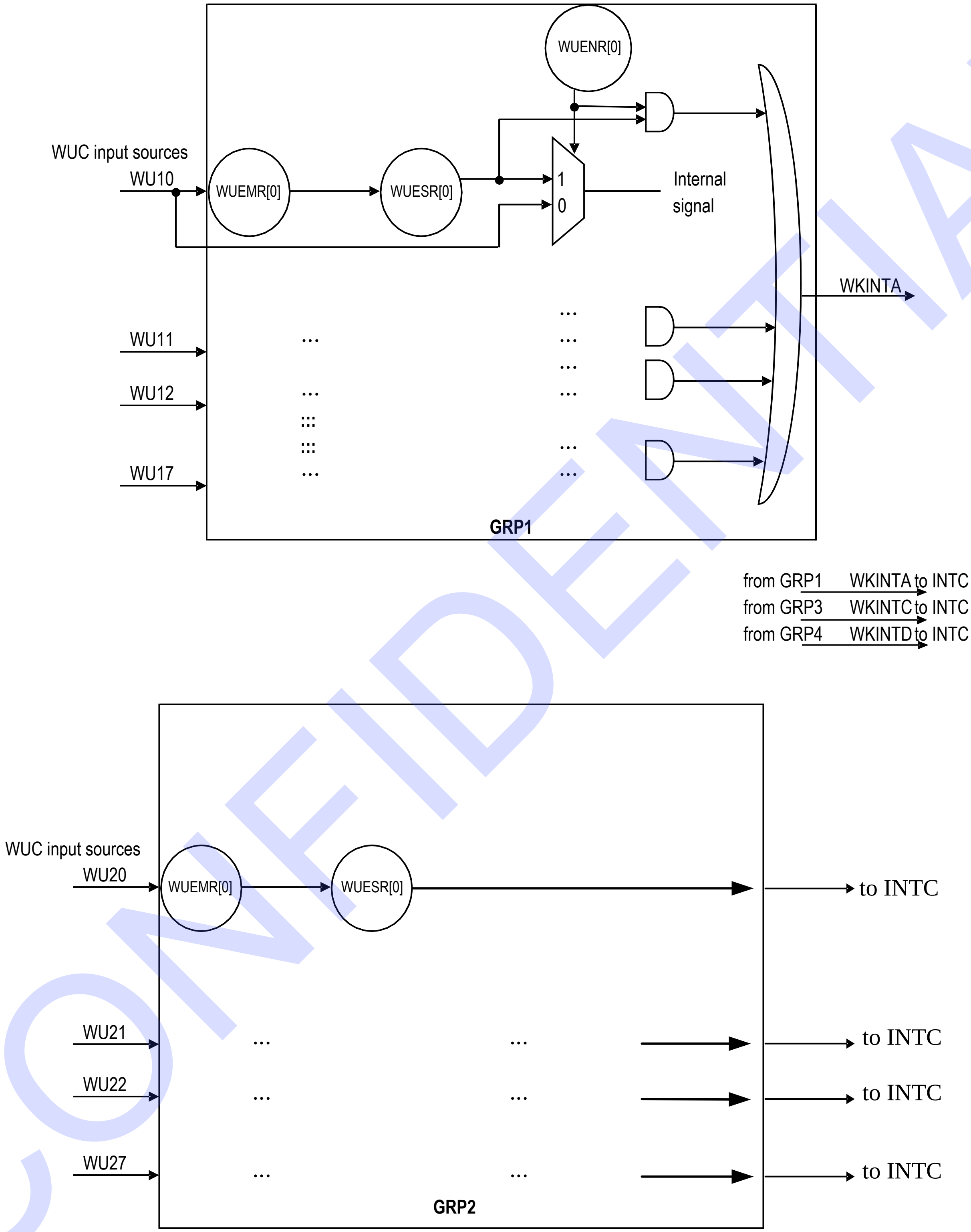
Group	WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
1	WU10	-	Reserved	-	-
	WU11	-	Reserved	-	-
	WU12	-	Reserved	-	-
	WU13	-	Reserved	-	-
	WU14	-	Reserved	-	-
	WU15	-	Reserved	-	-
	WU16	-	Reserved	-	-
	WU17	-	Reserved	-	-
2	WU20	WUI0	External Source from GPD0	INT1	Rising Edge Trig
	WU21	WUI1	External Source from GPD1	INT31	Rising Edge Trig
	WU22	WUI2	External Source from GPC4	INT21	Rising Edge Trig
	WU23	WUI3	External Source from GPC6	INT6	Rising Edge Trig
	WU24	WUI4	External Source from GPD2	INT17	Rising Edge Trig
	WU25	PWRSW	External Source from GPE4	INT14	-
	WU26	SWUC Wake Up	From SWUC Module	INT12	Rising Edge Trig
	WU27	-	Reserved	-	-
3	WU30	KSI[0]	External Source from Pin	WKINTC, to INT13	Rising Edge Trig
	WU31	KSI[1]	External Source from Pin		Rising Edge Trig
	WU32	KSI[2]	External Source from Pin		Rising Edge Trig
	WU33	KSI[3]	External Source from Pin		Rising Edge Trig
	WU34	KSI[4]	External Source from Pin		Rising Edge Trig
	WU35	KSI[5]	External Source from Pin		Rising Edge Trig
	WU36	KSI[6]	External Source from Pin		Rising Edge Trig
	WU37	KSI[7]	External Source from Pin		Rising Edge Trig
4	WU40	WUI5	External Source from GPE5	WKINTD, to INT5 & INT176	Rising Edge Trig
	WU41	-	Reserved	-	-
	WU42	LPC Access	LPC Cycle with Address Recognized See also Section 6.2.6, p71	WKINTD, to INT5	Rising Edge Trig
	WU43	SMDAT0	External Source from Pin	WKINTD, to INT5	Rising Edge Trig
	WU44	SMDAT1	External Source from Pin	WKINTD, to INT5	Rising Edge Trig
	WU45	WUI6	External Source from GPE6	WKINTD, to INT5 & to INT177	Rising Edge Trig
	WU46	WUI7	External Source from GPE7	WKINTD, to INT5 & to INT178	Rising Edge Trig
	WU47	SMDAT2	External Source from Pin	WKINTD, to INT5	Rising Edge Trig

Group	WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
5	WU50	-	Reserved	-	-
	WU51	-	Reserved	-	-
	WU52	-	Reserved	-	-
	WU53	-	Reserved	-	-
	WU54	-	Reserved	-	-
	WU55	-	Reserved	-	-
	WU56	-	Reserved	-	-
	WU57	-	Reserved	-	-
6	WU60	WUI16	External Source from GPH0	INT48	Rising Edge Trig
	WU61	WUI17	External Source from GPH1	INT49	Rising Edge Trig
	WU62	WUI18	External Source from GPH2	INT50	Rising Edge Trig
	WU63	WUI19	External Source from GPH3	INT51	Rising Edge Trig
	WU64	WUI20	External Source from GPF4	INT52	Rising Edge Trig
	WU65	WUI21	External Source from GPF5	INT53	Rising Edge Trig
	WU66	WUI22	External Source from GPF6	INT54	Rising Edge Trig
	WU67	WUI23	External Source from GPF7	INT55	Rising Edge Trig
7	WU70	WUI24	External Source from GPE0	INT72	Rising Edge Trig
	WU71	WUI25	External Source from GPE1	INT73	Rising Edge Trig
	WU72	WUI26	External Source from GPE2	INT74	Rising Edge Trig
	WU73	WUI27	External Source from GPE3	INT75	Rising Edge Trig
	WU74	WUI28	External Source from GPI4	INT76	Rising Edge Trig
	WU75	WUI29	External Source from GPI5	INT77	Rising Edge Trig
	WU76	WUI30	External Source from GPI6	INT78	Rising Edge Trig
	WU77	WUI31	External Source from GPI7	INT79	Rising Edge Trig
8	WU80	WUI32	External Source from GPA3	INT88	Rising Edge Trig
	WU81	WUI33	External Source from GPA4	INT89	Rising Edge Trig
	WU82	WUI34	External Source from GPA5	INT90	Rising Edge Trig
	WU83	WUI35	External Source from GPA6	INT91	Rising Edge Trig
	WU84	WUI36	External Source from GPB2	INT92	Rising Edge Trig
	WU85	WUI37	External Source from GPC0	INT93	Rising Edge Trig
	WU86	WUI38	External Source from GPC7	INT94	Rising Edge Trig
	WU87	WUI39	External Source from GPD7	INT95	Rising Edge Trig
9	WU88	WUI40	External Source from GPH4	INT85	Rising Edge Trig
	WU89	WUI41	External Source from GPH5	INT86	Rising Edge Trig
	WU90	WUI42	External Source from GPH6	INT87	Rising Edge Trig
	WU91	WUI43	External Source from GPA0	INT96	Rising Edge Trig
	WU92	WUI44	External Source from GPA1	INT97	Rising Edge Trig
	WU93	WUI45	External Source from GPA2	INT98	Rising Edge Trig
	WU94	WUI46	External Source from GPB4	INT99	Rising Edge Trig
	WU95	WUI47	External Source from GPC2	INT100	Rising Edge Trig
10	WU96	WUI48	External Source from GPF0	INT101	Rising Edge Trig
	WU97	WUI49	External Source from GPF1	INT102	Rising Edge Trig
	WU98	WUI50	External Source from GPF2	INT103	Rising Edge Trig
	WU99	WUI51	External Source from GPF3	INT104	Rising Edge Trig
	WU100	WUI52	External Source from GPA7	INT105	Rising Edge Trig
	WU101	WUI53	External Source from GPB0	INT106	Rising Edge Trig

Group	WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
	WU102	WUI54	External Source from GPB1	INT107	Rising Edge Trig
	WU103	WUI55	External Source from GPB3	INT108	Rising Edge Trig
	WU104	WUI56	External Source from GPB5	INT109	Rising Edge Trig
	WU105	WUI57	External Source from GPB6	INT110	Rising Edge Trig
	WU106	WUI58	External Source from GPB7	INT111	Rising Edge Trig
11	WU107	WUI59	External Source from GPC1	INT112	Rising Edge Trig
	WU108	WUI60	External Source from GPC3	INT113	Rising Edge Trig
	WU109	WUI61	External Source from GPC5	INT114	Rising Edge Trig
	WU110	WUI62	External Source from GPD3	INT115	Rising Edge Trig
	WU111	WUI63	External Source from GPD4	INT116	Rising Edge Trig
	WU112	WUI64	External Source from GPD5	INT117	Rising Edge Trig
	WU113	WUI65	External Source from GPD6	INT118	Rising Edge Trig
	WU114	WUI66	External Source from GPE4	INT119	Rising Edge Trig
12	WU115	WUI67	External Source from GPG0	INT120	Rising Edge Trig
	WU116	WUI68	External Source from GPG1	INT121	Rising Edge Trig
	WU117	WUI69	External Source from GPG2	INT122	Rising Edge Trig
	WU118	WUI70	External Source from GPG6	INT123	Rising Edge Trig
	WU119	WUI71	External Source from GPI0	INT124	Rising Edge Trig
	WU120	WUI72	External Source from GPI1	INT125	Rising Edge Trig
	WU121	WUI73	External Source from GPI2	INT126	Rising Edge Trig
	WU122	WUI74	External Source from GPI3	INT127	Rising Edge Trig
	WU123	WUI75	External Source from GPG3	INT144	Rising Edge Trig
13	WU124	WUI76	External Source from GPG4	INT145	Rising Edge Trig
	WU125	WUI77	External Source from GPG5	INT146	Rising Edge Trig
	WU126	WUI78	External Source from GPG7	INT147	Rising Edge Trig
	WU127	-	Reserved	-	-
	WU128	WUI80	External Source from GPJ0	INT128	Rising Edge Trig
	WU129	WUI81	External Source from GPJ1	INT129	Rising Edge Trig
	WU130	WUI82	External Source from GPJ2	INT130	Rising Edge Trig
	WU131	WUI83	External Source from GPJ3	INT131	Rising Edge Trig
14	WU132	WUI84	External Source from GPJ4	INT132	Rising Edge Trig
	WU133	WUI85	External Source from GPJ5	INT133	Rising Edge Trig
	WU134	WUI86	External Source from GPJ6	INT134	Rising Edge Trig
	WU135	WUI87	External Source from GPJ7	INT135	Rising Edge Trig
	WU136	-	Reserved	-	-
	WU137	-	Reserved	-	-
	WU138	-	Reserved	-	-
	WU139	-	Reserved	-	-
15	WU140	-	Reserved	-	-
	WU141	-	Reserved	-	-
	WU142	-	Reserved	-	-
	WU143	-	Reserved	-	-
	WU144	WUI96	External Source from GPM0	INT179	Rising Edge Trig
	WU145	WUI97	External Source from GPM1	INT180	Rising Edge Trig
	WU146	WUI98	External Source from GPM2	INT181	Rising Edge Trig
	WU147	WUI99	External Source from GPM3	INT182	Rising Edge Trig
16	WU148	WUI100	External Source from GPM4	INT183	Rising Edge Trig

Group	WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
	WU149	WUI101	External Source from GPM5	INT184	Rising Edge Trig
	WU150	WUI102	External Source from GPM6	INT185	Rising Edge Trig
	WU151	-	Reserved	-	-
19	WU168	-	Reserved	-	-
	WU169	-	Reserved	-	-
	WU170	-	Reserved	-	-
	WU171	-	Reserved	-	-
	WU172	-	Reserved	-	-
	WU173	-	Reserved	-	-
	WU174	-	Reserved	-	-
	WU175	-	Reserved	-	-
20	WU176	-	Reserved	-	-
	WU177	-	Reserved	-	-
	WU178	-	Reserved	-	-
	WU179	-	Reserved	-	-
	WU180	-	Reserved	-	-
	WU181	-	Reserved	-	-
	WU182	-	Reserved	-	-
	WU183	-	Reserved	-	-
21	WU184	-	Reserved	-	-
	WU185	-	Reserved	-	-
	WU186	-	Reserved	-	-
	WU187	-	Reserved	-	-
	WU188	-	Reserved	-	-
	WU189	-	Reserved	-	-
	WU190	-	Reserved	-	-
	WU191	-	Reserved	-	-
22	WU192	-	Reserved	-	-
	WU193	-	Reserved	-	-
	WU194	-	Reserved	-	-
	WU195	-	Reserved	-	-
	WU196	-	Reserved	-	-
	WU197	-	Reserved	-	-
	WU198	-	Reserved	-	-
	WU199	-	Reserved	-	-

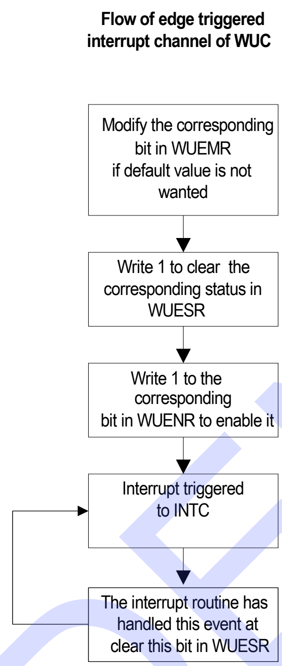
Figure 7-5. WUC Simplified Diagram



7.4.6 Programming Guide

If the WUC source is from GPIO port, the firmware should not enable the corresponding channel when this GPIO is not in alternate function.

Figure 7-6. Program Flow Chart for WUC



7.5 Keyboard Matrix Scan Controller

7.5.1 Overview

The module provides control for keyboard matrix scan.

7.5.2 Features

- Supports 18 x scan output
- Supports 8 x scan input
- Supports Schmitt trigger input pin
- Supports programmable pull-up on all output/input pins
- Supports one interrupt (connected to INT11 of INTC) for any KSI inputs to go low to wake up the system
- Supports GPIO mode for all KBS pins (GPIO mode overrides EPP mode)

7.5.3 Functional Description

- **KSI/KSO Used as Keyboard Matrix**

Normal usage.

- **KSI/KSO Used as GPIO**

If the EC is applied to a platform without keyboard matrix, KSI/KSO pins can be used as GPIO. See also Figure 7-35. Parallel Port Female 25-Pin Connector on page 535.

Table 7-5. KSI/KSO as GPIO List

KSI0/STB#	—	EPP Signal	Could be used as GPIO
KSI1/AFD#	Hardware strap	EPP Signal	Could be used as GPIO
KSI2/INIT#	Hardware strap	EPP Constant Signal	Could be used as GPIO
KSI3/SLIN#	—	EPP Signal	Could be used as GPIO
KSI4	Hardware strap	—	Could be used as GPIO
KSI5	Hardware strap	—	Could be used as GPIO
KSI6	—	—	Could be used as GPIO
KSI7	—	—	Could be used as GPIO
KSO0/PD0	—	EPP Signal	Could be used as GPIO
KSO1/PD1	—	EPP Signal	Could be used as GPIO
KSO2/PD2	—	EPP Signal	Could be used as GPIO
KSO3/PD3	—	EPP Signal	Could be used as GPIO
KSO4/PD4	—	EPP Signal	Could be used as GPIO
KSO5/PD5	—	EPP Signal	Could be used as GPIO
KSO6/PD6	—	EPP Signal	Could be used as GPIO
KSO7/PD7	—	EPP Signal	Could be used as GPIO
KSO8/ACK#	—	EPP Constant Signal	Could be used as GPIO
KSO9/BUSY	—	EPP Signal	Could be used as GPIO
KSO10/PE	—	EPP Constant Signal	Could be used as GPIO
KSO11/ERR#	—	EPP Constant Signal	Could be used as GPIO
KSO12/SLCT	—	EPP Constant Signal	Could be used as GPIO
KSO13	—	—	Could be used as GPIO
KSO14	—	—	Could be used as GPIO
KSO15	—	—	Could be used as GPIO

7.5.4 EC Interface Registers

The keyboard matrix scan registers are listed below. The base address is 1D00h.

Table 7-6. EC View Register Map, KB Scan

7 ... 0	Offset
Keyboard Scan Out [7:0] (KSOL)	00h
Keyboard Scan Out [15:8] (KSOH1)	01h
Keyboard Scan Out Control (KSOCTRL)	02h
Keyboard Scan Out [17:16] (KSOH2)	03h
Keyboard Scan In [7:0] (KSI)	04h
Keyboard Scan In Control (KSICTRLR)	05h
Keyboard Scan In [7:0] GPIO Control Register (KSIGCTRL)	06h
Keyboard Scan In [7:0] GPIO Output Enable Register (KSIGOEN)	07h
Keyboard Scan In [7:0] GPIO Data Register (KSIGDAT)	08h
Keyboard Scan In [7:0] GPIO Data Mirror Register (KSIGDMRR)	09h
Keyboard Scan Out [15:8] GPIO Control Register (KSOHGCTRL)	0Ah
Keyboard Scan Out [15:8] GPIO Output Enable Register (KSOHGOEN)	0Bh
Keyboard Scan Out [15:8] GPIO Data Mirror Register (KSOHGDMRR)	0Ch
Keyboard Scan Out [7:0] GPIO Control Register (KSOLGCTRL)	0Dh
Keyboard Scan Out [7:0] GPIO Output Enable Register (KSOLGOEN)	0Eh
Keyboard Scan Out [7:0] GPIO Data Mirror Register (KSOLGDMRR)	0Fh
KSO0 Low Scan Data Register (KSO0LSDR)	10h
KSO1 Low Scan Data Register (KSO1LSDR)	11h
KSO2 Low Scan Data Register (KSO2LSDR)	12h
KSO3 Low Scan Data Register (KSO3LSDR)	13h
KSO4 Low Scan Data Register (KSO4LSDR)	14h
KSO5 Low Scan Data Register (KSO5LSDR)	15h
KSO6 Low Scan Data Register (KSO6LSDR)	16h
KSO7 Low Scan Data Register (KSO7LSDR)	17h
KSO8 Low Scan Data Register (KSO8LSDR)	18h
KSO9 Low Scan Data Register (KSO9LSDR)	19h
KSO10 Low Scan Data Register (KSO10LSDR)	1Ah
KSO11 Low Scan Data Register (KSO11LSDR)	1Bh
KSO12 Low Scan Data Register (KSO12LSDR)	1Ch
KSO13 Low Scan Data Register (KSO13LSDR)	1Dh
KSO14 Low Scan Data Register (KSO14LSDR)	1Eh
KSO15 Low Scan Data Register (KSO15LSDR)	1Fh
KSO16 Low Scan Data Register (KSO16LSDR)	20h
KSO17 Low Scan Data Register (KSO17LSDR)	21h
Scan Data Control1 Register (SDC1R)	22h
Scan Data Control2 Register (SDC2R)	23h
Scan Data Control3 Register (SDC3R)	24h
Scan Data Status Register (SDSR)	25h
Keyboard Scan In [7:0] GPIO Open-Drain Register (KSIGPODR)	26h
Keyboard Scan Out [15:8] GPIO Open-Drain Register (KSOHGPODR)	27h
Keyboard Scan Out [7:0] GPIO Open-Drain Register (KSOLGPODR)	28h

7.5.4.1 Keyboard Scan Out Low Byte Data Register (KSOL)

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Keyboard Scan Out Low Data [7:0] (KSOL)** This is the 8-bit keyboard scan output register which controls the KSO[7:0] pins. In the GPIO mode, this register is used as KSO[7:0] Data Register (refer to the related KSO GPIO registers).

7.5.4.2 Keyboard Scan Out High Byte Data 1 Register (KSOH1)

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Keyboard Scan Out High Data 1 [7:0] (KSOH1)** This is the 8-bit keyboard scan output register which controls the KSO[15:8] pins. In the GPIO mode, this register is used as KSO[15:8] Data Register (Refer to the related KSO GPIO registers).

7.5.4.3 Keyboard Scan Out Control Register (KSOCTRL)

Address Offset: 02h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**KSO Pull Up (KSOPU)** Setting 1 enables the internal pull-up of the KSO[15:0] pins. To pull up KSO[17:16], set the GPCR registers of their corresponding GPIO ports. In the GPIO mode, the internal pull-up of the pins KSO[15:0] is always disabled even if this bit is set.
1	-	-	**Reserved**
0	R/W	0b	**KSO Open Drain (KSOOD)** Setting 1 enables the open-drain mode of the KSO[17:0] pins. Setting 0 selects the push-pull mode. In the GPIO mode, the open-drain mode of the pins KSO[15:0] is always disabled even if this bit is set.

7.5.4.4 Keyboard Scan Out High Byte Data 2 Register (KSOH2)

Address Offset: 03h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Keyboard Scan Out High Data 2 [1:0] (KSOH2)** This is the 2-bit keyboard scan output register which controls the KSO[17:16] pins.

7.5.4.5 Keyboard Scan In Data Register (KSIR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R	00h	**Keyboard Scan In High Data [7:0] (KSI)** This is the 8-bit keyboard scan input register which shows the value of the KSI[7:0] pins.

7.5.4.6 Keyboard Scan In Control Register (KSICTRLR)

Address Offset: 05h

Bit	R/W	Default	Description
7-5	-	000b	**Reserved**
4	R/W	0b	**Override PP from KBS (OVRPPK)** This bit overrides PP function which is enabled by hardware strap in KBS interface and disables it.
3	-	-	**Reserved**
2	R/W	0b	**KSI Pull Up (KSIPU)** Setting 1 enables the internal pull-up of the KSI[7:0] pins. In the GPIO mode, the internal pull-up of the pins KSI[7:0] is always disabled even if this bit is set.
1	-	-	**Reserved**
0	-	-	**Reserved**

7.5.4.7 Keyboard Scan In [7:0] GPIO Control Register (KSIGCTRLR)

Address Offset: 06h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 GPIO Control (KSI7GCTRL)** 0: KBS mode 1: GPIO mode
6	R/W	0b	**KSI6 GPIO Control (KSI6GCTRL)** 0: KBS mde 1: GPIO mode
5	R/W	0b	**KSI5 GPIO Control (KSI5GCTRL)** 0: KBS mode 1: GPIO mode
4	R/W	0b	**KSI4 GPIO Control (KSI4GCTRL)** 0: KBS mode 1: GPIO mode
3	R/W	0b	**KSI3 GPIO Control (KSI3GCTRL)** 0: KBS mode 1: GPIO mode
2	R/W	0b	**KSI2 GPIO Control (KSI2GCTRL)** 0: KBS mode 1: GPIO mode
1	R/W	0b	**KSI1 GPIO Control (KSI1GCTRL)** 0: KBS mode 1: GPIO mode
0	R/W	0b	**KSI0 GPIO Control (KSI0GCTRL)** 0: KBS mode 1: GPIO mode

7.5.4.8 Keyboard Scan In [7:0] GPIO Output Enable Register (KSIGOENR)

Address Offset: 07h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 GPIO Output Enable (KSI7GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

Bit	R/W	Default	Description
6	R/W	0b	**KSI6 GPIO Output Enable (KSI6GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
5	R/W	0b	**KSI5 GPIO Output Enable (KSI5GOEN)** 0: Disable GPIO output 1: Enblae GPIO output In KBS mode, this bit has no effect.
4	R/W	0b	**KSI4 GPIO Output Enable (KSI4GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
3	R/W	0b	**KSI3 GPIO Output Enable (KSI3GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
2	R/W	0b	**KSI2 GPIO Output Enable (KSI2GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
1	R/W	0b	**KSI1 GPIO Output Enable (KSI1GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
0	R/W	0b	**KSI0 GPIO Output Enable (KSI0GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

7.5.4.9 Keyboard Scan In [7:0] GPIO Data Register (KSIGDATR)

Address Offset: 08h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 GPIO Data (KSI7GDAT)** In the GPIO mode, KSI7 will output this bit if the corresponding Output Enable bit is enabled.
6	R/W	0b	**KSI6 GPIO Data (KSI6GDAT)** In the GPIO mode, KSI6 will output this bit if the corresponding Output Enable bit is enabled.
5	R/W	0b	**KSI5 GPIO Data (KSI5GDAT)** In the GPIO mode, KSI5 will output this bit if the corresponding Output Enable bit is enabled.
4	R/W	0b	**KSI4 GPIO Data (KSI4GDAT)** In the GPIO mode, KSI4 will output this bit if the corresponding Output Enable bit is enabled.
3	R/W	0b	**KSI3 GPIO Data (KSI3GDAT)** In the GPIO mode, KSI3 will output this bit if the corresponding Output Enable bit is enabled.
2	R/W	0b	**KSI2 GPIO Data (KSI2GDAT)** In the GPIO mode, KSI2 will output this bit if the corresponding Output Enable bit is enabled.

Bit	R/W	Default	Description
1	R/W	0b	**KSI1 GPIO Data (KSI1GDAT)** In the GPIO mode, KSI1 will output this bit if the corresponding Output Enable bit is enabled.
0	R/W	0b	**KSI0 GPIO Data (KSI0GDAT)** In the GPIO mode, KSI0 will output this bit if the corresponding Output Enable bit is enabled.

7.5.4.10 Keyboard Scan In [7:0] GPIO Data Mirror Register (KSIGDMRRR)

Address Offset: 09h

Bit	R/W	Default	Description
7	R	0b	**KSI7 GPIO Data Mirror (KSI7GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSI7 status on reads.
6	R	0b	**KSI6 GPIO Data Mirror (KSI6GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSI6 status on reads.
5	R	0b	**KSI5 GPIO Data Mirror (KSI5GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSI5 status on reads.
4	R	0b	**KSI4 GPIO Data Mirror (KSI4GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSI4 status on reads.
3	R	0b	**KSI3 GPIO Data Mirror (KSI3GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSI3 status on reads.
2	R	0b	**KSI2 GPIO Data Mirror (KSI2GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSI2 status on reads.
1	R	0b	**KSI1 GPIO Data Mirror (KSI1GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSI1 status on reads.
0	R	0b	**KSI0 GPIO Data Mirror (KSI0GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSI0 status on reads.

7.5.4.11 Keyboard Scan Out [15:8] GPIO Control Register (KSOHGCTRLR)

Address Offset: 0Ah

Bit	R/W	Default	Description
7	R/W	0b	**KSO15 GPIO Control (KSO15GCTRL)** 0: KBS mode 1: GPIO mode
6	R/W	0b	**KSO14 GPIO Control (KSO14GCTRL)** 0: KBS mode 1: GPIO mode
5	R/W	0b	**KSO13 GPIO Control (KSO13GCTRL)** 0: KBS mode 1: GPIO mode

Bit	R/W	Default	Description
4	R/W	0b	**KSO12 GPIO Control (KSO12GCTRL)** 0: KBS mode 1: GPIO mode
3	R/W	0b	**KSO11 GPIO Control (KSO11GCTRL)** 0: KBS mode 1: GPIO mode
2	R/W	0b	**KSO10 GPIO Control (KSO10GCTRL)** 0: KBS mode 1: GPIO mode
1	R/W	0b	**KSO9 GPIO Control (KSO9GCTRL)** 0: KBS mode 1: GPIO mode
0	R/W	0b	**KSO8 GPIO Control (KSO8GCTRL)** 0: KBS mode 1: GPIO mode

7.5.4.12 Keyboard Scan Out [15:8] GPIO Output Enable Register (KSOHGOENR)

Address Offset: 0Bh

Bit	R/W	Default	Description
7	R/W	0b	**KSO15 GPIO Output Enable (KSO15GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
6	R/W	0b	**KSO14 GPIO Output Enable (KSO14GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
5	R/W	0b	**KSO13 GPIO Output Enable (KSO13GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
4	R/W	0b	**KSO12 GPIO Output Enable (KSO12GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
3	R/W	0b	**KSO11 GPIO Output Enable (KSO11GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
2	R/W	0b	**KSO10 GPIO Output Enable (KSO10GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
1	R/W	0b	**KSO9 GPIO Output Enable (KSO9GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

Bit	R/W	Default	Description
0	R/W	0b	**KSO8 GPIO Output Enable (KSO8GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

7.5.4.13 Keyboard Scan Out [15:8] GPIO Data Mirror Register (KSOHGDMRRR)

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R	0b	**KSO15 GPIO Data Mirror (KSO15GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO15 status on reads.
6	R	0b	**KSO14 GPIO Data Mirror (KSO14GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO14 status on reads.
5	R	0b	**KSO13 GPIO Data Mirror (KSO13GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO13 status on reads.
4	R	0b	**KSO12 GPIO Data Mirror (KSO12GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO12 status on reads.
3	R	0b	**KSO11 GPIO Data Mirror (KSO11GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO11 status on reads.
2	R	0b	**KSO10 GPIO Data Mirror (KSO10GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO10 status on reads.
1	R	0b	**KSO9 GPIO Data Mirror (KSO9GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO9 status on reads.
0	R	0b	**KSO8 GPIO Data Mirror (KSO8GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO8 status on reads.

7.5.4.14 Keyboard Scan Out [7:0] GPIO Control Register (KSOLGCTRLR)

Address Offset: 0Dh

Bit	R/W	Default	Description
7	R/W	0b	**KSO7 GPIO Control (KSO7GCTRL)** 0: KBS mode 1: GPIO mode
6	R/W	0b	**KSO6 GPIO Control (KSO6GCTRL)** 0: KBS mode 1: GPIO mode
5	R/W	0b	**KSO5 GPIO Control (KSO5GCTRL)** 0: KBS mode 1: GPIO mode
4	R/W	0b	**KSO4 GPIO Control (KSO4GCTRL)** 0: KBS mode 1: GPIO mode

Bit	R/W	Default	Description
3	R/W	0b	**KSO3 GPIO Control (KSO3GCTRL)** 0: KBS mode 1: GPIO mode
2	R/W	0b	**KSO2 GPIO Control (KSO2GCTRL)** 0: KBS mode 1: GPIO mode
1	R/W	0b	**KSO1 GPIO Control (KSO1GCTRL)** 0: KBS mode 1: GPIO mode
0	R/W	0b	**KSO0 GPIO Control (KSO0GCTRL)** 0: KBS mode 1: GPIO mode

7.5.4.15 Keyboard Scan Out [7:0] GPIO Output Enable Register (KSOLGOENR)

Address Offset: 0Eh

Bit	R/W	Default	Description
7	R/W	0b	**KSO7 GPIO Output Enable (KSO7GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
6	R/W	0b	**KSO6 GPIO Output Enable (KSO6GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
5	R/W	0b	**KSO5 GPIO Output Enable (KSO5GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
4	R/W	0b	**KSO4 GPIO Output Enable (KSO4GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
3	R/W	0b	**KSO3 GPIO Output Enable (KSO3GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
2	R/W	0b	**KSO2 GPIO Output Enable (KSO2GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
1	R/W	0b	**KSO1 GPIO Output Enable (KSO1GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
0	R/W	0b	**KSO0 GPIO Output Enable (KSO0GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

7.5.4.16 Keyboard Scan Out [7:0] GPIO Data Mirror Register (KSOLGDMRRR)

Address Offset: 0Fh

Bit	R/W	Default	Description
7	R	0b	**KSO7 GPIO Data Mirror (KSO7GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO7 status on reads.
6	R	0b	**KSO6 GPIO Data Mirror (KSO6GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO6 status on reads.
5	R	0b	**KSO5 GPIO Data Mirror (KSO5GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO5 status on reads.
4	R	0b	**KSO4 GPIO Data Mirror (KSO4GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO4 status on reads.
3	R	0b	**KSO3 GPIO Data Mirror (KSO3GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO3 status on reads.
2	R	0b	**KSO2 GPIO Data Mirror (KSO2GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO2 status on reads.
1	R	0b	**KSO1 GPIO Data Mirror (KSO1GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO1 status on reads.
0	R	0b	**KSO0 GPIO Data Mirror (KSO0GDMRR)** In the KBS mode, this bit always returns 0 on reads. In the GPIO mode, this bit returns the pin KSO0 status on reads.

7.5.4.17 KSO0 Low Scan Data Register (KSO0LSDR)

Address Offset: 10h

Bit	R/W	Default	Description
7-0	R	0b	**KSO0 Low Scan Data Register (KSO0LSDR)** This is the 8-bit keyboard scan data at the KSO0 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.18 KSO1 Low Scan Data Register (KSO1LSDR)

Address Offset: 11h

Bit	R/W	Default	Description
7-0	R	0b	**KSO1 Low Scan Data Register (KSO1LSDR)** This is the 8-bit keyboard scan data at the KSO1 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.19 KSO2 Low Scan Data Register (KSO2LSDR)

Address Offset: 12h

Bit	R/W	Default	Description
7-0	R	0b	**KSO2 Low Scan Data Register (KSO2LSDR)** This is the 8-bit keyboard scan data at the KSO2 pin low.The Data Register is available for reading when Scan Data Valid is set.

7.5.4.20 KSO3 Low Scan Data Register (KSO3LSDR)

Address Offset: 13h

Bit	R/W	Default	Description
7-0	R	0b	**KSO3 Low Scan Data Register (KSO3LSDR)** This is the 8-bit keyboard scan data at the KSO3 pin low.The Data Register is available for reading when Scan Data Valid is set.

7.5.4.21 KSO4 Low Scan Data Register (KSO4LSDR)

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R	0b	**KSO4 Low Scan Data Register (KSO4LSDR)** This is the 8-bit keyboard scan data at the KSO4 pin low.The Data Register is available for reading when Scan Data Valid is set.

7.5.4.22 KSO5 Low Scan Data Register (KSO5LSDR)

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R	0b	**KSO5 Low Scan Data Register (KSO5LSDR)** This is the 8-bit keyboard scan data at the KSO5 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.23 KSO6 Low Scan Data Register (KSO6LSDR)

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R	0b	**KSO6 Low Scan Data Register (KSO6LSDR)** This is the 8-bit keyboard scan data at the KSO6 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.24 KSO7 Low Scan Data Register (KSO7LSDR)

Address Offset: 17h

Bit	R/W	Default	Description
7-0	R	0b	**KSO7 Low Scan Data Register (KSO7LSDR)** This is the 8-bit keyboard scan data at the KSO7 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.25 KSO8 Low Scan Data Register (KSO8LSDR)

Address Offset: 18h

Bit	R/W	Default	Description
7-0	R	0b	**KSO8 Low Scan Data Register (KSO8LSDR)** This is the 8-bit keyboard scan data at the KSO8 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.26 KSO9 Low Scan Data Register (KSO9LSDR)

Address Offset: 19h

Bit	R/W	Default	Description
7-0	R	0b	**KSO9 Low Scan Data Register (KSO9LSDR)** This is the 8-bit keyboard scan data at the KSO9 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.27 KSO10 Low Scan Data Register (KSO10LSDR)

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R	0b	**KSO10 Low Scan Data Register (KSO10LSDR)** This is the 8-bit keyboard scan data at the KSO10 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.28 KSO11 Low Scan Data Register (KSO11LSDR)

Address Offset: 1Bh

Bit	R/W	Default	Description
7-0	R	0b	**KSO11 Low Scan Data Register (KSO11LSDR)** This is the 8-bit keyboard scan data at the KSO11 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.29 KSO12 Low Scan Data Register (KSO12LSDR)

Address Offset: 1Ch

Bit	R/W	Default	Description
7-0	R	0b	**KSO12 Low Scan Data Register (KSO12LSDR)** This is the 8-bit keyboard scan data at the KSO12 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.30 KSO13 Low Scan Data Register (KSO13LSDR)

Address Offset: 1Dh

Bit	R/W	Default	Description
7-0	R	0b	**KSO13 Low Scan Data Register (KSO13LSDR)** This is the 8-bit keyboard scan data at the KSO13 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.31 KSO14 Low Scan Data Register (KSO14LSDR)

Address Offset: 1Eh

Bit	R/W	Default	Description
7-0	R	0b	**KSO14 Low Scan Data Register (KSO14LSDR)** This is the 8-bit keyboard scan data at the KSO14 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.32 KSO15 Low Scan Data Register (KSO15LSDR)

Address Offset: 1Fh

Bit	R/W	Default	Description
7-0	R	0b	**KSO15 Low Scan Data Register (KSO15LSDR)** This is the 8-bit keyboard scan data at the KSO15 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.33 KSO16 Low Scan Data Register (KSO16LSDR)

Address Offset: 20h

Bit	R/W	Default	Description
7-0	R	0b	**KSO16 Low Scan Data Register (KSO16LSDR)** This is the 8-bit keyboard scan data at the KSO16 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.34 KSO17 Low Scan Data Register (KSO17LSDR)

Address Offset: 21h

Bit	R/W	Default	Description
7-0	R	0b	**KSO17 Low Scan Data Register (KSO17LSDR)** This is the 8-bit keyboard scan data at the KSO17 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.5.4.35 Scan Data Control1 Register (SDC1R)

Address Offset: 22h

Bit	R/W	Default	Description
7	R/W	0b	**Scan Data Enable (SDEN)** 0: Disable 1: Enable
6	-	-	**Reserved**
5	R/W	0b	**Interrupt from Scan Data Valid Enable (INTSDVEN)** 0: Disable valid interrupt to INT84 1: Enable valid interrupt to INT84
4-3	-	-	**Reserved**

Bit	R/W	Default	Description
2-0	R/W	001b	**Scan Loop Select (SLS)** 000b: Reserved 001b: 2 round 010b: 3 round 011b: 4 round 100b: 5 round 101b: 6 round 110b: 7 round 111b: 8 round

7.5.4.36 Scan Data Control2 Register (SDC2R)

The following timing is based on clk_ec = 8MHz.

Address Offset: 23h

Bit	R/W	Default	Description
7-6	R/W	00b	**KSO Pin Count Select (KSOPCS)** 00: 8x16 01: 8x17 10: 8x18 11: Reserved
5-4	-	-	**Reserved**
3-0	R/W	0h	**Wait KSO High Delay (WKSOHDLY)** 0h: 26 us 1h: 36 us 2h: 45 us 3h: 54 us 4h: 63 us 5h: 72 us 6h: 82 us 7h: 91 us 8h: 100 us 9h: 109 us Others: Reserved

7.5.4.37 Scan Data Control3 Register (SDC3R)

The following timing is based on clk_ec = 8MHz.

Address Offset: 24h

Bit	R/W	Default	Description
7-4	R/W	0h	**Wait KSO Low Delay (WKSOLDLY)** 0h: 13 us 1h: 15 us 2h: 17 us 3h: 20 us 4h: 22 us 5h: 24 us 6h: 26 us 7h: 29 us 8h: 31 us 9h: 33 us Others: Reserved
3-0	R/W	0h	**Spacing Delay Between Rounds (SDLYBR)** 0h: 0 ms 1h: 1.15 ms 2h: 2.30 ms 3h: 3.45 ms 4h: 4.60 ms 5h: 5.75 ms 6h: 6.90 ms 7h: 8.05 ms 8h: 9.20 ms 9h: 10.35 ms Ah: 11.50 ms Bh: 12.65 ms Ch: 13.80 ms Dh: 14.95 ms Eh: 16.10 ms Fh: 17.25 ms

7.5.4.38 Scan Data Status Register (SDSR)

Address Offset: 25h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/WC	0b	**Scan Data Valid (SDV)** This bit is write cleared. 0: Data not available 1: Data valid

7.5.4.39 Keyboard Scan In [7:0] GPIO Open-Drain Register (KSIGPODR)

Address Offset: 26h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 Output Open-Drain Enable (KSI7ODEN)** 0b: Configure KSI7 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSI7 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
6	R/W	0b	**KSI6 Output Open-Drain Enable (KSI6ODEN)** 0b: Configure KSI6 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSI6 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
5	R/W	0b	**KSI5 Output Open-Drain Enable (KSI5ODEN)** 0b: Configure KSI5 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSI5 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
4	R/W	0b	**KSI4 Output Open-Drain Enable (KSI4ODEN)** 0b: Configure KSI4 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSI4 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
3	R/W	0b	**KSI3 Output Open-Drain Enable (KSI3ODEN)** 0b: Configure KSI3 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSI3 as open-drain if this pin is set to GPO.
2	R/W	0b	**KSI2 Output Open-Drain Enable (KSI2ODEN)** 0b: Configure KSI2 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSI2 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
1	R/W	0b	**KSI1 Output Open-Drain Enable (KSI1ODEN)** 0b: Configure KSI1 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSI1 as open-drain if this pin is set to GPO.
0	R/W	0b	**KSI0 Output Open-Drain Enable (KSI0ODEN)** 0b: Configure KSI0 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSI0 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.

7.5.4.40 Keyboard Scan Out [15:8] GPIO Open-Drain Register (KSOHGPODR)

Address Offset: 27h

Bit	R/W	Default	Description
7	R/W	0b	**KSO15 Output Open-Drain Enable (KSO15ODEN)** 0b: Configure KSO15 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO15 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.

Bit	R/W	Default	Description
6	R/W	0b	**KSO14 Output Open-Drain Enable (KSO14ODEN)** 0b: Configure KSO14 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO14 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
5	R/W	0b	**KSO13 Output Open-Drain Enable (KSO13ODEN)** 0b: Configure KSO13 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO13 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
4	R/W	0b	**KSO12 Output Open-Drain Enable (KSO12ODEN)** 0b: Configure KSO12 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO12 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
3	R/W	0b	**KSO11 Output Open-Drain Enable (KSO11ODEN)** 0b: Configure KSO11 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO11 as open-drain if this pin is set GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
2	R/W	0b	**KSO10 Output Open-Drain Enable (KSO10ODEN)** 0b: Configure KSO10 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO10 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
1	R/W	0b	**KSO9 Output Open-Drain Enable (KSO9ODEN)** 0b: Configure KSO9 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO9 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
0	R/W	0b	**KSO8 Output Open-Drain Enable (KSO8ODEN)** 0b: Configure KSO8 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO8 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.

7.5.4.41 Keyboard Scan Out [7:0] GPIO Open-Drain Register (KSOLGPODR)

Address Offset: 28h

Bit	R/W	Default	Description
7	R/W	0b	**KSO7 Output Open-Drain Enable (KSO7ODEN)** 0b: Configure KSO7 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO7 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
6	R/W	0b	**KSO6 Output Open-Drain Enable (KSO6ODEN)** 0b: Configure KSO6 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO6 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.

Bit	R/W	Default	Description
5	R/W	0b	**KSO5 Output Open-Drain Enable (KSO5ODEN)** 0b: Configure KSO5 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO5 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
4	R/W	0b	**KSO4 Output Open-Drain Enable (KSO4ODEN)** 0b: Configure KSO4 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO4 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
3	R/W	0b	**KSO3 Output Open-Drain Enable (KSO3ODEN)** 0b: Configure KSO3 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO3 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
2	R/W	0b	**KSO2 Output Open-Drain Enable (KSO2ODEN)** 0b: Configure KSO2 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO2 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
1	R/W	0b	**KSO1 Output Open-Drain Enable (KSO1ODEN)** 0b: Configure KSO1 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO1 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.
0	R/W	0b	**KSO0 Output Open-Drain Enable (KSO0ODEN)** 0b: Configure KSO0 as push-pull if this pin is set to GPO. The internal pull-up is disabled if this pin is set to GPO or GPI. 1b: Configure KSO0 as open-drain if this pin is set to GPO. The internal pull-up is enabled if this pin is set to GPO or GPI.

7.6 General Purpose I/O Port (GPIO)

7.6.1 Overview

The General Purpose I/O Port is composed of independent I/O pins controlled by registers.

7.6.2 Features

- I/O pins individually configured as input, output or alternate function
- Supports 86-port GPIO with serial flash
- Configurable internal pull-up resistors
- Configurable internal pull-down resistors
- Supports Schmitt-Trigger input on all ports except group I and group J

7.6.3 EC Interface Registers

The EC interface registers are listed below. The base address for GPIO is 1600h.

Table 7-7. EC View Register Map, GPIO

7 0	Offset
General Control Register (GCR)	00h
General Control 1 Register (GCR1)	F0h
General Control 2 Register (GCR2)	F1h
General Control 3 Register (GCR3)	F2h
General Control 4 Register (GCR4)	F3h
General Control 5 Register (GCR5)	F4h
General Control 6 Register (GCR6)	F5h
General Control 7 Register (GCR7)	F6h
General Control 8 Register (GCR8)	F7h
General Control 9 Register (GCR9)	F8h
General Control 10 Register (GCR10)	F9h
General Control 11 Register (GCR11)	FAh
General Control 12 Register (GCR12)	FBh
General Control 13 Register (GCR13)	FCh
General Control 14 Register (GCR14)	FDh
General Control 15 Register (GCR15)	FEh
Power Good Watch Control Register (PGWCR)	FFh
General Control 16 Register (GCR16)	E0h
General Control 17 Register (GCR17)	E1h
General Control 18 Register (GCR18)	E2h
General Control 19 Register (GCR19)	E4h
General Control 20 Register (GCR20)	E5h
General Control 21 Register (GCR21)	E6h
General Control 22 Register (GCR22)	E7h
General Control 23 Register (GCR23)	E8h
General Control 24 Register (GCR24)	E9h
General Control 29 Register (GCR29)	EEh
General Control 27 Register (GCR27)	D3h
General Control 28 Register (GCR28)	D4h
General Control 31 Register (GCR31)	D5h
General Control 32 Register (GCR32)	D6h
General Control 33 Register (GCR33)	D7h
General Control 30 Register (GCR30)	EDh
Port Data Register (GPDRA)	01h

7	0	Offset
Port Data Register (GPDRB)		02h
…		…
Port Data Register (GPDRJ)		0Ah
Port Data Register (GPDRM)		0Dh
Port Control n Registers (GPCRA0)		10h
Port Control n Registers (GPCRA1)		11h
…		…
Port Control n Registers (GPCRJ5)		5Dh
Port Control n Registers (GPCRM0)		A0h
...		...
Port Control n Registers (GPCRM6)		A6h
Port Data Mirror Register (GPDMRA)		61h
Port Data Mirror Register (GPDMRB)		62h
…		…
Port Data Mirror Register (GPDMRJ)		6Ah
Port Data Mirror Register (GPDMRM)		6Dh
Output Type Register (GPOTA)		71h
Output Type Register (GPOTB)		72h
Output Type Register (GPOTC)		73h
Output Type Register (GPOTD)		74h
Output Type Register (GPOTE)		75h
Output Type Register (GPOTF)		76h
Output Type Register (GPOTG)		77h
Output Type Register (GPOTH)		78h
Output Type Register (GPOTI)		79h
Output Type Register (GPOTJ)		7Ah
Output Type Register (GPOTM)		7Dh

7.6.3.1 General Control Register (GCR)

This register individually controls the bus state of each port. The input gating and output floating control signals can be used to reduce power consumption in various system conditions.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	0h	**GPB5 Follow LPCRST# Enable (GFLE)** 1: Refer to GFLES0 bit in this register. 0: Otherwise Note that GA20 is function 1 of GPB5, LPCRST# is function 1 of GPD2 and WUI4 is function 2 of GPD2.
6-3	-	-	**Reserved**
2-1	R/W	10b	**LPC Reset Enable (LPCRSTEN)** 00: Reserved 01: LPC Reset is enabled on GPB7. 10: LPC Reset is enabled on GPD2. 11: LPC Reset is disabled.
0	R/W	0b	**GFLE Set (GFLES0)** 1: GPDRB bit 5 will be set if WUI4 is level-low. 0: GPDRB bit 5 will be set immediately if there is a high-to-low transition on WUI4. If this “set” action occurs between a “reading from GPDRB” and “writing to GPDRB”, the GPDRB bit 5 is not writable in the “writing to GPDRB” action.

7.6.3.2 General Control 1 Register (GCR1)

Address Offset: F0h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-4	R/W	00b	**SPI Control (SPICTRL)** If this field is zero, the corresponding function 3 of SPI is disabled. Otherwise, partial of them will be set as function 3 if their corresponding GPCRn is 00b. 00b: SPI channel 0 and channel 1 are disabled. 10b: SSCK/SMOSI/SMISO/SSCE1# are enabled. 01b: SSCK/SMOSI/SMISO/SSCE0# are enabled. 11b: SSCK/SMOSI/SMISO/SSCE1#/SSCE0# are enabled.
3-2	R/W	00b	**UART2 Control (U2CTRL)** If this field is zero, the corresponding function 3 of UART2 is disabled. Otherwise, partial or all of them will be set as function 3 if their corresponding GPCRn is 00b. 00b: UART2 is disabled. 01b: SIN1/SOUT1 are enabled. 10b: SIN1/SOUT1/DSR1#/RTS1#/DTR1#/CTS1#/DCD1# are enabled. 11b: SIN1/SOUT1/DSR1#/RTS1#/DTR1#/CTS1#/DCD1#/RIG1# are enabled.
1-0	R/W	00b	**UART1 Control (U1CTRL)** If this field is zero, the corresponding function 3 of UART1 is disabled. Otherwise, partial or all of them are set as function 3 if their corresponding GPCRn is 00b. 00b: UART1 is disabled. 01b: SIN0/SOUT0 are enabled. 10b: SIN0/SOUT0/DSR0#/RTS0#/DTR0#/CTS0#/DCD0# are enabled. 11b: SIN0/SOUT0/DSR0#/RTS0#/DTR0#/CTS0#/DCD0#/RIG0# are enabled.

7.6.3.3 General Control 2 Register (GCR2)

Address Offset: F1h

Bit	R/W	Default	Description
7	R/W	0b	**TACH2 Enable (TACH2E)** Refer to Table 7-8. GPIO Alternate Function on page 254.
6	R/W	0b	**CK32K Out Enable (CK32OE)** Refer to Table 7-8. GPIO Alternate Function on page 254.
5	R/W	0b	**SMBus Channel 3 Enable (SMB3E)** Refer to Table 7-8. GPIO Alternate Function on page 254.
4	R/W	0b	**PECI Enable (PECIE)** Refer to Table 7-8. GPIO Alternate Function on page 254.
3-0	-	-	**Reserved**

7.6.3.4 General Control 3 Register (GCR3)

If VCC power-down and I/O port pins have been configured as their respective alternative function mode, enabling these bits will turn off corresponding I/O port pins.

Address Offset: F2h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	1b	**PECI VCC Power-down Gating (PECIPDG)** 0b: Disable 1b: Turn off PECI related pins if VCC powers down.
5	R/W	0b	**UART2 VCC Power-down Gating (UART2PDG)** 0b: Disable 1b: Turn off UART2 related pins if VCC power-down.
4	R/W	0b	**UART1 VCC Power-down Gating (UART1PDG)** 0b: Disable 1b: Turn off UART1 related pins if VCC powers down.
3	R/W	0b	**SSPI VCC Power-down Gating (SSPIPDG)** 0b: Disable 1b: Turn off SSPI related pins if VCC powers down.
2	-	-	**Reserved**
1	R/W	0b	**ECSMI#/ECSCI# VCC Power-down Gating (EEPDG)** 0b: Disable 1b: Turn off ECSMI#/ECSCI# related pins if VCC powers down. Please note that this feature is regardless of the GPMD field in GPCR register for EEPDG bit.
0	R/W	0b	**CLKRUN#/GA20/KBRST# VCC Power-down Gating (CGKPDG)** 0b: Disable 1b: Turn off CLKRUN#/GA20/KBRST# related pins if VCC powers down. Please note that the GPMD field in GPCR register for CGKPDG bit has no impact on this feature.

7.6.3.5 General Control 4 Register (GCR4)

Address Offset: F3h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R/W	000b	**Hardware Bypass Enable (HWBPE)** 000b: Disable 001b: GPI6 input will be directly bypassed to BAO. 010b: GPI7 input willl be directly bypassed to BBO. 011b: GPI6/GPI7 input will be directly bypassed to BAO/BBO. 101b: GPI6 input will be directly bypassed to BAO and BBO. Others: Reserved

7.6.3.6 General Control 5 Register (GCR5)

Address Offset: F4h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	000b	**Power Good Watch Delay Time (PLR2DLY)** These bits control the delay time of Power Good Watch function. 000b: about 100 ms. 001b: about 500 ms. 010b: about 1000 ms. 011b: about 1500 ms. 100b: about 2000 ms. 101b: about 2500 ms. 110b: about 3000 ms. 111b: about 4000 ms.
3	R/W	0b	**Power Good Drop Pin Select (PGDRPSEL)** This bit controls the selection of the drop pins while power good watch condition occurs. 0b: GPB5-7 and GPH0-6 will be reset. 1b: GPB5-7 will be reset.
2	R/W	0b	**Power Good Watch Enable (PGOODEN)** 0b: Power Good Watch function is disabled. 1b: Power Good Watch function is enabled. This bit will be cleared when power good watch condition is detected. Please note that whether GPH0-6 will be reset or not is controlled by the PGDRPSEL bit.
1	R/W	0b	**TACH1B Enable (T1BEN)** 0b: Disable 1b: GPJ3 will select TACH1B as its alternative function. Refer to Table 7-8. GPIO Alternate Function on page 254.
0	R/W	0b	**TACH0B Enable (T0BEN)** 0b: Disable 1b: GPJ2 will select TACH0B as its alternative function. Refer to Table 7-8. GPIO Alternate Function on page 254.

7.6.3.7 General Control 6 Register (GCR6)

Address Offset: F5h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**Power Good Watch Pin Select (PGWPSEL)** This bit controls the selection of the watch pin in power good watch function. 0b: GPH4 is selected. 1b: GPE0 is selected.
4	-	-	**Reserved**
3	R/W	1b	**UART SOUT1 Enable (SOUT1EN)** This bit enables the transmitter of UART2 separately. 0b: SOUT1 is disabled. 1b: SOUT1 is enabled.

Bit	R/W	Default	Description
2	R/W	1b	**UART SIN1 Enable (SIN1EN)** This bit enables the receiver of UART2 separately. 0b: SIN1 is disabled. 1b: SIN1 is enabled.
1	R/W	1b	**UART SOUT0 Enable (SOUT0EN)** This bit enables the transmitter of UART1 separately. 0b: SOUT0 is disabled. 1b: SOUT0 is enabled.
0	R/W	1b	**UART SIN0 Enable (SIN0EN)** This bit enables the receiver of UART1 separately. 0b: SIN0 is disabled. 1b: SIN0 is enabled.

7.6.3.8 General Control 7 Register (GCR7)

Address Offset: F6h

Bit	R/W	Default	Description
7	R/W	0b	**SMCLK2 Pin Switch (SMCLK2PS)** 0b: SMCLK2 is located on GPF6. 1b: SMCLK2 is located on GPC7. Refer to Table 7-8. GPIO Alternate Function on page 254.
6-0	-	-	**Reserved**

7.6.3.9 General Control 8 Register (GCR8)

Address Offset: F7h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**PWRSW WDT 2 Enable 1 (PWSW2EN1)** A timeout reset event will be asserted to reset EC after PWRSW has been pulled low for more than a determined period indicated by PWDT2CNTR on page 240. Write 1b: Set bit and enable WDT 2. Write 0b: Ignored Read returns the last written data. Once the bit is set, it cannot be disabled again unleses VSTBY Power-Up Reset or Warm Reset is enabled.
3-2	R/W	00b	**UART2 Control 2 (U2CTRL2)** If this field is zero, the corresponding function 3 of UART2 is disabled when U2CTRL is set to 00b. Otherwise, partial or all of them will be set as function 3 if their corresponding GPCRn is 00b. 00b: UART2 is disabled when U2CTRL is set to 00b. 01b: SIN1/SOUT1/RTS1# are enabled. 10b: SIN1/SOUT1/RTS1#/CTS1# are enabled. 11b: SIN1/SOUT1/DSR1#/RTS1#/DTR1#/CTS1# are enabled.

Bit	R/W	Default	Description
1-0	R/W	00b	**UART1 Control 2 (U1CTRL2)** If this field is zero, the corresponding function 3 of UART1 is disabled when U1CTRL is set to 00b. Otherwise, partial or all of them are set as function 3 if their corresponding GPCRn is 00b. 00b: UART1 is disabled when U1CTRL is set to 00b. 01b: SIN0/SOUT0/RTS0# are enabled. 10b: SIN0/SOUT0/RTS0#/CTS0# are enabled. 11b: SIN0/SOUT0/DSR0#/RTS0#/DTR0#/CTS0# are enabled.

7.6.3.10 General Control 9 Register (GCR9)

Address Offset: F8h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**PWRSW WDT 2 Enable 2 (PWSW2EN2)** A timeout reset event will be asserted to reset EC after PWRSW has been pulled low for more than a determined period indicated by PWDT2CNTR on page 240. 0b: Disable 1b: Dedicate PWRSW to timeout reset function. Write 1b: Set bit and enable WDT 2. Write 0b: Clear bit. The WDT 2 is enabled by (PWSW2EN1 | PWSW2EN2) Read returns the last written data.
4	-	-	**Reserved**
3	R/W	0b	**PWRSW WDT 2 GPO Output Enable (PWSWDT2GPEN)** A timeout reset event will be asserted to generate a low pulse on GPI5 after PWRSW has been pulled low for more than a determined period. 0b: Disable 1b: Enable **Note: GPI5 should be alternate function.**
2	W	0b	**PWRSW WDT 1 Enable 2 (PWSW1EN2)** A timeout reset event will be asserted to reset EC after PWRSW has been pulled low for more than a determined period indicated by PWDT1CNTR on page 240. Write 1b: Set bit, enable WDT 1, and touch (re-start) WDT 1. Write 0b: Clear bit. The WDT 1 is enabled by (PWSW1EN1 | PWSW1EN2) Read returns the last written data.
1	R/W	0b	**PWRSW WDT 1 Enable 1 (PWSW1EN1)** A timeout reset event will be asserted to reset EC after PWRSW has been pulled low for more than a determined period indicated by PWDT1CNTR on page 240. Write 1b: Set bit and enable WDT 1. Write 0b: Ignored Read returns the last written data. Once the bit is set, it cannot be disabled again unless VSTBY Power-Up Reset or Warm Reset is enabled.

Bit	R/W	Default	Description
0	R/W	0b	**Check PWRSW (CHKPWRSW)** 0: WDT1/2 counts only if PWRSW low, otherwise cleared. 1: WDT1/2 counts only if PWRSW low and GPE6 high, otherwise cleared.

7.6.3.11 General Control 10 Register (GCR10)

Address Offset: F9h

Bit	R/W	Default	Description
7-5	R/W	000b	**PWRSW WDT 2 Output Reset Pulse Width (PWSW2RPW)** This is the generated pulse width on GPI5 after PWRSW has been pulled low for more than a determined period. 000b: 30 us 001b: 200 ms 010b: 3 sec Others: Reserved **Note:** It also means delay 30 us/200 ms/3 sec to reset EC.
4-3	-	-	**Reserved**
2-0	R/W	000b	**PWRSW WDT 2 Counter Byte (PWDT2CNTR)** Selective WDT 2 timeout periods. 000b: 10 sec 001b: 8 sec 010b: 12 sec 100b: 7.5 sec 111b: 15 sec Others: Reserved The register content is not writable if PWSW2EN is set. The register content is reloaded when the counter state is from “clear” to “count”.

7.6.3.12 General Control 11 Register (GCR11)

Address Offset: FAh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0000b	**PWRSW WDT 1 Counter Byte (PWDT1CNTR)** Selective WDT 1 timeout periods. 0000b: 4sec 0001b: 5sec 0010b: 6sec 0011b: 7sec 0100b: 8sec 0101b: 9sec 0110b: 10sec 0111b: 11sec 1100b: 12sec Others: Reserved The register content is reloaded when the counter state is from “clear” to “count”.

7.6.3.13 General Control 12 Register (GCR12)

Address Offset: FBh

Bit	R/W	Default	Description
7-0	R/W	00h	**GPIO Lock Authentication Data (GLAD)** The lock state is default off. Write: If the lock state is off, write Auth. Data will enable the lock state. If the lock state is on, write the same Auth. Data will disable the lock state. Read: 00h: The lock state is off. 01h: The lock state is on.

7.6.3.14 General Control 13 Register (GCR13)

Address Offset: FCh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**GPJ0 Lock Enable (GPJ0LE)** Enabling this bit will lock the output state of GPJ0. **Note**: This bit can be changed only when the lock state is off.
1	R/W	0b	**GPD7 Lock Enable (GPD7LE)** Enabling this bit will lock the output state of GPD7. **Note**: This bit can be changed only when the lock state is off.
0	R/W	0b	**GPD6 Lock Enable (GPD6LE)** Enabling this bit will lock the output state of GPD6. **Note**: This bit can be changed only when the lock state is off.

7.6.3.15 General Control 14 Register (GCR14)

Address Offset: FDh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**WUI Debounce Independent Enable (WUIDIE)** Debounce Independent for WUI0, WUI1, WUI2, WUI3, WUI5 and PWRSW. 0b: Disable 1b: Enable
2-0	R/W	0h	**WUI Debounce Select (WUIDS)** Debounce WUI inputs from WUI0, WUI1, WUI2, WUI3, WUI5 and PWRSW. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec

7.6.3.16 General Control 15 Register (GCR15)

Address Offset: FEh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**Comparator 2 GPIO Enable (CMP2GPEN)** Comparator 2 output to GPJ5 0b: Disable 1b: Enable
1	R/W	0b	**Comparator 1 GPIO Enable (CMP1GPEN)** Comparator 1 output to GPJ4 0b: Disable 1b: Enable
0	R/W	0b	**Comparator 0 GPIO Enable (CMP0GPEN)** Comparator 0 output to GPJ3 0b: Disable 1b: Enable

7.6.3.17 Power Good Watch Control Register (PGWCR)

Address Offset: FFh

Bit	R/W	Default	Description
7	R/W	0b	**Power Good Watch Mode 1 Enable (PGWM1EN)** 1b: Enable Power good watch mode 1 with the use of PGWFS to decide go back or not. 0b: Otherwise.
6	R/WC	0b	**Power Good Watch Flag Status (PGWFS)** This bit will be cleared when a timeout reset event of power good watch occurs. This bit will be cleared when PGWM1EN is cleared.
5-4	-	-	**Reserved**
3	R/W	0b	**PWRSW WDT 2 to Drop Low Enable (PWSW2DLEN)** 1b: A timeout reset event from PWRSW WDT 2 occurs. It will drop power good watch pin to low and delay 1 second before EC is reset. 0b: A timeout reset event from PWRSW WDT 2 occurs and EC will be reset immediately.
2-0	-	-	**Reserved**

7.6.3.18 General Control 16 Register (GCR16)

Address Offset: E0h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	0h	**WUI1 Debounce Select (WUI1DS)** Debounce WUI inputs from WUI1. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec
3	-	-	**Reserved**
2-0	R/W	0h	**WUI0 Debounce Select (WUI0DS)** Debounce WUI inputs from WUI0. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec

7.6.3.19 General Control 17 Register (GCR17)

Address Offset: E1h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	0h	**WUI3 Debounce Select (WUI3DS)** Debounce WUI inputs from WUI3. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec
3	-	-	**Reserved**
2-0	R/W	0h	**WUI2 Debounce Select (WUI2DS)** Debounce WUI inputs from WUI2. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec

7.6.3.20 General Control 18 Register (GCR18)

Address Offset: E2h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	0h	**WUI5 Debounce Select (WUI5DS)** Debounce WUI inputs from WUI5. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec
3	-	-	**Reserved**
2-0	R/W	0h	**PWRSW Debounce Select (PWRSWDS)** Debounce WUI inputs from PWRSW. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec

7.6.3.21 General Control 19 Register (GCR19)

Address Offset: E4h

Bit	R/W	Default	Description
7	R/W	0b	**GPB5 Input Voltage Selection (GPB5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
6	R/W	0b	**GPB6 Input Voltage Selection (GPB6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
5	R/W	1b	**GPC1 Input Voltage Selection (GPC1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
4	R/W	1b	**GPC2 Input Voltage Selection (GPC2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
3	R/W	0b	**GPC7 Input Voltage Selection (GPC7VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

Bit	R/W	Default	Description
2	R/W	0b	**GPD0 Input Voltage Selection (GPD0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
1	R/W	0b	**GPD1 Input Voltage Selection (GPD1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
0	R/W	1b	**GPD2 Input Voltage Selection (GPD2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

7.6.3.22 General Control 20 Register (GCR20)

Address Offset: E5h

Bit	R/W	Default	Description
7	R/W	0b	**GPD3 Input Voltage Selection (GPD3VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
6	R/W	0b	**GPD4 Input Voltage Selection (GPD4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
5	R/W	1b	**GPE0 Input Voltage Selection (GPE0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
4	R/W	0b	**GPE6 Input Voltage Selection (GPE6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
3	R/W	1b	**GPE7 Input Voltage Selection (GPE7VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
2	R/W	1b	**GPF2 Input Voltage Selection (GPF2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
1	R/W	1b	**GPF3 Input Voltage Selection (GPF3VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
0	R/W	1b	**GPF4 Input Voltage Selection (GPF4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

7.6.3.23 General Control 21 Register (GCR21)

Address Offset: E6h

Bit	R/W	Default	Description
7	R/W	1b	**GPF5 Input Voltage Selection (GPF5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
6	R/W	1b	**GPF6 Input Voltage Selection (GPF6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
5	R/W	1b	**GPF7 Input Voltage Selection (GPF7VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
4	R/W	0b	**GPG1 Input Voltage Selection (GPG1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
3	R/W	0b	**GPG6 Input Voltage Selection (GPG6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
2	R/W	0b	**GPH0 Input Voltage Selection (GPH0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
1	R/W	1b	**GPH1 Input Voltage Selection (GPH1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
0	R/W	1b	**GPH2 Input Voltage Selection (GPH2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

7.6.3.24 General Control 22 Register (GCR22)

Address Offset: E7h

Bit	R/W	Default	Description
7	R/W	0b	**GPC0 Input Voltage Selection (GPC0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable internal pull-up if this bit is set to one.
6	R/W	0b	**GPD7 Input Voltage Selection (GPD7VS)** 0b: 3.3V. 1b: 1.8V. Do not enable internal pull-up if this bit is set to one.
5	R/W	0b	**GPD6 Input Voltage Selection (GPD6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable internal pull-up if this bit is set to one.

Bit	R/W	Default	Description
4	R/W	0b	**GPD5 Input Voltage Selection (GPD5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable internal pull-up if this bit is set to one.
3	R/W	0b	**GPE5 Input Voltage Selection (GPE5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable internal pull-up if this bit is set to one.
2	R/W	0b	**GPE4 Input Voltage Selection (GPE4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable internal pull-up if this bit is set to one.
1	R/W	1b	**GPB3 Input Voltage Selection (GPB3VS)** 0b: 3.3V. 1b: 1.8V. Do not enable internal pull-up if this bit is set to one.
0	R/W	1b	**GPB4 Input Voltage Selection (GPB4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable internal pull-up if this bit is set to one.

7.6.3.25 General Control 23 Register (GCR23)

Address Offset: E8h

Bit	R/W	Default	Description
7	R/W	1b	**GPI4 Input Voltage Selection (GPI4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
6	R/W	1b	**GPI3 Input Voltage Selection (GPI3VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
5	R/W	1b	**GPI2 Input Voltage Selection (GPI2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
4	R/W	1b	**GPI1 Input Voltage Selection (GPI1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
3	R/W	1b	**GPJ3 Input Voltage Selection (GPJ3VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
2	R/W	1b	**GPJ2 Input Voltage Selection (GPJ2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

Bit	R/W	Default	Description
1	R/W	1b	**GPJ1 Input Voltage Selection (GPJ1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
0	R/W	1b	**GPJ0 Input Voltage Selection (GPJ0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

7.6.3.26 General Control 24 Register (GCR24)

Address Offset: E9h

Bit	R/W	Default	Description
7	R/W	0b	**Toggle mode of GPDR (TMGPDR)** When toggle mode is enable and in GPO mode, write 1 to the bits of GPDR will make output pin be inversed; Write 0 to the bits of GPDR will not change the output pin. 0b: Disable 1b: Enable toggle mode.
6	R/W	0b	**GPA7 Input Voltage Selection (GPA7VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
5	R/W	0b	**GPA6 Input Voltage Selection (GPA6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
4	-	-	**Reserved**
3	R/W	0b	**GPC6 Input Voltage Selection (GPC6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
2	R/W	0b	**GPC4 Input Voltage Selection (GPC4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
1	R/W	1b	**GPA5 Input Voltage Selection (GPA5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
0	R/W	1b	**GPA4 Input Voltage Selection (GPA4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

7.6.3.27 General Control 27 Register (GCR27)

Address Offset: D3h

Bit	R/W	Default	Description
7	R/W	0b	**GPH5 Input Voltage Selection (GPH5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
6	R/W	0b	**GPI7 Input Voltage Selection (GPI7VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
5	R/W	0b	**GPI6 Input Voltage Selection (GPI6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
4	R/W	0b	**GPI5 Input Voltage Selection (GPI5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
3	R/W	0b	**GPI0 Input Voltage Selection (GPI0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
2	R/W	0b	**GPJ6 Input Voltage Selection (GPJ6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
1	R/W	0b	**GPJ5 Input Voltage Selection (GPJ5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
0	R/W	0b	**GPJ4 Input Voltage Selection (GPJ4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

7.6.3.28 General Control 28 Register (GCR28)

Address Offset: D4h

Bit	R/W	Default	Description
7	R/W	0b	**GPE2 Input Voltage Selection (GPE2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
6	R/W	0b	**GPE1 Input Voltage Selection (GPE1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
5	R/W	0b	**GPF1 Input Voltage Selection (GPF1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

Bit	R/W	Default	Description
4	R/W	0b	**GPF0 Input Voltage Selection (GPF0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
3	R/W	0b	**GPG2 Input Voltage Selection (GPG2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
2	R/W	0b	**GPG0 Input Voltage Selection (GPG0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
1	-	-	**Reserved**
0	R/W	0b	**GPH6 Input Voltage Selection (GPH6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

7.6.3.29 General Control 31 Register (GCR31)

Address Offset: D5h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

7.6.3.30 General Control 32 Register (GCR32)

Address Offset: D6h

Bit	R/W	Default	Description
7-04	-	-	**Reserved**

7.6.3.31 General Control 33 Register (GCR33)

Address Offset: D7h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**GPJ7 Input Voltage Selection (GPJ7VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
1-0	-	-	**Reserved**

7.6.3.32 General Control 30 Register (GCR30)

Address Offset: EDh

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4-2	R/W	000b	**VCC Power Domain Select (VCCPDS[2:0])** 000b: VCC is supplied by 3.3V for LPC. 100b: VCC is supplied by 1.8V eSPI/LPC. R_{on} is eSPI spec. value. 101b: VCC is supplied by 1.8V eSPI/LPC. R_{on} is eSPI spec. value + 5 ohm. 110b: VCC is supplied by 1.8V eSPI/LPC. R_{on} is eSPI spec. value + 10 ohm. Others: Reserved. The VCCPDS[2] is internally gated to 1 if it's configured as eSPI in 16-byte signature.
1-0	-	-	**Reserved**

7.6.3.33 General Control 29 Register (GCR29)

Address Offset: EEh

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**GPM6 Power Domain Select (GPM6PDS)** 0b: Reserved 1b: ALERT#/SERIRQ/GPM6 is supplied by VCC.

7.6.3.34 Port Data Registers A-M (GPDRA-M)

The Port Data register (GPDR) is an 8-bit register. The pin function is controlled by Port Control Register (GPCRn). When the pin function is set to be a general output pin, the value of the GPDRx bit is directly output to its corresponding pin. When the pin function is set to be a general input pin, the pin level status can be detected by reading the corresponding register bit. Each register contains one group which has eight ports at most.

Address Offset: 01h-0Dh

Bit	R/W	Default	Description
7-0	R/W	GPDRG[0]: 1b Otherwise: 0b	**Port Data Register (GPDRn[7:0])** When the pin function is set to be a general output pin, the value of this bit is directly output to its corresponding pin. In the output mode, reading returns the last written data to GPDRn. In other modes, reading this register returns the pin level status. For group I/J, the return data may have no meaning in the function 1 mode.

7.6.3.35 Port Data Mirror Registers A-M (GPDMRA-M)

Address Offset: 61h-6Dh

Bit	R/W	Default	Description
7-0	R	-	**Port Data Mirror Register (GPDMRn[7:0])** Reading this register returns the pin level status. For group I/J, the return data may have no meaning in the function 1 mode.

7.6.3.36 Port Control n Registers (GPCRn, n = A0-M6)

These registers are used to control the functions of each I/O port pin. Each register is responsible for the settings of one pin in the port.

If Operation Mode is “Alternate Function”, Function 1 and/or Function 2/3 will be enabled. Refer to Table 7-8. GPIO Alternate Function on page 254 for the detail.

Address Offset: Refer to Table 7-8. GPIO Alternate Function

<table>
<tr><th>Bit</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7-6</td><td>R/W</td><td>Refer to Table 7-8 on page 254</td><td>Port Pin Mode (GPMD[1:0])
These bits are used to select the GPIO operation Mode.
<table>
<tr><th>GPMD[1:0]</th><th>Pin Status</th><th>READ GPDRn</th><th>WRITE GPDRn</th></tr>
<tr><td>00b</td><td>Alternate Function</td><td>Pin Status</td><td>GPDR is writable but it has no effects on the pin status.</td></tr>
<tr><td>01b</td><td>Output</td><td>Pin Status</td><td>The value written to GPDR is output to pin.</td></tr>
<tr><td>10b</td><td>Input</td><td>Pin Status</td><td>GPDR is writable but it has no effects on the pin status.</td></tr>
<tr><td>11b</td><td>Reserved</td><td>-</td><td>-</td></tr>
</table></td></tr>
<tr><td>5-3</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>2</td><td>R/W</td><td>Refer to Table 7-8 on page 254</td><td>Port Pin Pull Up (GPPU)
This bit is used to pull the port and always valid regardless of GPMD, input or output. Enable this bit will increase power consumption.
Note that if one port is operated in output mode, it should not enable this bit unless its output type is open-drain.

If both of GPPU and GPPD are set 1b, the corresponding port would be configured as tri-state.</td></tr>
<tr><td>1</td><td>R/W</td><td>Refer to Table 7-8 on page 254</td><td>Port Pin Pull Down (GPPD)
This bit is used to pull the port and always valid regardless of GPMD, input or output.

If both of GPPU and GPPD are set 1b, the corresponding port would be configured as tri-state.</td></tr>
<tr><td>0</td><td>R/W</td><td>0</td><td>Reserved</td></tr>
</table>

7.6.3.37 Output Type Registers A/B/C/D/E/F/G/H/I/J/M (GPOT A/B/C/D/E/F/G/H/I/J/M)

The Output Type register (GPOT) is an 8-bit register. These registers control the output type of GPIO. Each register contains one group which has eight ports at most. Note that these bits are valid only when corresponding GPMD equals to 01 (Output mode).

Other GPIO pin(s) can support open-drain by setting its(their) GPDR register(s) as 0 and switch GPMD field in GPCR register between input and output mode.

Address Offset: 71h, 72h, 73h, 74h, 75h, 76h, 77h, 78h, 79h, 7Ah, 7Dh,

Bit	R/W	Default	Description
7-0	R/W	00h	**Output Type Register (GPOTn[7:0])** The adjustable output types are only available on all port GPA0-A7, GPB0-B7, GPC0-C7, GPD0-D7, GPE0-E7, GPF0-F7 , GPG0-G7,GPH0-H6, GPI0-I7, GPJ0-J7 and GPM0-M6. For each bit: 0: Push-pull output 1: Open-drain output

7.6.4 Alternate Function Selection

The following lists function 1 and function 2 of each GPIO port. Notice that the GA20 function can be implemented by GPO or function 1 which is implemented at KBC module. Function 1 of GPB6 is KBRST# from KBC module through SWUC mode. It is recommended to input LPCRST# from GPD2 port.

Table 7-8. GPIO Alternate Function

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output Driving (mA)	Power	Pull Cap	Def Pull	5VT	1.8V Input	Def Mode
GPIOA	0	1610h	24	PWM0	GPCRA0[7:6]=00	WUI43	Always	-	-	8/16	VSTBY	Up/Dn	-	Y	-	GPI
	1	1611h	25	PWM1	GPCRA1[7:6]=00	WUI44	Always	-	-	8/16	VSTBY	Up/Dn	-	Y	-	GPI
	2	1612h	28	PWM2	GPCRA2[7:6]=00	WUI45	Always	-	-	8/16	VSTBY	Up/Dn	-	Y	-	GPI
	3	1613h	29	PWM3	GPCRA3[7:6]=00	WUI32	Always	-	-	8/16	VSTBY	Up/Dn	-	Y	-	GPI
	4	1614h	30	PWM4	GPCRA4[7:6]=00	WUI33	Always	SMCLK5	GPCRA4[7:6]=00 / PMER1[1]=1	8	VSTBY	Up/Dn	-	Y	Y	GPI
	5	1615h	31	PWM5	GPCRA5[7:6]=00	WUI34	Always	SMDAT5	GPCRA5[7:6]=00 / PMER1[1]=1	8	VSTBY	Up/Dn	-	Y	Y	GPI
	6	1616h	32	PWM6	GPCRA6[7:6]=00	WUI35	Always	SSCK	GPCRA6[7:6]=00 / SPICTRL>0	8	VSTBY	Up/Dn	-	Y	Y	GPI
	7	1617h	34	PWM7	GPCRA7[7:6]=00	WUI52	Always	RIG1#	GPCRA7[7:6]=00 / U2CTRL=3	8	VSTBY	Up/Dn	-	Y	Y	GPI
GPIOB	0	1618h	108	-	-	WUI53	Always	SIN0	GPCRB0[7:6]=00 / U1CTRL>0 / SIN0EN=1	8/16	VSTBY	Up/Dn	-	Y	-	GPI
	1	1619h	109	-	-	WUI54	Always	SOUT0	GPCRB1[7:6]=00 / U1CTRL>0 / SOUT0EN=1	8/16	VSTBY	Up/Dn	-	Y	-	GPI
	2	161Ah	123	-	-	WUI36	Always	TMA0	GPCRB2[7:6]=00 TMA0EN = 1	8	VSTBY	Up/Dn	-	-	-	GPI
	3	161Bh	110	SMCLK0	GPCRB3[7:6]=00	WUI55	Always	-	-	4	VSTBY	Up/Dn	-	Y	Y	Func1 1.8V in
	4	161Ch	111	SMDAT0	GPCRB4[7:6]=00	WUI46	Always	-	-	4	VSTBY	Up/Dn	-	Y	Y	Func1 1.8V in
	5	161Dh	126	GA20	GPCRB5[7:6]=00	WUI56	Always	-	-	2	VSTBY	Up/Dn	-	-	Y	GPI
	6	161Eh	4	KBRST#	GPCRB6[7:6]=00	WUI57	Always	-	-	2	VSTBY	Up/Dn	-	-	Y	GPI
	7	161Fh	112	RING# PWRFAIL#	GPCRB7[7:6]=00 GPCRB7[7:6]=00	WUI58	Always	CK32KOUT LPCRST#	GPCRB7[7:6]=00 / CK32OE=1 / LPCRSTEN=01	8/16	VSTBY	Up/Dn	-	Y	-	GPI

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output Driving (mA)	Power	Pull Cap	Def Pull	5VT	1.8V Input	Def Mode
GPIOC	0	1620h	119	-	-	WUI37	Always	-	-	2	VSTBY	Up/Dn	-	Y	Y	GPI
	1	1621h	115	SMCLK1	GPCRC1[7:6]=00	WUI59	Always	-	-	4	VSTBY	Up/Dn	-	Y	Y	GPI
	2	1622h	116	SMDAT1	GPCRC2[7:6]=00	WUI47	Always	-	-	4	VSTBY	Up/Dn	-	Y	Y	GPI
	3	1623h	56	KSO16	GPCRC3[7:6]=00	WUI60	Always	SMOSI	GPCRC3[7:6]=00 / SPICTRL>0	8	VSTBY	Up/Dn	-	-	-	GPI
	4	1624h	120	-	-	WUI2	Always	-	-	2	VSTBY	Up/Dn	-	-	Y	GPI
	5	1625h	57	KSO17	GPCRC5[7:6]=00	WUI61	Always	SMISO	GPCRC5[7:6]=00 / SPICTRL>0	8	VSTBY	Up/Dn	-	-	-	GPI
	6	1626h	124	-	-	WUI3	Always	-	-	2	VSTBY	Up/Dn	-	-	Y	GPI
	7	1627h	16	PWUREQ#	GPCRC7[7:6]=00	WUI38	Always	BBO SMCLK2ALT	GPCRC7[7:6]=00 / HWBPE[2:1]>0 GPCRC7[7:6]=00 / SMCLK2PS=1	8/16	VSTBY	Up/Dn	-	-	Y	GPI
GPIOD	0	1628h	18	RI1#	GPCRD0[7:6]=00	WUI0	Always	-	-	4	VSTBY	Up/Dn	-	-	Y	GPI
	1	1629h	21	RI2#	GPCRD1[7:6]=00	WUI1	Always	-	-	4	VSTBY	Up/Dn	-	Y	Y	GPI
	2	162Ah	22	LPCRST#	LPCRSTEN=10	WUI4	Always	-	-	8	VSTBY	Up/Dn	-	Y	Y	Func1
	3	162Bh	23	ECSCI#	GPCRD3[7:6]=00	WUI62	Always	-	-	8	VSTBY	Up/Dn	-	Y	Y	GPI
	4	162Ch	15	ECSMI#	GPCRD4[7:6]=00	WUI63	Always	-	-	8	VSTBY	Up/Dn	-	-	Y	GPI
	5	162Dh	33	GINT	GPCRD5[7:6]=00	WUI64	Always	CTS0#	GPCRD5[7:6]=00 / U1CTRL>1	8	VSTBY	Up/Dn	-	Y	Y	GPI
	6	162Eh	47	TACH0A	GPCRD6[7:6]=00	WUI65	Always	-	-	2	VSTBY	Up/Dn	-	-	Y	GPI
	7	162Fh	48	TACH1A	GPCRD7[7:6]=00	WUI39	Always	-	-	2	VSTBY	Up/Dn	-	-	Y	GPI
GPIOE	0	1630h	19	L80HLAT	GPCRE0[7:6]=00	WUI24	Always	BAO SMCLK4	GPCRE0[7:6]=00 / HWBPE[0]=1 GPCRE0[7:6]=00 / PMER1[1]=1	8/16	VSTBY	Up/Dn	-	Y	Y	GPI
	1	1631h	82	-	-	WUI25	Always	-	-	8	VSTBY	Up/Dn	-	Y	Y	GPI
	2	1632h	83	-	-	WUI26	Always	-	-	8	VSTBY	Up/Dn	-	Y	Y	GPI
	3	1633h	84	-	-	WUI27	Always	-	-	8/16	VSTBY	Up/Dn	-	Y	-	GPI
	4	1634h	125	PWRSW	GPCRE4[7:6]=00	WUI66	Always	-	-	2	VSTBY	Up/Dn	-		Y	GPI
	5	1635h	35	-	-	WUI5	Always	RTS1#	GPCRE5[7:6]=00 / U2CTRL>1	2	VSTBY	Up/Dn	-	Y	Y	GPI
	6	1636h	17	LPCPD#	GPCRE6[7:6]=00	WUI6	Always	-	-	2	VSTBY	Up/Dn	-	Y	Y	GPI
	7	1637h	20	L80LLAT	GPCRE7[7:6]=00	WUI7	Always	SMDAT4	GPCRE7[7:6]=00 / PMER1[0]=1	8/16	VSTBY	Up/Dn	-	Y	Y	GPI

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output Driving (mA)	Power	Pull Cap	Def Pull	5VT	1.8V Input	Def Mode
GPIOF	0	1638h	85	-	-	WUI48	Always	CEC	GPCRF0[7:6]=00 CECEN = 1	8	VSTBY	Up/Dn	-	Y	Y	GPI
	1	1639h	86	-	-	WUI49	Always	-	-	8	VSTBY	Up/Dn	-	Y	Y	GPI
	2	163Ah	87	-	-	WUI50	Always	DTR0# SMCLK3	GPCRF2[7:6]=00 / U1CTRL>1 GPCRF2[7:6]=00 / SMB3E=1 / SMB3PSEL=1	8	VSTBY	Up/Dn	-	Y	Y	GPI
	3	163Bh	88	-	-	WUI51	Always	RTS0# SMDAT3	GPCRF3[7:6]=00 / U1CTRL>1 GPCRF3[7:6]=00 / SMB3E=1 / SMB3PSEL=1	8	VSTBY	Up/Dn	-	Y	Y	GPI
	4	163Ch	89	PD1CC1	GPCRF4[7:6]=10 GPCRF4[2:1]=11	WUI20	Always	-	-	8	VSTBY	Up/Dn	Dn, See note 3	Y	Y	GPI
	5	163Dh	90	PD1CC2	GPCRF5[7:6]=10 GPCRF5[2:1]=11	WUI21	Always	-	-	8	VSTBY	Up/Dn	Dn, See note 3	Y	Y	GPI
	6	163Eh	117	SMCLK2	GPCRF6[7:6]=00 / SMCLK2PS=0	WUI22	Always	PECI	GPCRF6[7:6]=00 / PECIE=1	4	VSTBY	Up/Dn	-	-	Y	GPI
	7	163Fh	118	SMDAT2	GPCRF7[7:6]=00	WUI23	Always	PECIRQT#	GPCRF7[7:6]=00 / PECIE=1 / SMCLK2PS=0	4	VSTBY	Up/Dn	-	-	Y	GPI
GPIOG	0	1640h	106	-	-	WUI67	Always	SSCE1#	GPCRG0[7:6]=00 / SPICTRL[0]>0	8	VSTBY	Up/Dn		Y	Y	GPO,H
	1	1641h	107	-	-	WUI68	Always	DTR1#	GPCRG1[7:6]=00 / U2CTRL>1	8/16	VSTBY	Up/Dn	Dn	Y	Y	GPO,L /ID7
	2	1642h	100	-	-	WUI69	Always	SSCE0#	GPCRG2[7:6]=00 / SPICTRL[0]>0	4	VSTBY	Up/Dn	-	Y	Y	GPI
	3	1643h	101	FSCE#	GPCRG3[7:6]=00 or SIFE=1	-	-	-	-	8 (output only)	VFSPI	-	-	Y	-	GPI Don't pull up this.
	4	1644h	102	FMOSI	GPCRG4[7:6]=00 or SIFE=1	-	-	-	-	8 (output only)	VFSPI	-	-	Y	-	GPI Don't pull up this.
	5	1645h	103	FMISO	GPCRG5[7:6]=00 or SIFE=1	-	-	-	-	(input only)	VFSPI	-	-	Y	-	GPI Don't pull up this.

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output Driving (mA)	Power	Pull Cap	Def Pull	5VT	1.8V Input	Def Mode
	6	1646h	104	-	-	WUI70	Always	DSR0#	GPCRG6[7:6]=00 / U1CTRL>1	4	VSTBY	Up/Dn	-	Y	Y	GPI Must be pulled up this.
	7	1647h	105	FSCK	GPCRG7[7:6]=00 or SIFE=1	-	-	-	-	8 (output only)	VFSPI	-	-	Y	-	GPI Don't pull up this.
GPIOH	0	1648h	93	CLKRUN#	GPCRH0[7:6]=00	WUI16	Always	-	-	8	VSTBY	Up/Dn	-	Y	Y	GPI/ID0
	1	1649h	94	PD2CC1	GPCRH1[7:6]=10 GPCRH1[2:1]=11	WUI17	Always	SIN1 SMCLK3	GPCRH1[7:6]=00 / U2CTRL>0 / SIN1EN=1 / UART1PSEL=0 GPCRH1[7:6]=00 / SMB3E=1 / SMB3PSEL=0	8	VSTBY	Up/Dn	Dn, See note 3	Y	Y	GPI/ID1
	2	164Ah	95	PD2CC2	GPCRH2[7:6]=00 GPCRH2[2:1]=11	WUI18	Always	SOUT1 SMDAT3	GPCRH2[7:6]=00 / U2CTRL>0 / SOUT1EN=1 / UART1PSEL=0 GPCRH2[7:6]=00 / SMB3E=1 / SMB3PSEL=0	8	VSTBY	Up/Dn	Dn, See note 3	Y	Y	GPI/ID2
	3	164Bh	96	-	-	WUI19	Always	-	-	8/16	VSTBY	Up/Dn	-	Y	-	GPI/ID3
	4	164Ch	97	-	-	WUI40	Always	-	-	8/16	VSTBY	Up/Dn	-	Y	-	GPI/ID4
	5	164Dh	98	-	-	WUI41	Always	SIN1	GPCRH1[7:6]=00 / U2CTRL>0 / SIN1EN=1 / UART1PSEL=1	8	VSTBY	Up/Dn	Dn	Y	Y	GPI/ID5
	6	164Eh	99	-	-	WUI42	Always	SOUT1	GPCRH2[7:6]=00 / U2CTRL>0 / SOUT1EN=1 / UART1PSEL=1	8	VSTBY	Up/Dn	Dn	Y	Y	GPI/ID6

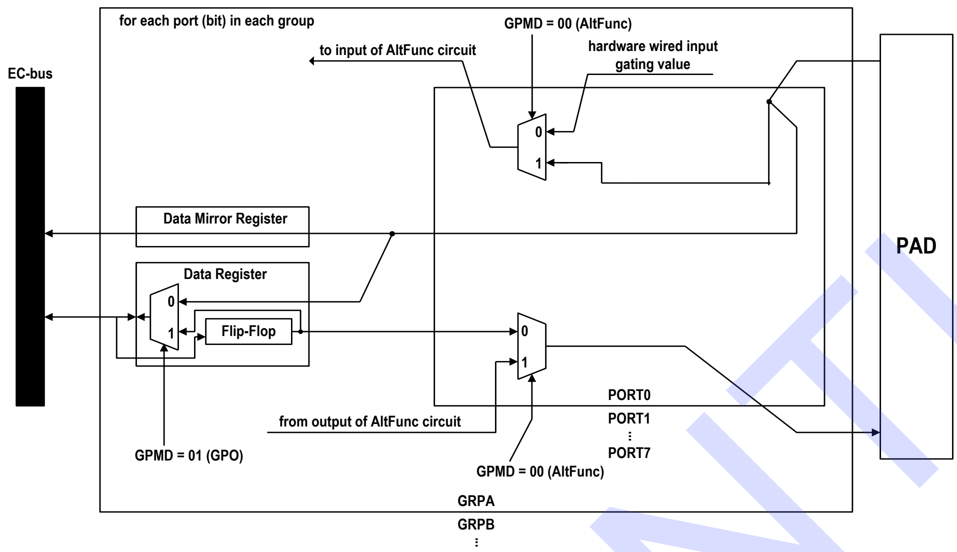
Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output Driving (mA)	Power	Pull Cap	Def Pull	5VT	1.8V Input	Def Mode
GPIOI	0	1650h	66	ADC0	GPCRI0[7:6]=00	WUI71	GPCRI0[7:6]=10	-	-	2	VSTBY / AVCC	-	-	-	Y	GPI
	1	1651h	67	ADC1	GPCRI1[7:6]=00	WUI72	GPCRI1[7:6]=10	-	-	2	VSTBY / AVCC	-	-	-	Y	GPI
	2	1652h	68	ADC2	GPCRI2[7:6]=00	WUI73	GPCRI2[7:6]=10	-	-	2	VSTBY / AVCC	-	-	-	Y	GPI
	3	1653h	69	ADC3	GPCRI3[7:6]=00	WUI74	GPCRI3[7:6]=10	-	-	2	VSTBY / AVCC	-	-	-	Y	GPI
	4	1654h	70	ADC4	GPCRI4[7:6]=00	WUI28	GPCRI4[7:6]=10	-	-	2	VSTBY / AVCC	-	-	-	Y	GPI
	5	1655h	71	ADC5	GPCRI5[7:6]=00	WUI29	GPCRI5[7:6]=10	DCD1#	GPCRI5[7:6]=00 / U2CTRL>1	2	VSTBY / AVCC	-	-	-	Y	GPI
	6	1656h	72	ADC6	GPCRI6[7:6]=00	WUI30	GPCRI6[7:6]=10	DSR1#	GPCRI6[7:6]=00 / U2CTRL>1	2	VSTBY / AVCC	-	-	-	Y	GPI
	7	1657h	73	ADC7	GPCRI7[7:6]=00	WUI31	GPCRI7[7:6]=10	CTS1#	GPCRI7[7:6]=00 / U2CTRL>1	2	VSTBY / AVCC	-	-	-	Y	GPI
GPIOJ	0	1658h	76	-	-	WUI80	Always	TACH2	GPCRJ0[7:6]=00 / T0BEN=1	4	VSTBY	Up/Dn	-	-	Y	GPI
	1	1659h	77	-	-	WUI81	Always	-	-	4	VSTBY	Up/Dn	-	-	Y	GPI
	2	165Ah	78	-	-	WUI82	GPCRJ2[7:6]=10	TACH0B	GPCRJ2[7:6]=00 / T0BEN=1	4	VSTBY	Up/Dn	-	-	Y	GPI
	3	165Bh	79	-	-	WUI83	GPCRJ3[7:6]=10	TACH1B	GPCRJ3[7:6]==00 / T1BEN=1	4	VSTBY	Up/Dn	-	-	Y	GPI
	4	165Ch	80	-	-	WUI84	GPCRJ4[7:6]=10	DCD0#	GPCRJ4[7:6]=00 / U1CTRL>1	4	VSTBY	Up/Dn	-	-	Y	GPI
	5	165Dh	81	-	-	WUI85	GPCRJ5[7:6]=10	RIG0#	GPCRJ5[7:6]=00 / U1CTRL=3	4	VSTBY	Up/Dn	-	-	Y	GPI
	6	165Eh	128	-	-	WUI86	Always	-	-	2	VSTBY	-	-	-	Y	GPI
	7	165Fh	2	-	-	WUI87	Always	-	-	2	VSTBY	-	-	-	Y	GPI
GPIOM	0	16A0h	10	LAD0	GPCRM0[7:6]=00	WUI96	Always	-	-	8	VCC	Up/Dn	-	-	Y	Func1
	1	16A1h	9	LAD1	GPCRM1[7:6]=00	WUI97	Always	-	-	8	VCC	Up/Dn	-	-	Y	Func1
	2	16A2h	8	LAD2	GPCRM2[7:6]=00	WUI98	Always	-	-	8	VCC	Up/Dn	-	-	Y	Func1
	3	16A3h	7	LAD3	GPCRM3[7:6]=00	WUI99	Always	-	-	8	VCC	Up/Dn	-	-	Y	Func1
	4	16A4h	13	LPCCLK	GPCRM4[7:6]=00	WUI100	Always	-	-	2	VCC	Up/Dn	-	-	Y	Func1
	5	16A5h	6	LFRAME#	GPCRM5[7:6]=00	WUI101	Always	-	-	2	VCC	Up/Dn	-	-	Y	Func1
	6	16A6h	5	SERIRQ	GPCRM6[7:6]=00	WUI102	Always	-	-	8	VCC	Up/Dn	-	-	Y	Func1

Note: Since all GPIOs belong to the VSTBY power plane, there are some special considerations below:
(1) If it is output to external VCC derived power plane circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power plane circuit, this external circuit must consider not floating the GPIO input.
(3) For pins with the CC function, the default is with the 5.1k pull-down resistor. It needs to be disabled when these pins are for the GPIO use.

Table 7-9. GPIO with Some Other Function

Pin	Description	Note
GPC7(=BBO)	Hardware bypass: one of the following: GPI6 bypass to GPC7. GPI7 bypass to GPC7.	Refer to Section 7.6.3.5 General Control 4 Register (GCR4), page 236.
GPE0(=BAO)	Hardware bypass: GPI6 bypass to GPE0.	
GPE4	A timeout reset event will be asserted to reset EC after GPE4 has been pulled low for more than 10 seconds. This reset will be output to GPI5 as well.	Refer to Section 7.6.3.10 General Control 9 Register (GCR9), page 239.
In: GPH4, GPI2, GPI3 Out: The same as above GPB5-7, GPH0-6	Power Good Watch: Basically, it's an extension of above.	Refer to Section 7.6.3.6 General Control 5 Register (GCR5) , page 237. Refer to Section 7.6.3.7 General Control 6 Register (GCR6) , page 237 .
In: GPE0, GPI2, GPI3 Out: The same as above	Power Good Watch: It's alternative input of above.	Refer to Section 7.6.3.6 General Control 5 Register (GCR5) , page 237. Refer to Section 7.6.3.7 General Control 6 Register (GCR6) , page 237 .
GPD0 GPD1 GPC4 GPC6 GPE5 GPE4	Input Debounce circuit Debounce WUI inputs from WUI0, WUI1 ,WUI2 ,WUI3 ,WUI5 and PWRSW.	Refer to Section 7.6.3.15 General Control 14 Register (GCR14) , page 241. Refer to Section 7.6.3.18 General Control 16 Register (GCR16), page 243. Refer to Section 7.6.3.19 General Control 17 Register (GCR17), page 243. Refer to Section 7.6.3.20 General Control 18 Register (GCR18), page 244.

Figure 7-7. GPIO Simplified Diagram



7.6.5 Programming Guide

The firmware should modify LPCRSTEN when it boots up if necessary.

7.7 EC Clock and Power Management Controller (ECPM)

7.7.1 Overview

The EC Clock and Power Management module provide the EC clock control and power management.

7.7.2 Features

- Supports programmable EC clock frequency
- Supported by module power-down mode control
- Supports PLL power-down when CPU enters a Sleep mode

7.7.3 EC Interface Registers

The clock generation and power management registers are listed below. The base address is 1E00h.

Table 7-10. EC View Register Map, ECPM

7 0	Offset
Reserved	00h
Clock Gating Control 1 Register (CGCTRL1R)	01h
Clock Gating Control 2 Register (CGCTRL2R)	02h
Clock Gating Control 3 Register (CGCTRL3R)	05h
PLL Control (PLLCTRL)	03h
Auto Clock Gating (AUTOCG)	04h
PLL Frequency (PLLFREQR)	06h
Reserved	07h
PLL Clock Source Status (PLLCSS)	08h
Clock Gating Control 4 Register (CGCTRL4R)	09h
Clock Gating Control 5 Register (CGCTRL5R)	13h
Clock Gating Control 6 Register (CGCTRL6R)	15h
System Clock Divide Control Register 0 (SCDCR0)	0Ch
System Clock Divide Control Register 1 (SCDCR1)	0Dh
System Clock Divide Control Register 2 (SCDCR2)	0Eh
System Clock Divide Control Register 3 (SCDCR3)	0Fh
System Clock Divide Control Register 4 (SCDCR4)	10h

7.7.3.1 Clock Gating Control 1 Register (CGCTRL1R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

7.7.3.2 Clock Gating Control 2 Register (CGCTRL2R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 02h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**

Bit	R/W	Default	Description
4	R/W	0b	**SWUC Clock Gating (SWUCCG)** 0: Operation 1: Clock to this module is gated
3-0	-	-	**Reserved**

7.7.3.3 Clock Gating Control 3 Register (CGCTRL3R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 05h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	W	1b	**Reserved** Always write 1 to this bit.
5-4	-	-	**Reserved**
3	R/W	0b	**PECI Clock Gating (PECICG)** 0: Operation 1: Clocks to PECI module is gated.
2	R/W	0b	**UART Clock Gating (UART12CG)** 0: Operation 1: Clocks to UART1/UART2 modules are gated.
1	R/W	0b	**SSPI Clock Gating (SSPICG)** 0: Operation 1: Clock to this module is gated.
0	R/W	1b	**DBGR Clock Gating (DBGRCG)** 0: Operation 1: Clock to this module is gated.

7.7.3.4 PLL Control (PLLCTRL)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 03h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	0b	**Deep Doze Mode Control (DDMC)** 0: PLL will be disabled 1: PLL will not be disabled (Deep Doze Mode)
0	R/W	1b	**PLL Power Down Control (PPDC)** 0: PLL will not be powered down by software until VSTBY is not supplied. Excuting STANDBY instruction will enter the EC Doze mode. 1: PLL will be powered down after excuting STANDBY instruction and entering an EC power-down mode.

7.7.3.5 Auto Clock Gating (AUTOCG)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 04h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	1b	**Auto UART1 Clock Gating (AUART1CG)** 1: The UART1 clock will be automatically gated if the corresponding port of GPIO is not in its alternative function. It also overrides UART12CG bit in CGCTRL3R register. If UART1SD bit in RSTDMMC register is 1, the clock will also be gated if the chip is in the Doze/Deep Doze/Sleep mode. If UART1SD bit in RSTDMMC register is 0, the clock will also be gated if VCC is off. 0: The UART1 clock is gated by UART12CG bit in CGCTRL3R register.
5	R/W	1b	**Auto UART2 Clock Gating (AUART2CG)** 1: The UART2 clock will be automatically gated if the corresponding port of GPIO is not in its alternative function. It also overrides UART12CG bit in CGCTRL3R register. If UART2SD bit in RSTDMMC register is 1, the clock will also be gated if the chip is in the Doze/Deep Doze/Sleep mode. If UART2SD bit in RSTDMMC register is 0, the clock will also be gated if VCC is off. 0: The UART2 clock is gated by UART12CG bit in CGCTRL3R register.
4	R/W	1	**Auto SSPI Clock Gating (ASSPICG)** 1: The SSPI clock will be automatically gated if the corresponding port of GPIO is not in its alternative function. It also overrides SSPICG bit in CGCTRL3R register. If SSPISD bit in RSTDMMC register is 1, the clock will also be gated if the chip is in the Doze/Deep Doze/Sleep mode. If SSPISD bit in RSTDMMC register is 0, the clock will also be gated if VCC is off. 0: The SSPI clock is gated by SSPICG bit in CGCTRL3R register.
3-0	-	-	**Reserved**

7.7.3.6 PLL Frequency (PLLFREQR)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 06h

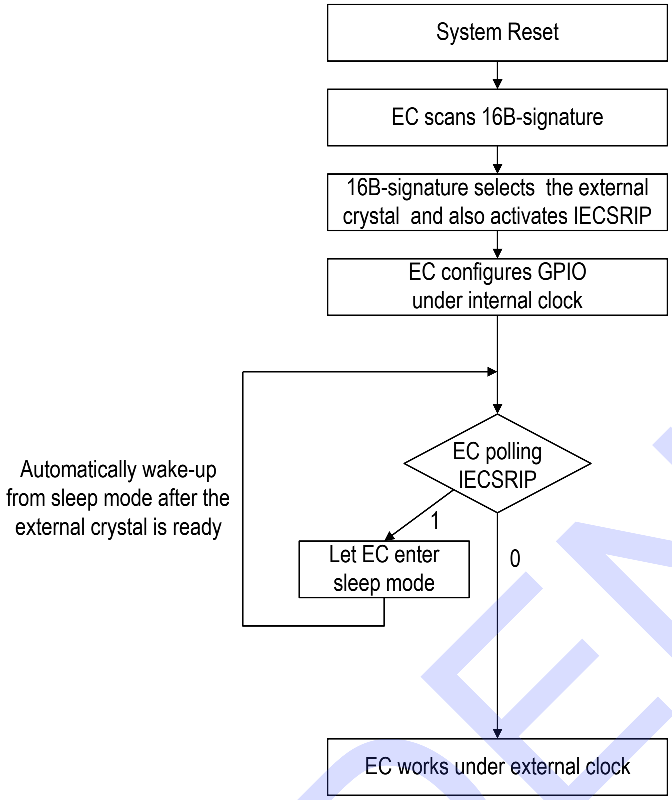
Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0100b	**PLL Frequency (PLLFREQ)** 0000b: Select 8MHz as PLL frequency. 0001b: Select 16MHz as PLL frequency. 0010b: Select 24MHz as PLL frequency. 0011b: Select 32MHz as PLL frequency. 0100b: Select 48MHz as PLL frequency. (Default) 0101b: Select 64MHz as PLL frequency. 0110b: Select 72MHz as PLL frequency. 0111b: Select 96MHz as PLL frequency. Otherwise: Reserved Read returns the current PLL frequency setting. Writing data to this register doesn't change the PLL frequency immediately, which will be changed when the status is changed into wakeup from the Sleep mode. SCEMINHW field in FLHCTRL2R register may be required before the PLL frequency is changed.

7.7.3.7 PLL Clock Source Status (PLLCSS)

Address Offset: 08h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R	0b	**Internal-to-External Clock Switching Request Is Postponing (IECSRIP)** The EC scan the 16B-signature by the internal clock and switch to the external clock if 8th byte's bit 4 in 16B-signature is 0b; however, the switching time-point can be postponed by setting 8th byte's bit 6 in 16B-signature to 1 until Sleep mode. It's userful to toggle GPIO in early time. 0b: Otherwise. 1b: Internal-to-external clock switching is postponing. Let EC enter Sleep mode to finish this clock switching request. Refer to Figure 7-8. Program Flow Chart of IECSRIP. Refer to section 6.4.3.12.1 16B-signature and Implicit/Explicit EC Code Base Address on page 116.

Figure 7-8. Program Flow Chart of IECSRIP



7.7.3.8 Clock Gating Control 4 Register (CGCTRL4R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 09h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**SMB Bus CHC Clock Gating (SMBBCCG)** 0: Operation 1: Clock to this channel is gated.
3	R/W	0b	**SMB Bus CHB Clock Gating (SMBBBCG)** 0: Operation 1: Clock to this channel is gated.
2	R/W	0b	**SMB Bus CHA Clock Gating (SMBBACG)** 0: Operation 1: Clock to this channel is gated.
1	R/W	0b	**SMB Bus Clock Gating (SMBBCG)** 0: Operation 1: Clock to this module is gated.
0	-	-	**Reserved**

7.7.3.9 Clock Gating Control 5 Register (CGCTRL5R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 13h

Bit	R/W	Default	Description
7	-	-	Reserved
6	R/W	0b	**PD2 Clock Gating (PD2CG)** 0: Operation 1: Clocks to this module is gated.
5	-	-	**Reserved**
4	-	-	Reserved
3	R/W	0b	**SPI Slave Clock Gating (SPISLVCG)** 0: Operation 1: Clocks to this module is gated.
2	-	-	Reserved
1	R/W	0b	**PD1 Clock Gating (PD1CG)** 0: Operation 1: Clock to this module is gated.
0	R/W	0b	**PD0 Clock Gating (PD0CG)** 0: Operation 1: Clock to this module is gated.

7.7.3.10 Clock Gating Control 6 Register (CGCTRL6R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 15h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**RISCV JTAG Debug Clock Gating (RISCVDEBUGCG)** 0: Operation 1: Clocks to this module is gated.
2	R/W	0b	**RISCV FPU Clock Gating (RISCVFPUCG)** 0: Operation 1: Clocks to this module is gated.
1-0	-	-	**Reserved**

7.7.3.11 System Clock Divide Control Register 0 (SCDCR0)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	010b	**Fnd(SPI) Clock Frequency Select (CLK_FND_DIV_SEL)** 000: PLL clock Frequency / 1. 001: PLL clock Frequency / 2. 010: PLL clock Frequency / 3. 011: PLL clock Frequency / 4. 100: PLL clock Frequency / 5. 101: PLL clock Frequency / 6. else: Reserved
3	-	-	**Reserved**
2-0	R/W	000b	**MCU Clock Frequency Select (CLK_CPU_DIV_SEL)** 000: PLL clock Frequency / 1. 001: PLL clock Frequency / 2. 010: PLL clock Frequency / 3. 011: PLL clock Frequency / 4. 100: PLL clock Frequency / 5. 101: PLL clock Frequency / 6. 110: Internal 2M Hz clock. 111: 32k Hz clock.

7.7.3.12 System Clock Divide Control Register 1 (SCDCR1)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	1b	**UART Clock Frequency Select (CLK_UART_DIV_SEL)** 0000: PLL clock Frequency / 1. 0001: PLL clock Frequency / 2. 0010: PLL clock Frequency / 3. 0011: PLL clock Frequency / 4. 0100: PLL clock Frequency / 5. 0101: PLL clock Frequency / 6. 0110: PLL clock Frequency / 7. 0111: PLL clock Frequency / 8. 1000: PLL clock Frequency / 9. 1001: PLL clock Frequency / 10. 1010: PLL clock Frequency / 11. 1011: PLL clock Frequency / 12. 1100: PLL clock Frequency / 13. 1101: PLL clock Frequency / 14. 1110: PLL clock Frequency / 15. 1111: PLL clock Frequency / 16.

7.7.3.13 System Clock Divide Control Register 2 (SCDCR2)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 0Eh

Bit	R/W	Default	Description
7-4	R/W	1b	**SSPI Clock Frequency Select (CLK_SSPI_DIV_SEL)** 0000: PLL clock Frequency / 1. 0001: PLL clock Frequency / 2. 0010: PLL clock Frequency / 3. 0011: PLL clock Frequency / 4. 0100: PLL clock Frequency / 5. 0101: PLL clock Frequency / 6. 0110: PLL clock Frequency / 7. 0111: PLL clock Frequency / 8. 1000: PLL clock Frequency / 9. 1001: PLL clock Frequency / 10. 1010: PLL clock Frequency / 11. 1011: PLL clock Frequency / 12. 1100: PLL clock Frequency / 13. 1101: PLL clock Frequency / 14. 1110: PLL clock Frequency / 15. 1111: PLL clock Frequency / 16
3-0	R/W	1b	**SMB Clock Frequency Select (CLK_SMB_DIV_SEL)** 0000: PLL clock Frequency / 1. 0001: PLL clock Frequency / 2. 0010: PLL clock Frequency / 3. 0011: PLL clock Frequency / 4. 0100: PLL clock Frequency / 5. 0101: PLL clock Frequency / 6. 0110: PLL clock Frequency / 7. 0111: PLL clock Frequency / 8. 1000: PLL clock Frequency / 9. 1001: PLL clock Frequency / 10. 1010: PLL clock Frequency / 11. 1011: PLL clock Frequency / 12. 1100: PLL clock Frequency / 13. 1101: PLL clock Frequency / 14. 1110: PLL clock Frequency / 15. 1111: PLL clock Frequency / 16.

7.7.3.14 System Clock Divide Control Register 3 (SCDCR3)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 0Fh

Bit	R/W	Default	Description
7-4	R/W	1b	**JTAG Clock Frequency Select (CLK_JTAG_DIV_SEL)** 0000: PLL clock Frequency / 1. 0001: PLL clock Frequency / 2. 0010: PLL clock Frequency / 3. 0011: PLL clock Frequency / 4. 0100: PLL clock Frequency / 5. 0101: PLL clock Frequency / 6. 0110: PLL clock Frequency / 7. 0111: PLL clock Frequency / 8. 1000: PLL clock Frequency / 9. 1001: PLL clock Frequency / 10. 1010: PLL clock Frequency / 11. 1011: PLL clock Frequency / 12. 1100: PLL clock Frequency / 13. 1101: PLL clock Frequency / 14. 1110: PLL clock Frequency / 15. 1111: PLL clock Frequency / 16
3-0	R/W	001b	**EC Clock Frequency Select (CLK_EC_DIV_SEL)** x000: Fnd clock Frequency / 1. x001: Fnd clock Frequency / 2. x010: Fnd clock Frequency / 3. x011: Fnd clock Frequency / 3.5. x100: Fnd clock Frequency / 4. x101: Fnd clock Frequency / 5. x110: Fnd clock Frequency / 6. x111: Fnd clock Frequency / 7. Writing data to CLK_EC_DIV_SEL bits doesn't change the EC Clock frequency immediately, which will be changed when the status is changed into wakeup from the Sleep mode.

7.7.3.15 System Clock Divide Control Register 4 (SCDCR4)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 10h

Bit	R/W	Default	Description
7-4	R/W	0101b	**USBPD Clock Frequency Select (CLK_USBPD_DIV_SEL)** 0000: PLL clock Frequency / 1. 0001: PLL clock Frequency / 2. 0010: PLL clock Frequency / 3. 0011: PLL clock Frequency / 4. 0100: PLL clock Frequency / 5. 0101: PLL clock Frequency / 6. 0110: PLL clock Frequency / 7. 0111: PLL clock Frequency / 8. 1000: PLL clock Frequency / 9. 1001: PLL clock Frequency / 10. 1010: PLL clock Frequency / 11. 1011: PLL clock Frequency / 12. 1100: PLL clock Frequency / 13. 1101: PLL clock Frequency / 14. 1110: PLL clock Frequency / 15. 1111: PLL clock Frequency / 16
3-0	R/W	0h	**PWM Clock Frequency Select (CLK_PWM_DIV_SEL)** 0000: PLL clock Frequency / 1. 0001: PLL clock Frequency / 2. 0010: PLL clock Frequency / 3. 0011: PLL clock Frequency / 4. 0100: PLL clock Frequency / 5. 0101: PLL clock Frequency / 6. 0110: PLL clock Frequency / 7. 0111: PLL clock Frequency / 8. 1000: PLL clock Frequency / 9. 1001: PLL clock Frequency / 10. 1010: PLL clock Frequency / 11. 1011: PLL clock Frequency / 12. 1100: PLL clock Frequency / 13. 1101: PLL clock Frequency / 14. 1110: PLL clock Frequency / 15. 1111: PLL clock Frequency / 16

7.8 SMBus Interface (SMB)

7.8.1 Overview

The SMBus/I2C interface includes six SMBus channels. The module can maintain bi-directional communication with the external devices through the interface SMCLK0/SMDAT0, SMCLK1/SMDAT1, SMCLK2/SMDAT2, SMCLK3/SMDAT3, SMCLK4/SMDAT4 and SMCLK5/SMDAT5 pins. It is compatible with ACCESS BUS and I2C BUS.

7.8.2 Features

- Supports SMBus 2.0
- Supports four SMBus channels
- Performs SMBus messages with packet error checking (PEC) either enabled or disabled
- Compatible with I2C cycles
- SMBus master also supports two 32-byte FIFOs for read/write (FIFO Mode). Besides, master FIFO supports threshold function as well.
- Two SMBus slaves on channel A and B. Slave channel A also supports 16-byte FIFO for read/write (FIFO Mode). Besides, slave FIFO supports threshold function as well.
- Two user-defined Slave addresses for each slave
- Supports pre-defined command (dedicated pre-defined slave address) for Slave channel A
- Supports Bridge function; SMBus interface can bridge signal from Slave A to Master C
- Independently select SMCLK frequency for each channel

7.8.3 Functional Description

The SMBus Channel A contains one SMBus master and one SMBus slave.
The SMBus Channel B contains one SMBus master and one SMBus slave.
The SMBus Channel C contains one SMBus master.
The SMBus Channel D,E,F contain 4, 4, 1 masters and one slave.

The default interface of the SMBus slave in Channel A is located at SMCLK0/SMDAT0. The default interface of the SMBus slave in Channel B is located at SMCLK1/SMDAT1. The interface of the SMBus slave can be switched to SMCLK1/SMDAT1 or SMCLK2/SMDAT2 or SMCLK3/SMDAT3 or SMCLK4/SMDAT4 or SMCLK5/SMDAT5.

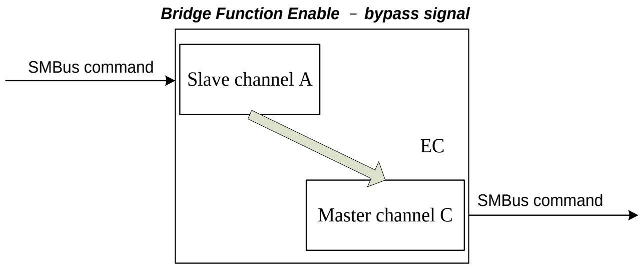
The master supports seven command protocols of the SMBus (see System Management Bus Specification): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, and Block Read/Write. The master also supports the I2C-compatible cycles (see The I2C-Bus Specification). Furthermore, SMBus master supports 32 Byte FIFO for following commands, Block Write (FIFO Mode), Block Read (FIFO Mode), I2C-compatible Write (FIFO Mode), I2C-compatible Read (FIFO Mode) and I2C Write to Read (FIFO Mode). For Crystal-Free case, SMBus master hardware will continue to complete the transmission of FIFO data to the slave device after EC enters the sleep mode. Master FIFO also supports threshold function. Threshold function lets software process part of FIFO data before FIFO becomes empty and it can improve the transmission performance of the bus.

The slave supports three types of messages: Byte Write, Byte Read, and Host Notify.

Slave channel A also supports pre-defined command. It supports protocol such as I2EC Read/Write, Flash Read and Follow mode command for each SPI instruction.

SMBus interface also supports bridge function. Whether function is enabled or not is controlled by writing 1 to SBF bit of SLVISELR register. Then write 1 to SMHEN bit of HOCTL2_C to enable Master channel C and write 1 to SLVEN bit of HOCTL2_A to enable slave channel A. Besides, set SCLKS of SCLKTS_C to select the SMCLK rate for channel C. Bridge function will bypass slave channel A signal to Master channel C. The data in the bridge mode will be bridged by byte if it is the slave address; otherwise it will be bridged by bit.

Figure 7-9. Diagram of SMBus Bridge Bypass Function



7.8.3.1 SMBus Master Interface

When an interrupt to INTC (INT9, INT10, and INT16 for channel A, B, and C respectively) is detected, software can read the Host Status Register to know the interrupt source. There are 5 interrupt conditions: Byte Done, Failed, Bus Error, Device Error, and Finish.

Quick Command:
In the Quick Command, the Transmit Slave Address Register is sent. Software should force the PEC_EN bit in Host Control Register and I2C_EN bit in Host Control 2 Register to 0 when this command is run.

Send Byte/ Receive Byte:
In the Send Byte command, the Transmit Slave Address and Host Command Registers are sent.
In the Receive Byte command, the Transmit Slave Address Register is sent. The received data is stored in the Host DATA 0 register. Software must force the I2C_EN bit in Host control 2 Register to 0 when this command is run.

Write Byte/ Write Word
In the Write Byte command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Registers are sent.
In the Write Word command, the Transmit Slave Address Register, Host Command Register, Host Data 0, and Host Data 1 Registers are sent.
In these commands, software must force the I2C_EN bit in Host Control 2 Register to 0.

Read Byte/ Read Word
In the Read Byte command, the Transmit Slave Address Register and Host Command Register are sent. Data is received into the Host Data 0 Register.
In the Read Word command, the Transmit Slave Address Register and Host Command Register are sent. The returned 2 bytes of data are received into the Host Data 0 Register and Host Data 1 Register.
In these commands, software must force the I2C_EN bit in Host Control 2 Register to 0.

Process Call
In the Process Call command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data1 registers are sent. The returned 2 bytes of data are received into the Host Data 0 Register and Host Data 1 Register. When the I2C_EN bit in Host Control 2 Register is set to 1, the Host Command Register will not be sent.
Note: The Process Call command with I2C_EN bit set and the PEC_EN bit set produce undefined results.

Block Write/ Block Read
In the Block Write command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 (byte count) register are sent. Data is then sent from the Host Block Data Byte register.
In the Block Read commands, the Transmit Slave Address Register, and Host Command Register are sent. The first byte (byte count) received is stored in the Host Data 0 register, and the remaining bytes are stored in the Host Block Data Byte register.
The Byte Done Status bit in the Host Status Register will be set 1 when the master has received a byte (for

Block Read commands) or if it has completed transmission of a byte (for Block Write commands).
Note: On the block read command, software shall write 1 to LAST BYTE bit in Host Control Register when the next byte will be the last byte to be received.

I2C Block Read
This command allows the SMBus logic to perform block reads to I2C devices in a 10-bit addressing mode.
In I2C Block Read Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent. Bit 0 of the Transmit Slave Address Register has to be 0. The received data is stored in the Host Block Data Byte register.

I2C-compatible Write Command
In I2C-compatible Write Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent and the transmitted data is set in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set to 1 when the host has completed transmission of a byte.

Note: Software shall write 0 to I2C_EN bit in Host Control Register 2 when the cycle is decided to be finished.

I2C-compatible Read Command
In I2C-compatible Read Command, the Transmit Slave Address Register is sent and the received data is stored in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set to 1 when the host has received a byte.

Note: Software shall write 1 to LABY bit in the Host Control Register when the next byte to be received is the last one.

I2C-compatible Combined Command
This command allows the SMBus logic to perform direction switch from I2C Write Command to I2C Read Command or from I2C Read Command to I2C Write Command in I2C-compatible cycles.
In I2C-compatible Combined Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent. Bit 0 of the Transmit Slave Address Register is set to decide the direction of the cycle and the received data is also stored in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set 1 when the host has completed transmission of a byte or received a byte.

Note: Software shall control the I2C_SW_EN bit and I2C_SW_WAIT bit in Host Control Register 2 when the direction switch is decided to be performed.

Block Write Command (FIFO Mode)
In the Block Write command(FIFO Mode), the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register (byte count, if I2C_EN = 0) are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. The data is then sent from FIFO. (Software shall write data to the Host Block Data Byte Register depending on byte count set in Data 0 Register). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

Block Read Command (FIFO Mode)
In the Block Read commands(FIFO Mode), the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1. When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt. Software read the data from the Host Data 0 Register to get the byte count, and read the data from the Host Block Data Byte Register to get the received data bytes. If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

I2C-compatible Write Command (FIFO Mode)
In I2C-compatible Write Command(FIFO Mode), the Transmit Slave Address Register and Host Block Data

Byte Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. When the datas in the FIFO have been transmitted, an interrupt will be generated. If the byte count is less than 32, software can read the Host Status Register to know the source of the interrupt(Finish interrupt is 1) or check FIFO Block Done status when this transmission is over 32 data bytes(byte count > 32). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Block Done Status bit in the FIFO Control Register, then HW would transmit the successive bytes from FIFO. When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

I2C-compatible Read Command (FIFO Mode)
In I2C-compatible Read Command(FIFO Mode), the Transmit Slave Address Register is sent (Software shall write data to this register). Bit 0 of the Transmit Slave Address Register has to be 1 and the received data byte is stored in the Host Block Data Byte Register. When the datas have been received to FIFO, an interrupt will be generated. If the byte count is less than 32, software can read the Host Status Register to know the source of the interrupt(Finish interrupt is 1). Software can get FIFO datas through Host Block Data Byte Register or check FIFO Block Done status when this transmission is over 32 data bytes(byte count > 32). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Block Done Status bit in the FIFO Control Register, then HW would receive the successive bytes into FIFO. When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

7.8.3.2 SMBus Slave Interface

The slave supports the following three types of messages: Byte Write, Byte Read, and Host Notify. Furthermore, Slave channel A also supports 16-byte FIFO for read/write (FIFO Mode). Slave FIFO also supports threshold function. Threshold function lets software process part of FIFO data before FIFO becomes empty and it can improve the transmission performance of the bus.

When an interrupt to INTC (INT9 for SMBus slave) is detected, software can read the slave Status Register to know the interrupt source. There are 4 interrupt conditions: STOP Condition Detect Status, Slave Timeout Status, Slave Data Status, and Host Notify Status. In the Byte Write/Byte Read command, software must write/read data in the slave Data Register twice to release the SMCLK line. For the first time, software would set/get data in the slave Data Register, but the SMCLK line would not be released. The SMCLK line would be held low until software writes/reads data in the slave Data Register for the second time, after which the SMCLK line would be reelased.

SMBus Slave will issue INT81 for the occurrance of Clock Held event.
Here are the steps Software shall follow:

1. Enable the slave stretch clock low bit of HOCTL2_A or HOCTL2_B register. SMBus Slave will hold Smbus clock to low after the start bit is received. If the control bit is set, this register required to be set before entering the sleep mode.
2. When INT81 is generated, the software shall check SSSLS bit of SLSTA_A and SLSTA_B Register to know which slave side is stretching SMBCLK low.
3. Software can disable slave stretch clock low function to release clock by writing the slave stretch clock low bit to zero.
4. After the above steps, SMBus Master side will get bus control and continually send data bit to Slave side.

Byte Write
In the byte write command, the value of the first received byte (Slave Address) must match the value in Receive Slave Address Register. If the value of the first received byte matches, the second byte (Command Data) will be received and stored in the slave Data Register and waiting for the software to read the data (for the first time). The SMCLK line will be held low until the data is read (for the second time). After the data is read, the third byte (Data) is received and stored in the slave Data Register and waiting for the software to read the data (for the first time). The SMCLK line will be held low until the data is read (for the second time).

Byte Read
In the byte read command, the value of the first received byte (Slave Address) must match the value in Receive

Slave Address Register. If the value of the first received byte matches, the second byte (Command Data) will be received and stored in the slave Data Register and waiting for the software to read the data (for the first time). The SMCLK line will be held low until the data is read (for the second time). After the Repeated Start and Slave Address cycle, the software shall write the data to the slave Data Register (for the first time) and this register will be sent during the Data Byte Cycle. The SMCLK line will be held low until the data is set in the slave Data Register for the second time, after which the SMCLK line would be reelased.

Host Notify Command
In the host notify command, the first received byte must be 0001000b. The second received byte is stored in the Notify Device Address Register. The next two bytes are stored in the Notify Data Low Byte Register and Notify Data High Byte Register.

7.8.3.3 SMBus Porting Guide

(1).SMBus Master Interface:

The SMBus controller requires that various data and command registers be setup for the message to be sent. When the START bit in the Host Control Register is set, the SMBus controller will perform the requested transaction. Any register values needed for computation purposes should be saved prior to issuing of a new command.

The "Timing Registers" (00h~07h) should be programmed before the transaction starts. In addition, the SMCLK frequency of channel A~C can be switched independently to 50 kHz, 100 kHz, or 400 kHz by setting the registers 09h~0Ah, which means SMCLK timing doesn't relate to "Timing Register (00h~07h)." Besides the 25ms Register, all of the other count numbers are based on EC clock. For example, write the 1Bh (37 / FreqEC ~= 4.0us) into the 4.0us register.
(FreqEC is listed in Table 10-2 on page 570 and this example assumes FreqEC = 8 MHz.)

The IT81202 SMBus Interface can perform SMBus messages with either packet error checking (PEC) enabled or disabled (PEC_EN bit = 1 or 0 in the Host Control Register). The actual PEC calculation and checking is performed in software.
Here is the steps the software shall follow to program the registers for various command.

1. Quick Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Quick Command, the Transmit Slave Address Register is sent (Software shall write data to the Transmit Slave Address Register).
(3). Start the transaction (Write 41h to the Host Control Register, which will select the "Quick Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt is generated. Software can read the Host Status Register to know the source of the interrupt.

Note: After reading the Status Register, the software must write 1 to clear it.

2. Send Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Send Byte Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to the Transmit Slave Address Register and Host Command Register) (Host Command Register is used for transmitting data here). Bit 0 of the Transmit Slave Address Register has to be 0.
(3). Start the transaction (Write 45h to the Host Control Register, which will select the "Send Byte/Receive Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host

Status Register to know the source of the interrupt.

3. Receive Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Receive Byte Command, the Transmit Slave Address Register is sent (Software shall write data to the Transmit Slave Address Register). Bit 0 of the Transmit Slave Address Register has to be 1.
(3). Start the transaction (Write 45h to the Host Control Register, which will select the "Send Byte/Receive Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.
(5). In Receive Byte Command, the received data is stored in the Host Data 0 Register. Software can read this register to get the data.

4. Write Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Write Byte Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Packet Error Check Register and this register will be sent, too.
(3). Start the transaction (Write 49h to the Host Control Register, which will select the "Write Byte/Read Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.

5. Write Word Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Write Word Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Packet Error Check Register. And this register will be sent, too.
(3). Start the transaction (Write 4dh to the Host Control Register, which will select the "Write Word/Read Word Command", enable the interrupts, and start the transaction).
(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

6. Read Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Read Byte Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
(3). Start the transaction (Write 49h to the Host Control Register, which will select the "Write Byte/Read Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
(5). In Read Byte Command, the data received is stored in the Host Data 0 Register. Software can read this register to get the data.

If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

7. Read Word Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Read Word Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
(3). Start the transaction (Write 4dh to the Host Control Register, which will select the “Write Word/Read Word Command”, enable the interrupts, and start the transaction).
(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
(5). In Read Word Command, the received data is stored in the Host Data 0 Register and Host Data 1 Register. Software can read these registers to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

8. Process Call Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Process Call Command will skip the command code.
(3). In Process Call Command, the Transmit Slave Address Register, Host Command Register (if I2C_EN = 0), Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
(4). Start the transaction (Write 51h to the Host Control Register, which will select the “Process Call Command”, enable the interrupts, and start the transaction).
(5). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
(6). In Process Call Command, the received data is stored in the Host Data 0 Register and Host Data 1 Register. Software can read these registers to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

Note: The I2C_EN bit and PEC_EN bit can’t be set high at the same time. It will produce the undefined results.

9. Block Write Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Block Write Command will skip sending the byte count (Host Data 0 Register).
(3). In Block Write Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register (byte count, if I2C_EN = 0) are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. The data is then sent from the Host Block Data Byte Register (Software shall write data to this register).
(4). Start the transaction (Write 55h to the Host Control Register, which will select the “Block Read/Block Write Command”, enable the interrupts, and start the transaction).
(5). When the data in Host Block Data Byte Register is sent, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software writes the data to the Host Block Data Byte Register, then the data is sent from this register by SMBus logic.
(7). Repeat step (5) and (6) for the other data byte until all of the data were sent.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Packet Error

Check Register and this register will be sent, too.

(8). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

10. Block Read Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Block Read Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
(3). Start the transaction (Write 55h to the Host Control Register, which will select the "Block Read/Block Write Command", enable the interrupts, and start the transaction).
(4). When the byte count and the first byte data are received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(5). Software read the data from the Host Data 0 Register to get the byte count, and read the data from the Host Block Data Byte Register to get the first data byte.
(6). When the next data is received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(7). Software read the data from the Host Block Data Byte Register to get the data.
(8). Repeat step (6) and (7) until the last byte.
(9). Set the LAST BYTE bit in the Host Control Register to indicate that the next byte will be the last byte to be received.
(10). Get an interrupt and receive the last byte.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

11. I2C Block Read Command

This command allows the SMBus logic to perform block reads to I2C devices in a 10-bit addressing mode.

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In I2C Block Read Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
(3). Start the transaction (Write 59h to the Host Control Register, which will select the "I2C Block Read Command", enable the interrupts, and start the transaction).
(4). When the data is received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(5). Software can read the data from the Host Block Data Byte Register to get the data.
(6). Repeat step (4) and (5) until the last byte.
(7). Set the LAST BYTE bit in the Host Control Register to indicate that the next byte will be the last byte to be received.
(8). Get an interrupt and receive the last byte.

12. I2C-compatible Write Command

(1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit in the Host Control Register 2 to 1.
(3). In I2C-compatible Write Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
(4). Start the transaction (Write 5Dh to the Host Control Register, which will select the "Extend Command", enable the interrupts, and start the transaction).
(5). When the data in the Host Block Data Byte Register has been transmitted, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).

(6). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register. Then, the data is transmitted from this register by the SMBus logic.
(7). Repeat step (5) and (6) for the other data bytes until software wants to finish the cycle.
(8). If software wants to finish the cycle, set I2C_EN bit in the Host Control Register 2 to 0 after the last transmitted data byte has been sent (Byte Done interrupt is generated).
(9). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

13. I2C-compatible Read Command

(1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit in the Host Control Register 2 to 1.
(3). In I2C-compatible Read Command, the Transmit Slave Address Register is sent (Software shall write data to this register). Bit 0 of the Transmit Slave Address Register has to be 1 and the received data byte is stored in the Host Block Data Byte Register.
(4). Start the transaction (Write 5Dh to the Host Control Register, which will select the “Extend Command”, enable the interrupts, and start the transaction).
(5). When the data has been received from the Host Block Data Byte Register, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register.
(7). Repeat step (5) and (6) for the other data bytes until the last byte is going to be received.
(8). Set the LABY bit in the Host Control Register after the Byte Done interrupt is generated to indicate that the next byte will be the last to be received.
(9). Get the Byte Done interrupt of the last byte, and receive the last data byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

14. I2C-compatible Combined Command

This command allows the SMBus logic to perform direction switch from I2C Write Command to I2C Read Command or from I2C Read Command to I2C Write Command in the I2C-compatible cycles.

From I2C Write Command to I2C Read Command:
(1). In the I2C Write Command mentioned above, software can control the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to switch the direction to the I2C Read Command.
(2). After the last transmitted data byte has been sent in the I2C Write Command, the Byte Done interrupt will be generated. Then, software can set 1 to the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to make the SMBus logic wait for the setting by software for the I2C Read Command.
(3). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(4). Set 0 to the I2C_SW_WAIT bit in the Host Control Register 2 to start the I2C Read Command.
(5). When the data has been received and stored in the Host Block Data Byte Register, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register.
(7). Repeat step (5) and (6) for the other data bytes until the last byte is going to be received.
(8). Set the LABY bit in the Host Control Register after the Byte Done interrupt is generated to indicate that the next byte will be the last to be received.
(9). Get the Byte Done interrupt of the last byte, and receive the last data byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

From I2C Read Command to I2C Write Command:

(1). In the I2C Read Command mentioned above, software can control the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to switch the direction to the I2C Write Command.
(2). In the I2C Read Command, after setting the LABY bit in the Host Control Register, software can set 1 to the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to make the SMBus logic wait for the setting by software for the I2C Write Command.
(3). Get the Byte Done interrupt of the last byte, and receive the last byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(4). Software writes the transmitted data byte in the Host Block Data Byte Register.
(5). Set 0 to the I2C_SW_WAIT bit in the Host Control Register 2 to start the I2C Write Command.
(6). When the data in the Host Block Data Byte Register has been sent, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(7). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register. Then, the data is sent from this register by the SMBus logic.
(8). Repeat step (6) and (7) for the other data bytes until software wants to finish the cycle.
(9). If software wants to finish the cycle, set I2C_EN bit in the Host Control Register 2 to 0 after the last transmitted data byte has been sent (Byte Done interrupt is generated).
(10). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(11). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

15. Block Write Command (FIFO Mode)

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).
(2). Enable Master FIFO Mode.
(3). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Block Write Command will skip sending the byte count (Host Data 0 Register).
(4). In Block Write Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register (byte count, if I2C_EN = 0) are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. The data is then sent from FIFO. (Software shall write data to the Host Block Data Byte Register depending on byte count set in Data 0 Register).
(5). Start the transaction (Write 55h to the Host Control Register, which will select the “Block Read/Block Write Command”, enable the interrupts, and start the transaction).
(6). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

Note: The I2C_EN bit and PEC_EN bit can’t be set high at the same time. It will produce the undefined results.

16. Block Read Command (FIFO Mode)

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). Enable Master FIFO Mode
(3). In Block Read Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
(4). Start the transaction (Write 55h to the Host Control Register, which will select the “Block Read/Block Write Command”, enable the interrupts, and start the transaction).
(5). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
(6). Software reads the data from the Host Data 0 Register to get the byte count, and read the data from the Host Block Data Byte Register to get the received data bytes. If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

17. I2C-compatible Write Command (FIFO Mode)

(1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit in the Host Control Register 2 to 1.
(3). Enable Master FIFO Mode.
(4). Write byte count value to Data 0 register to indicate HW how many bytes will (should) be transmitted.
(5). In I2C-compatible Write Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
(6). Write data bytes to FIFO through Host Block Data Byte Register.
(7). Start the transaction (Write 5Dh to the Host Control Register, which will select the "Extend Command", enable the interrupts, and start the transaction).
(8). When the datas in the FIFO have been transmitted, an interrupt will be generated. If the byte count is less than 32, software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).
(9). Or check FIFO Block Done status when this transmission is over 32 data bytes (byte count > 32).
(10). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Block Done Status bit in the FIFO Control Register, then HW will transmit the successive bytes from FIFO.
(11). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1). If this cycle is not completed yet, then go to step (9) again.

18. I2C-compatible Read Command (FIFO Mode)

(1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit in the Host Control Register 2 to 1.
(3). Enable Master FIFO Mode.
(4). Write byte count value to Data 0 register to indicate HW how many bytes will (should) be received.
(5). In I2C-compatible Read Command, the Transmit Slave Address Register is sent (Software shall write data to this register). Bit 0 of the Transmit Slave Address Register has to be 1 and the received data byte is stored in the Host Block Data Byte Register.
(6). Start the transaction (Write 5Dh to the Host Control Register, which will select the "Extend Command", enable the interrupts, and start the transaction).
(7). When the datas have been received to FIFO, an interrupt will be generated. If the byte count is less than 32, software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).
(8). Software can get FIFO datas through Host Block Data Byte Register.
(9). Or check FIFO Block Done status when this transmission is over 32 data bytes (byte count > 32).
(10). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Block Done Status bit in the FIFO Control Register, then HW will receive the successive bytes into FIFO.
(11). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1). If this cycle is not completed yet, then go to step (9) again.

(2).SMBus Slave Interface:

The slave supports three types of messages: Byte Write, Byte Read, and Host Notify.
Here are the steps the software shall follow to program the registers for various commands.

1. Byte Write

(1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).
(2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
(3). Write a slave address to Receive Slave Address Register. Now the SMBus logic is ready to respond the data transmission from the external SMBus device.
(4). When an interrupt is generated, the software can read the slave Status Register to know the source of

the interrupt (It shall be 02h for Byte Write Command).

(5). Software can read the data from the slave Data Register for the first time. (This data byte is the command code.) The SMCLK line would be held low until software reads the data for the second time.

(6). When the next interrupt is generated, the software can read the slave Status Register to know the source of the interrupt (It shall be 02h for Byte Write Command).

(7). Software can read the data from the slave Data Register for the first time. (This data byte is the Data Byte in SMBus Protocol.) The SMCLK line would be held low until software reads the data for the second time, after which the SMCLK line would be reelased.

2. Byte Read

(1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).

(2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).

(3). Write a slave address to Receive Slave Address Register. Now the SMBus logic is ready to respond the data transmission from the external SMBus device.

(4). When an interrupt is generated, the software can read the slave Status Register to know the source of the interrupt (It shall be 02h for Byte Read Command).

(5). Software can read the data from the slave Data Register for the first time. (This data byte is the command code.) The SMCLK line would be held low until software reads the data for the second time, after which the SMCLK line would be reelased.

(6). When the next interrupt is generated, the software can read the slave Status Register to know the source of the interrupt (It shall be 0Ah for Byte Read Command).

(7). Software can write the data to the slave Data Register for the first time. (This data will be sent to the external device.) The SMCLK line would be held low until software reads the data for the second time, after which the SMCLK line would be reelased.

3. Host Notify Command

(1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).

(2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).

(3). When an interrupt is generated, the software can read the slave Status Register to know the source of the interrupt (It shall be 01h for Host Notify Command).

(4). Software can read the data from the Notify Device Address Register, Notify Data Low Byte Register, and Notify Data High Byte Register.

Furthermore, Slave channel A also supports 16-byte FIFO for read/write (FIFO Mode). Slave FIFO also supports threshold function. Threshold function lets software process part of FIFO data before FIFO becomes empty and it can improve the transmission performance of the bus.

For slave 16-byte FIFO mode, software needs to enable the slave FIFO mode (Write 01h to Slave FIFO Control Register (SLVFFCTL)Register). If the master wants to write any data to the slave, the slave side INT9 is generated and the software can read the slave Status Register to know the source of the interrupt as well as read the slave FIFO status register to know the length of FIFO bytecnt. Software can read data from the slave Data Register continuously according to the bytecnt. If the master wants to read any data from the slave, the slave side INT9 is generated and the software can read the slave Status Register to know the source of the interrupt as well as write data to the slave Data Register continuously.

(3). Pre-defined Command:

Slave channel A also supports pre-defined command. Whether function is enabled or not is controlled by writing 1 to HSPE bit of SFFCTL register and the dedicated pre-defined slave address is 0x5C. The supported protocols are listed below.

1. Reset through I2C:

Reset

S	5ch	W	A	5ah	A	a5h	A	P

Assert reset to EC.

2. I2EC through I2C:

I2EC Address Write

S	5ch	W	A	10h	A	EC Address[23:16]	A	EC Address[15:8]	A	EC Address[7:0]	A	P

I2EC Address Read

S	5ch	W	A	10h	A	S	5ch	R	A	EC Address[23:16]	A	EC Address[15:8]	A	EC Address[7:0]	A	P

I2EC Data Write

S	5ch	W	A	11h	A	EC Data[7:0]	A	P

I2EC Data Read

S	5ch	W	A	11h	A	S	5ch	R	A	EC Data[7:0]	A	P

(1). I2EC Write:

- Specify the targeted address of EC memory through “I2EC Address Write”.
- Write EC memory addressed by the targeted address through “I2EC Data Write”.

I2EC Address Write → I2EC Data Write

(2). I2EC Read:

- Specify the targeted address of EC memory through “I2EC Address Write”.
- Read EC memory addressed by the targeted address through “I2EC Data Read”.

I2EC Address Write → I2EC Data Read

3. IO Read through I2C:

IO Address Write

S	5ch	W	A	12h	A	IO Address[15:8]	A	IO Address[7:0]	A	P

IO Address Read

S	5ch	W	A	12h	A	S	5ch	R	A	IO Address[15:8]	A	IO Address[7:0]	A	P

IO Data Write

S	5ch	W	A	13h	A	IO Data[7:0]	A	P

IO Data Read

S	5ch	W	A	13h	A	S	5ch	R	A	IO Data[7:0]	A	P

(1). IO Write:

IO Address Write → IO Data Write

(2). IO Read:

IO Address Write → IO Data Read

4. Flash Read through I2C:

Flash Address Write

S	5ch	W	A	14h	A	Flash Address[23:16]	A	Flash Address[15:8]	A	Flash Address[7:0]	A	P

Flash Address Read

S	5ch	W	A	14h	A	S	5ch	R	A	Flash Address[23:16]	A	Flash Address[15:8]	A	Flash Address[7:0]	A	P

Flash Data Read

S	5ch	W	A	15h	A	S	5ch	R	A	Flash Data[7:0]	A	P

Flash Data Read (auto increase address)

S	5ch	W	A	16h	A	S	5ch	R	A	Flash Data[7:0]	A	Flash Data[7:0]	A	....	P
										(Flash Address)		(Flash Address + 1)			

(1). Flash Read:

- Specify the targeted address of Flash memory through “Flash Address Write”.
- Read Flash memory addressed by the targeted address through “Flash Data Read”.

Flash Address Write → Flash Data Read

5. Follow Mode for SPI Bus through I2C:

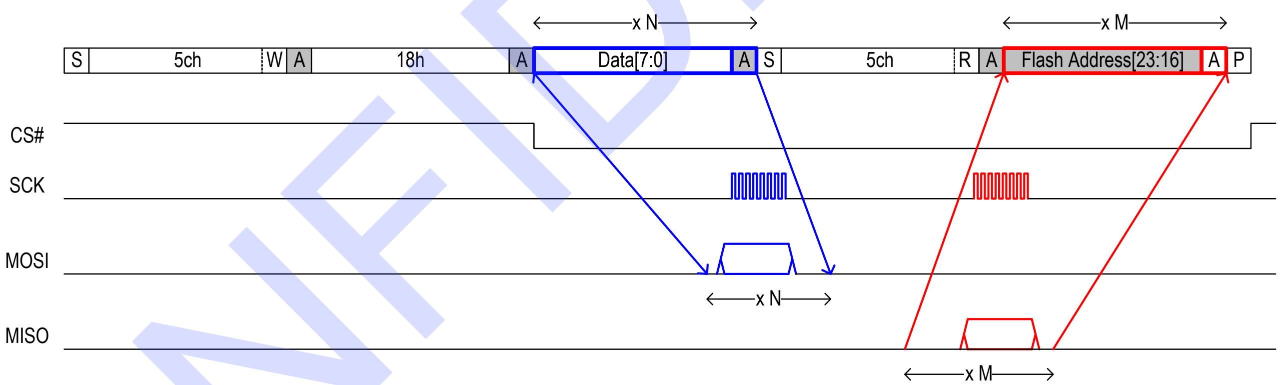
Set CS# of SPI Bus High

S	5ch	W	A	17h	P

Transfer Write/Read Cycle to SPI Bus

S	5ch	W	A	18h	A	Data[7:0]	A	S	5ch	R	A	Flash Address[23:16]	A	P
						x N						x M		

(1). Always execute “Set CS# of SPI Bus high” first.
(2). Use “Transfer Write/Read Cycle to SPI Bus” to generate the SPI cycle.



6. Fast AAIW:

(1). Use “Follow Mode for SPI Bus through I2C” to construct the AAIW cycle with addresses. That is

a. Let CS# of SPI Bus high
b. Write adh
c. Write address[23:16]
d. Write address[15:8]
e. Write address[7:0]
f. Write Data 0
g. Write Data 1
h. Let CS# of SPI Bus high

(2). Use “Follow Mode for SPI Bus through I2C**”** to construct the RDSR cycle. That is

a. Let CS# of SPI Bus high
b. Write 05h
c. Polling status until flash returns non-busy
d. Let CS# of SPI Bus high

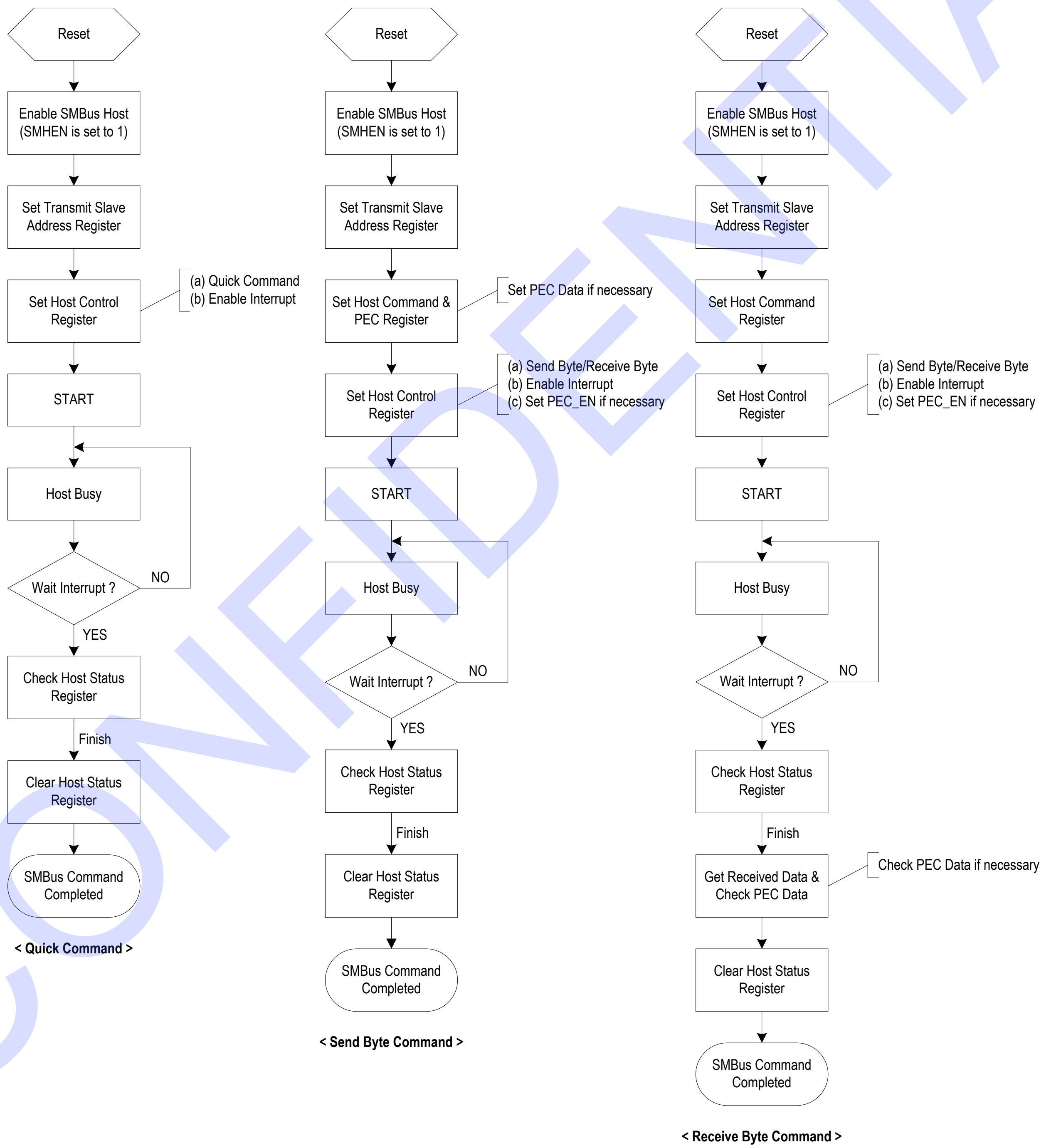
(3). Use “Fast data-insertion for AAIW” to write the remaining data.

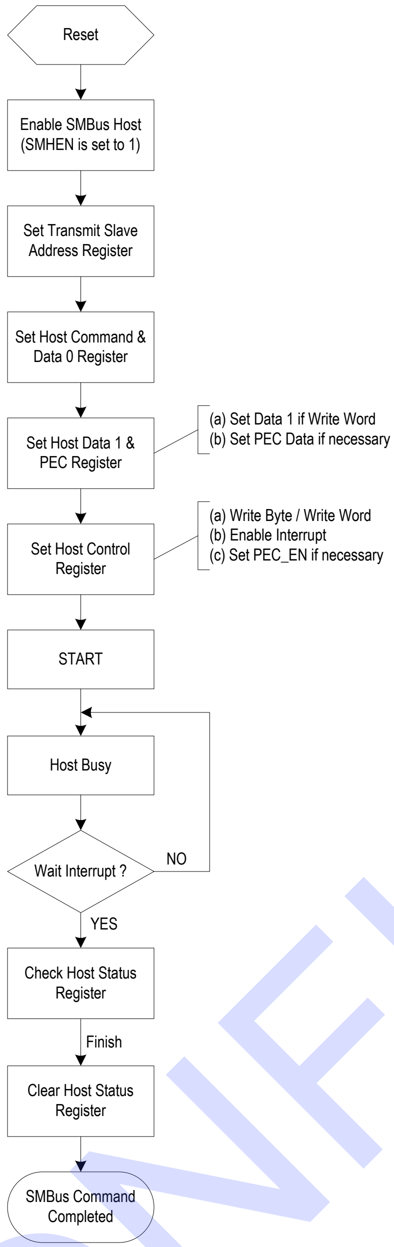
Fast data-insertion for AAIW

S	5ch	W	A	adh	A	Data 2	A	Data 3	A	⋯	Data N	A	P

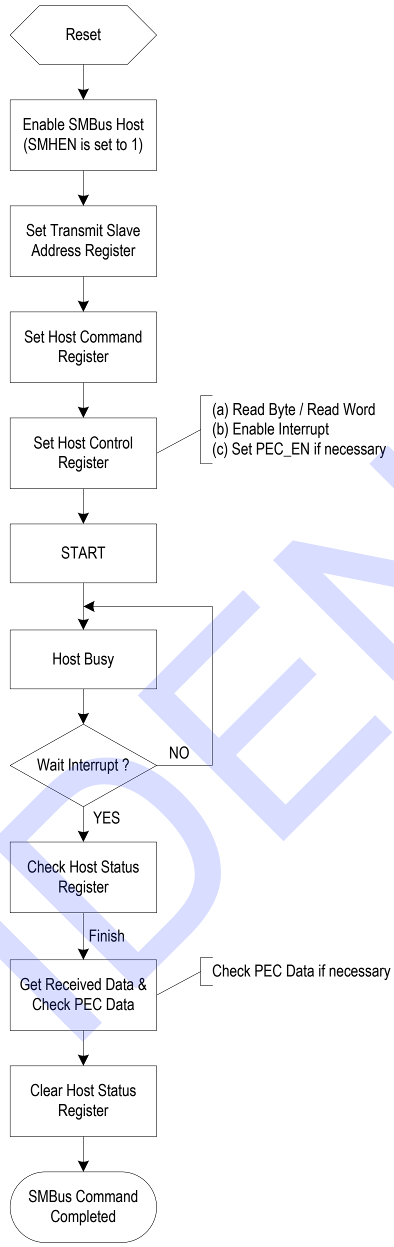
7.8.3.4 SMBus Master Programming Guide

Figure 7-10. Program Flow Chart of SMBus Master Interface

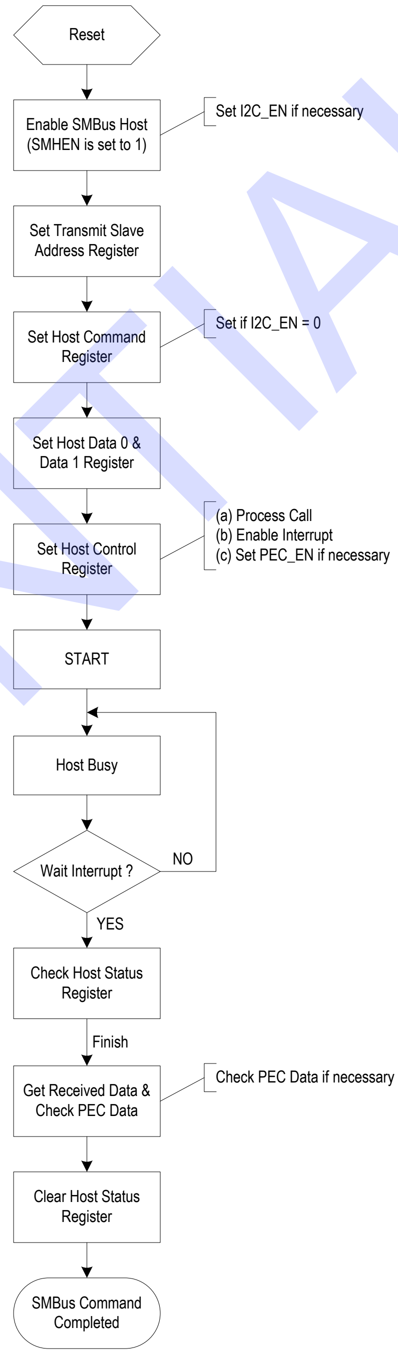




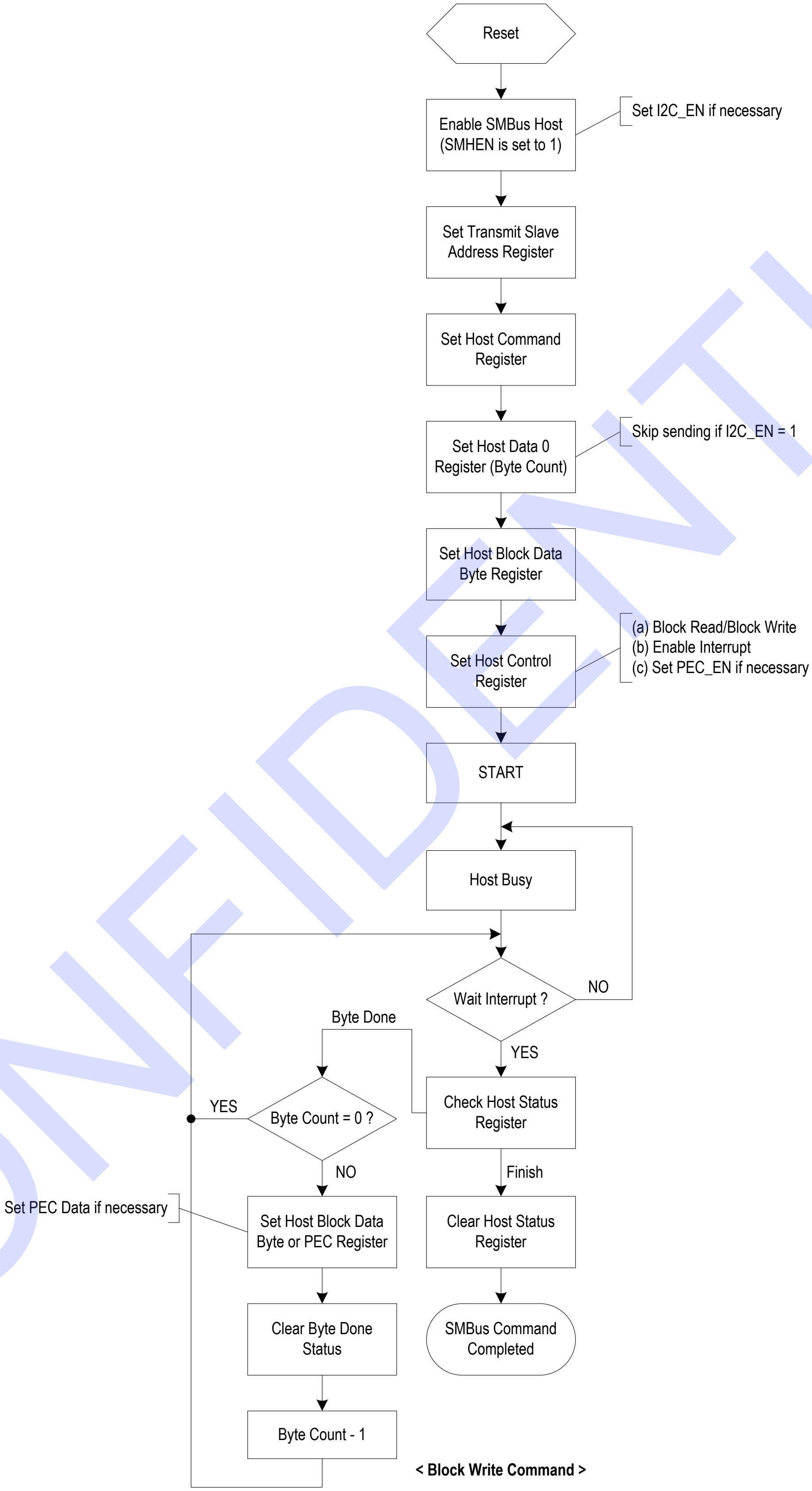
< Write Byte / Word Command >



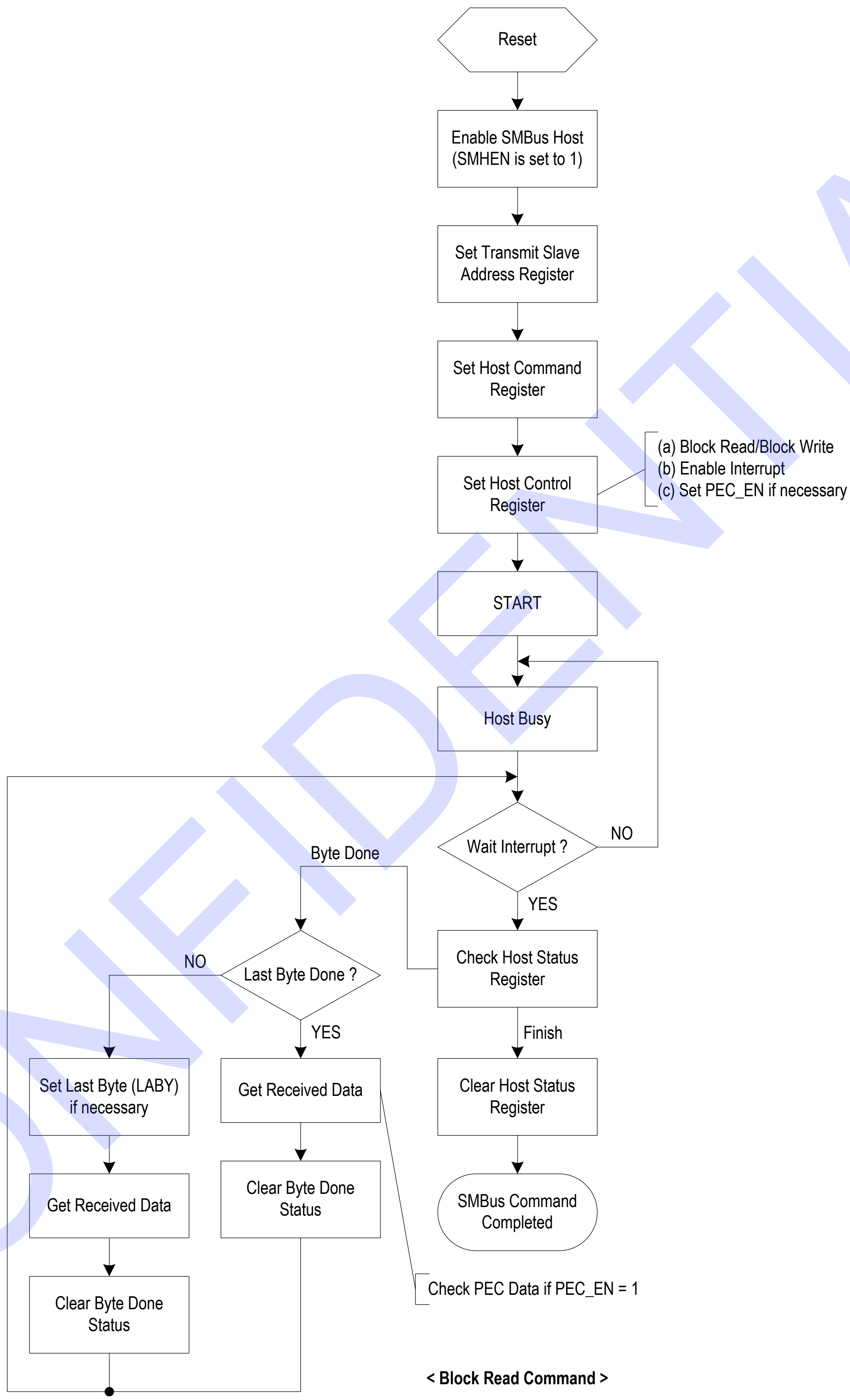
< Read Byte / Word Command >



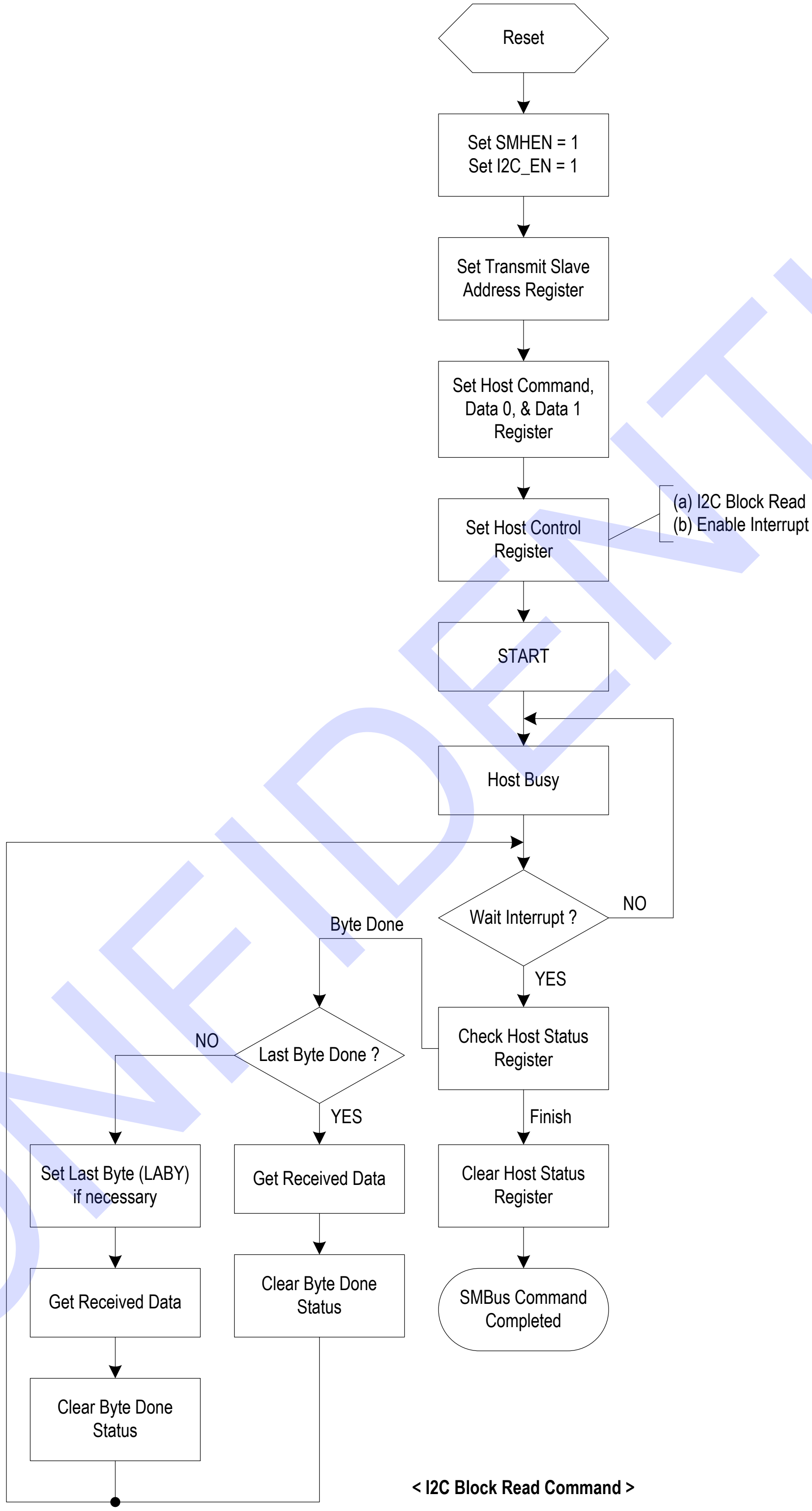
< Process Call Command >



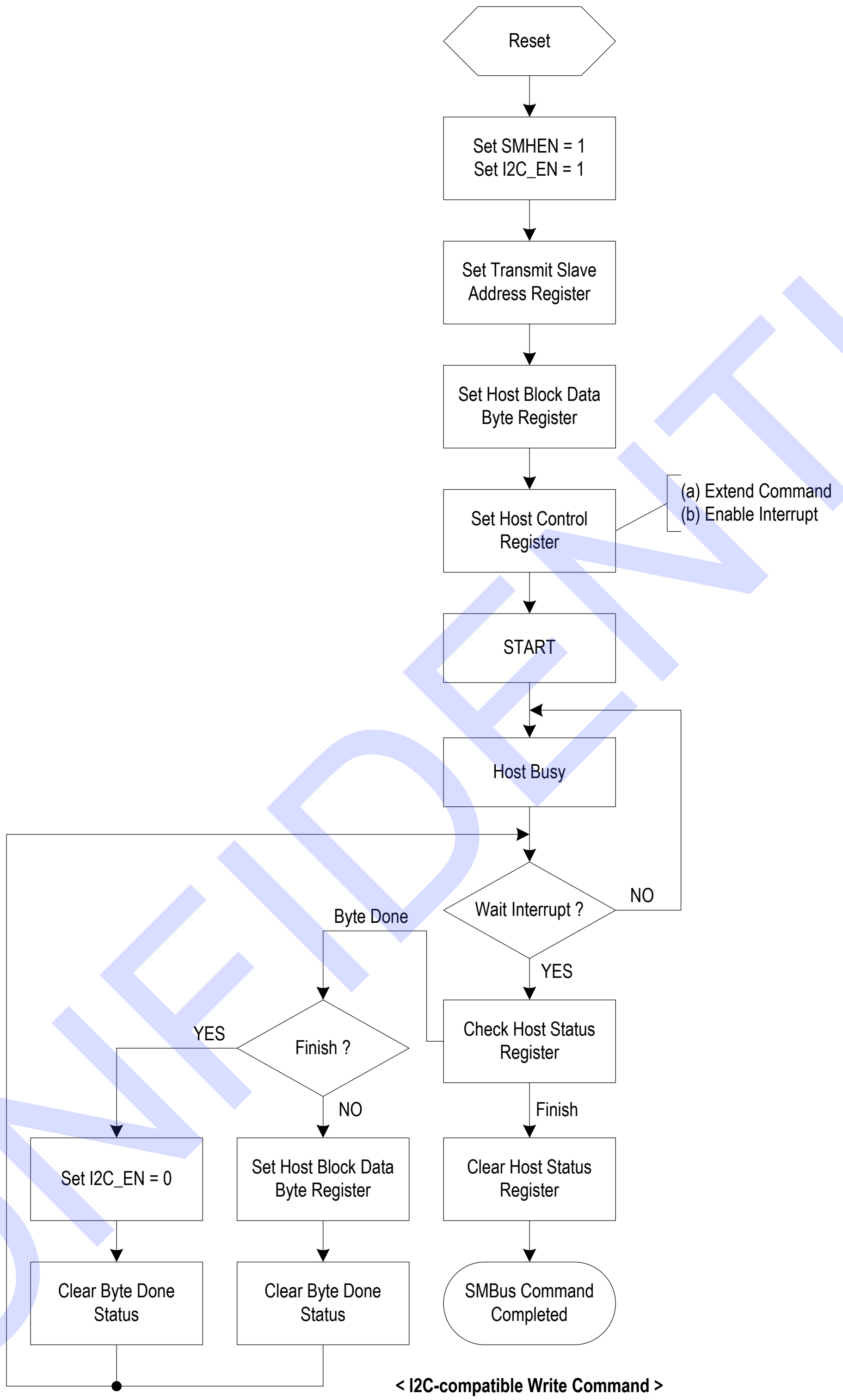
< Block Write Command >



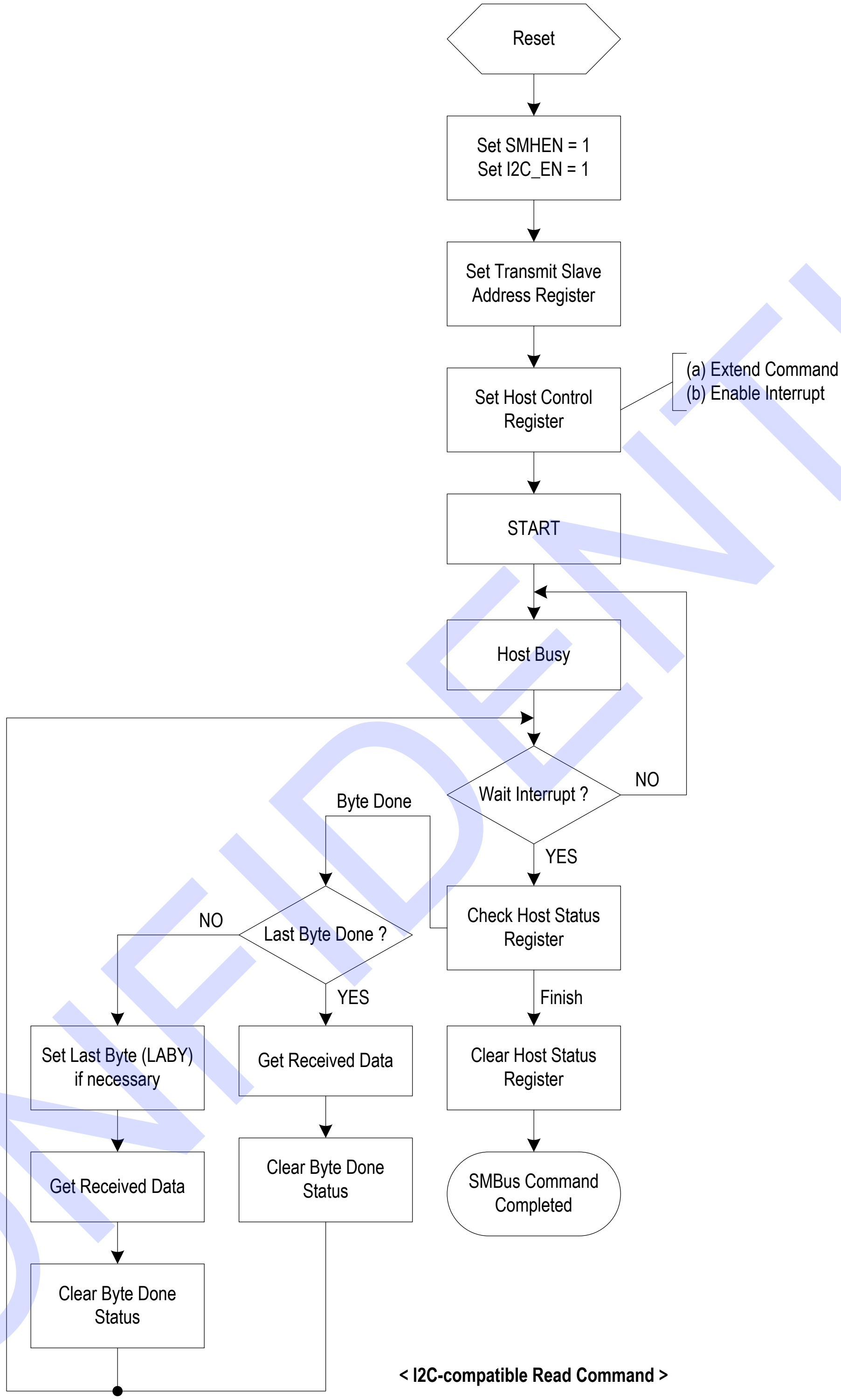
< Block Read Command >



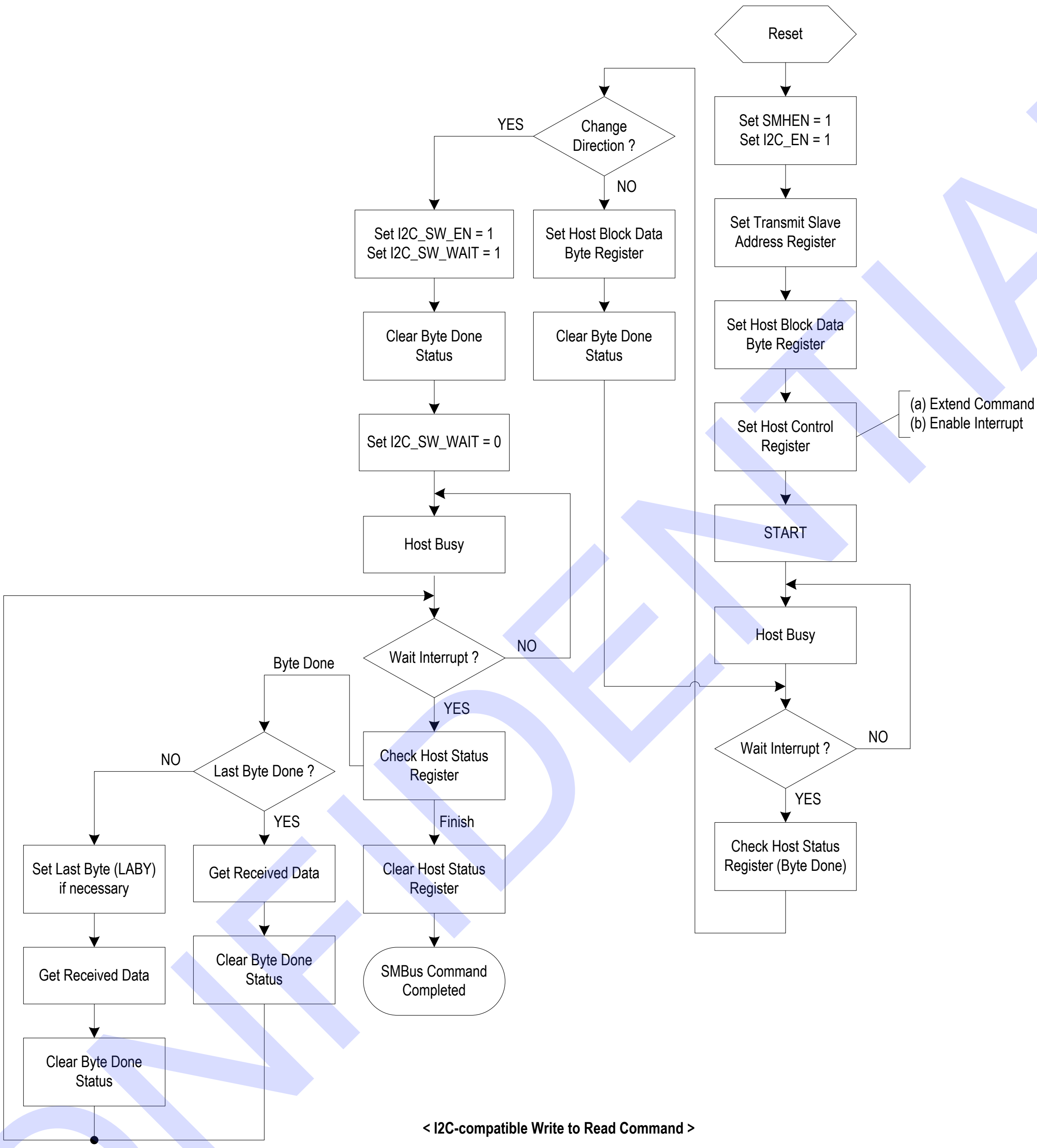
< I2C Block Read Command >



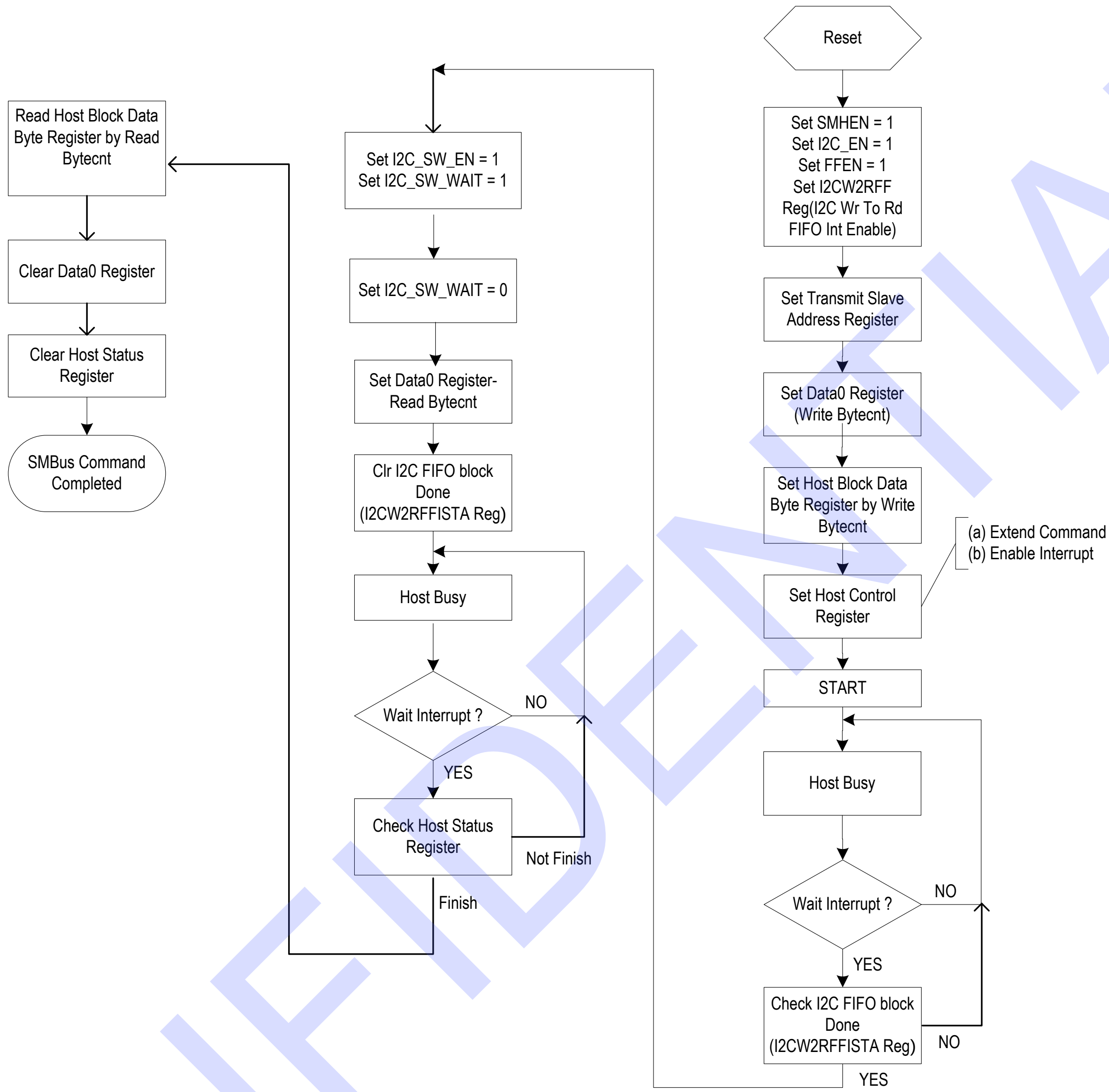
< I2C-compatible Write Command >



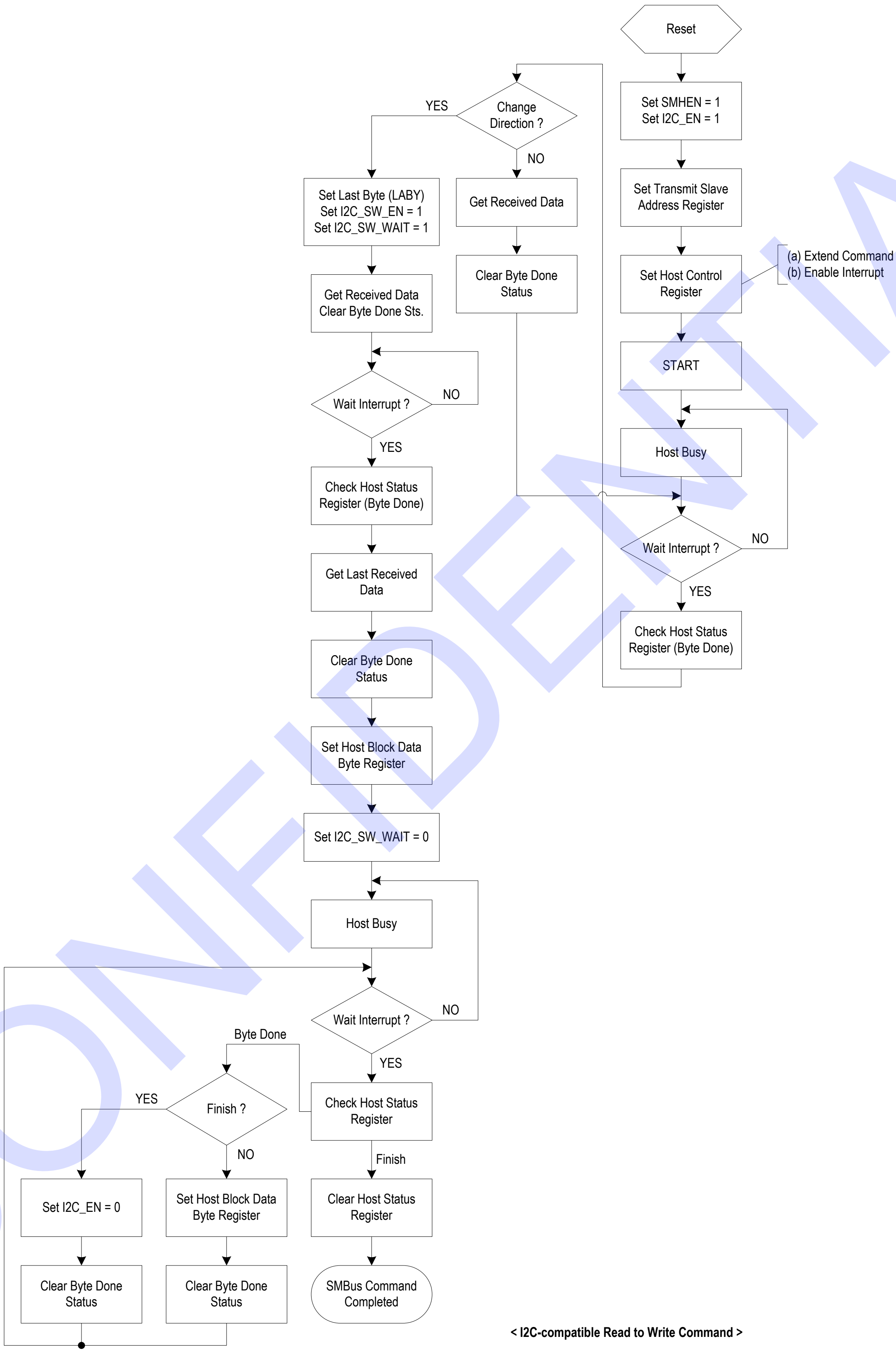
< I2C-compatible Read Command >



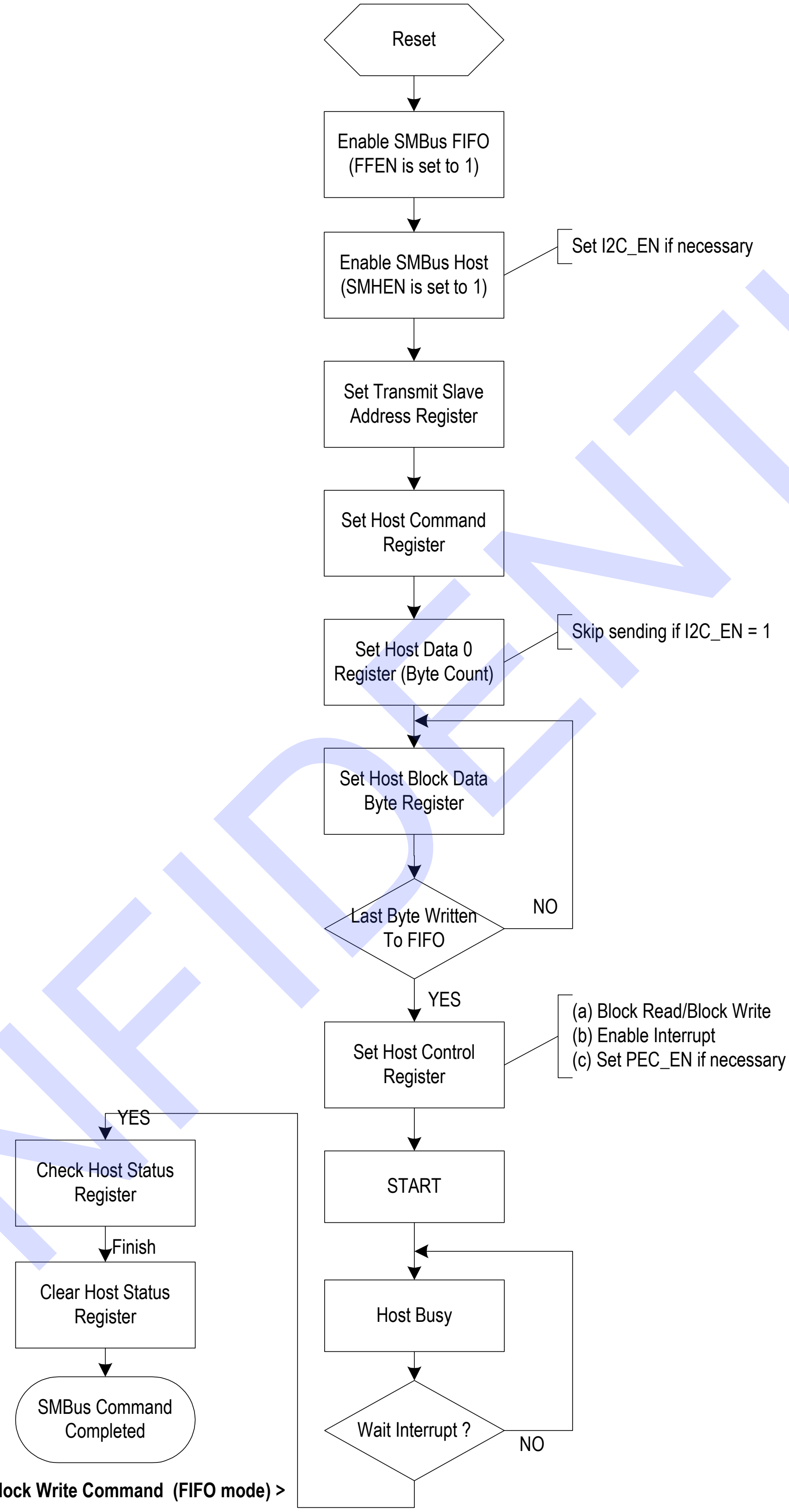
< I2C-compatible Write to Read Command >



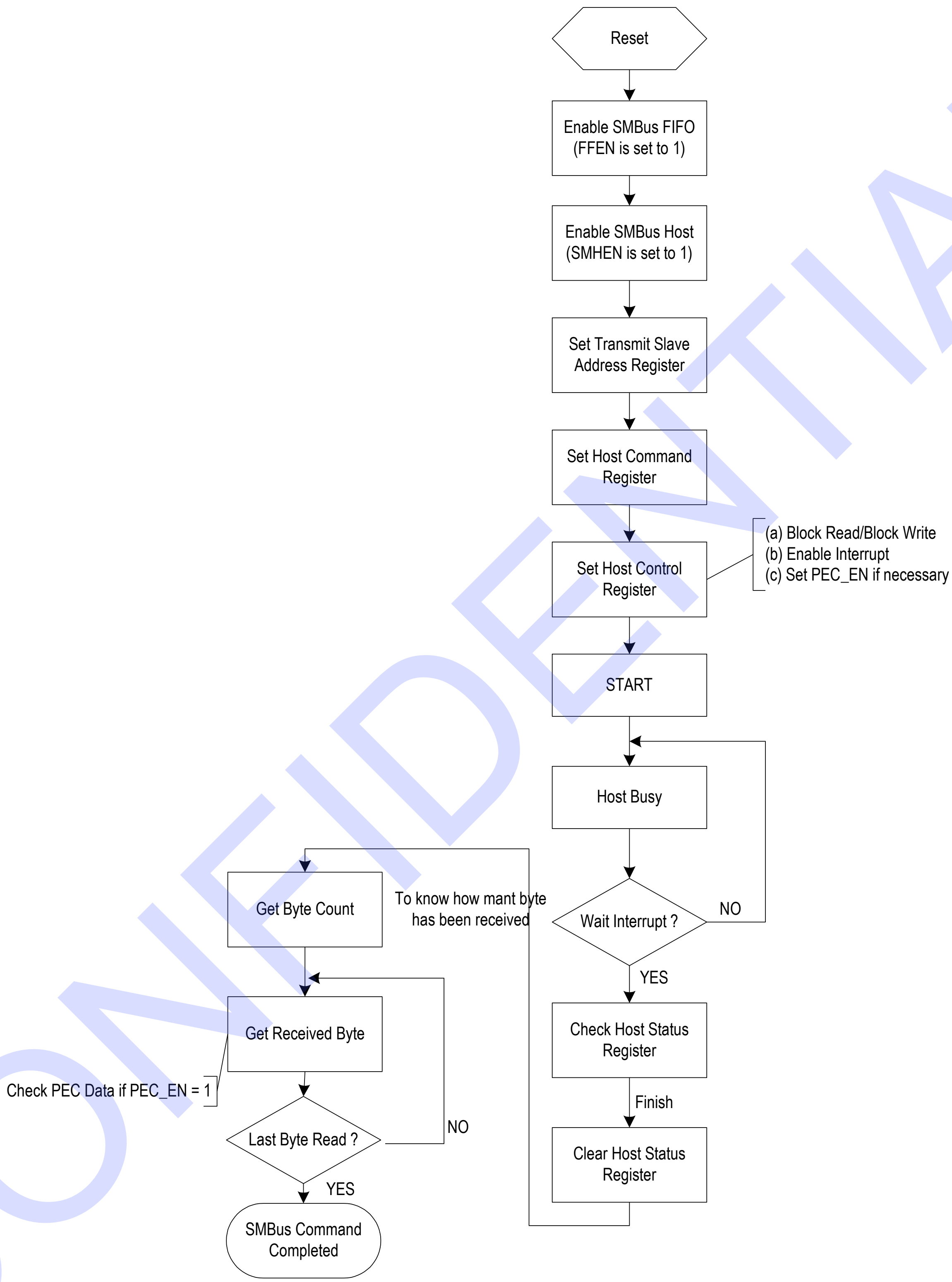
< I2C-compatible Write to Read Command (FIFO Mode) >



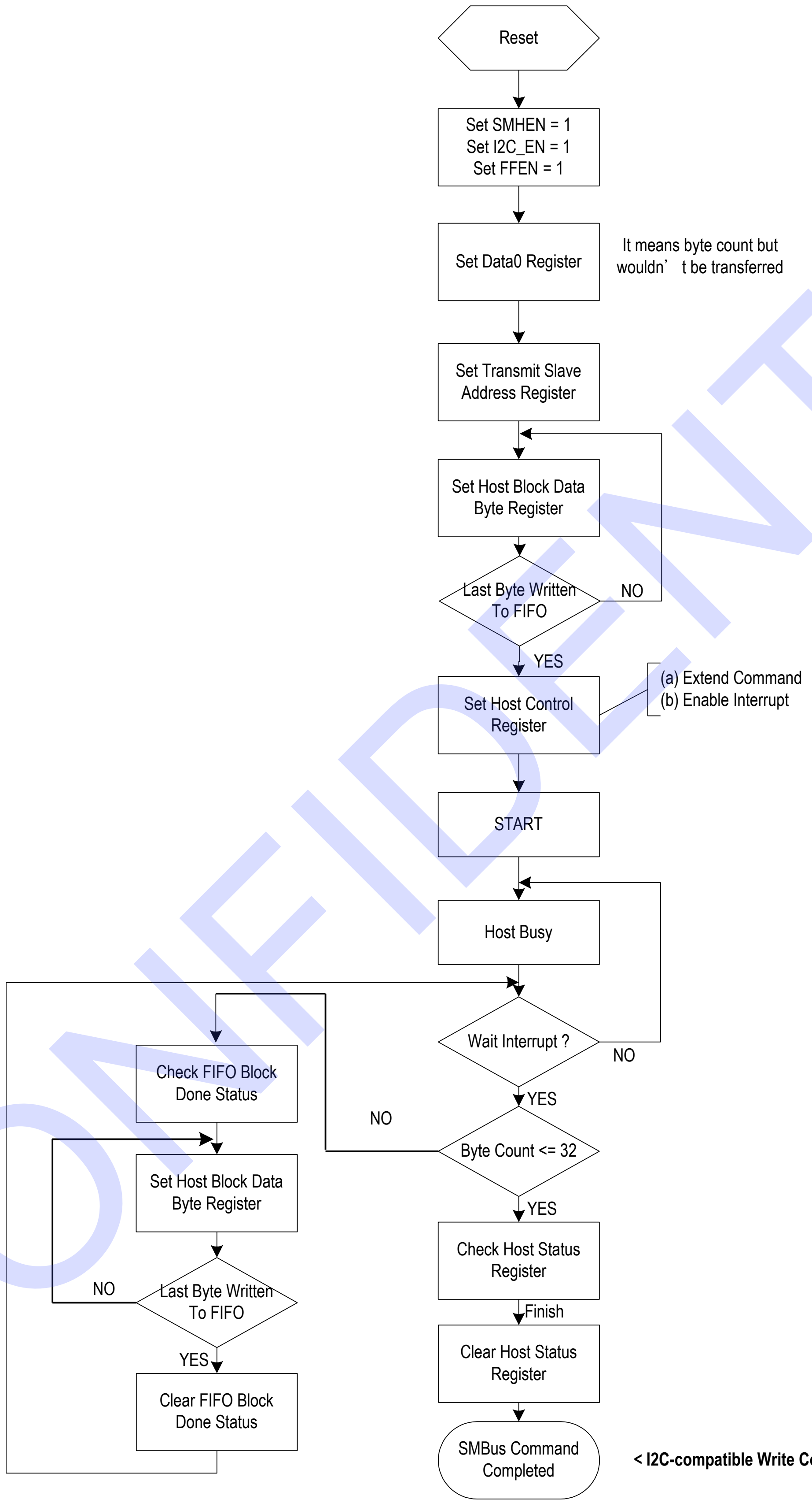
< I2C-compatible Read to Write Command >



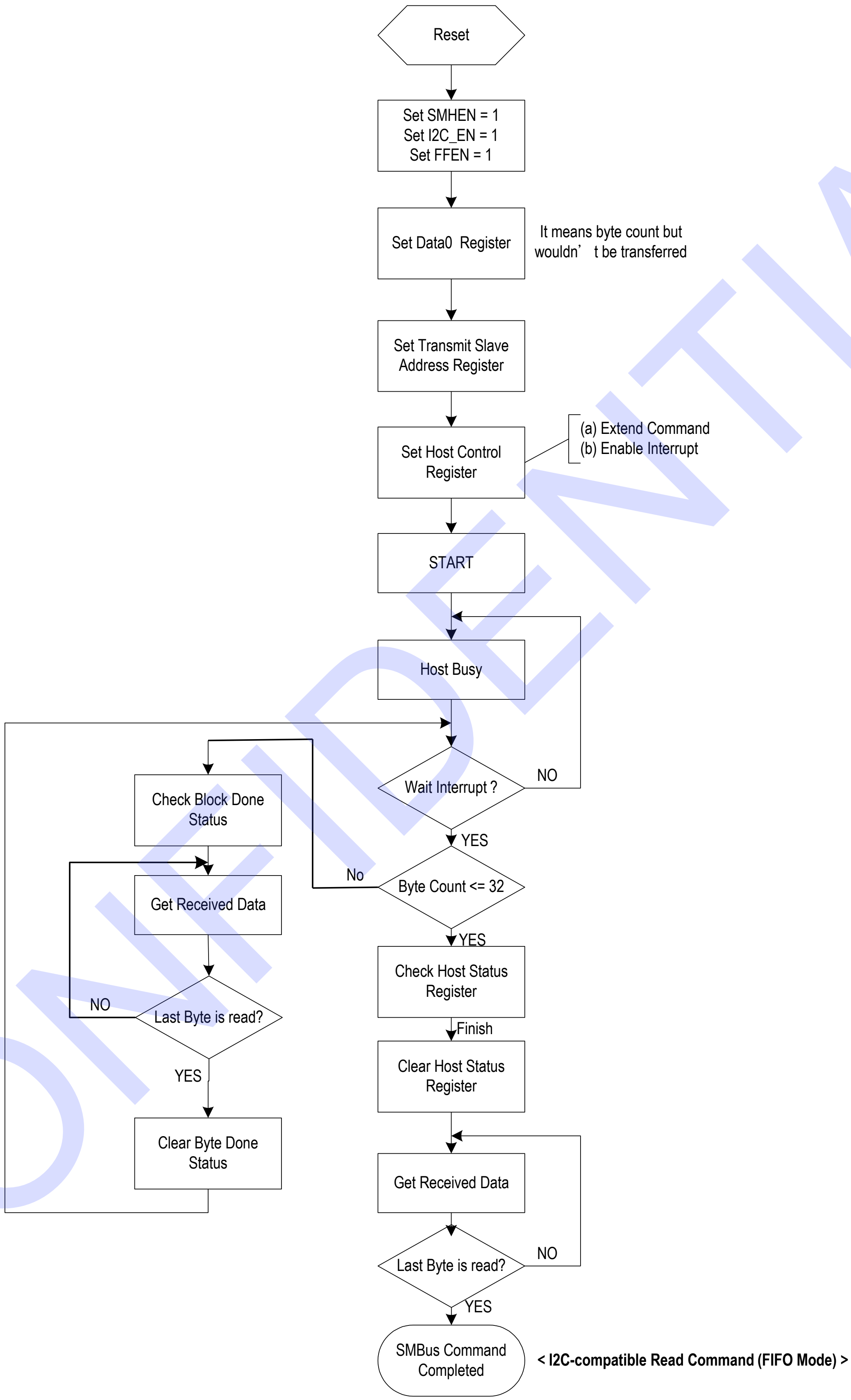
< Block Write Command (FIFO mode) >



< Block Read Command (FIFO mode) >



< I2C-compatible Write Command (FIFO Mode) >



< I2C-compatible Read Command (FIFO Mode) >

7.8.3.5 Description of SMCLK and SMDAT Line Control in Software Mode

(1) Control the SMCLK and SMDAT line by setting SCLCTL bit, SDACTLE bit, and SDACTL bit in SMBus Pin Control register (a.k.a., in software mode).
(2) When the SMCLK and SMDAT line are controlled in software mode, the hardware's SMBus logic will be reset, so the hardware will release the SMCLK and SMDAT line.
(3) The hardware's mechanism of 25 ms time-out will not work in software mode.

Note: It is recommended that SMCLK and SMDAT line should not be controlled in software mode and hardware mode simultaneously.

7.8.3.6 Description of SMBus Master and Slave Interface Select

The interface of the SMBus master and slave can be switched from SMCLK0/SMDAT0 to SMCLK5/SMDAT5 by setting the SMB01CHS, SMB23CHS and SMB45CHS registers.

Note: Switching the interfaces of the channels to the same interface is invalid.

7.8.3.7 Expression of SMBus Interrupt Events

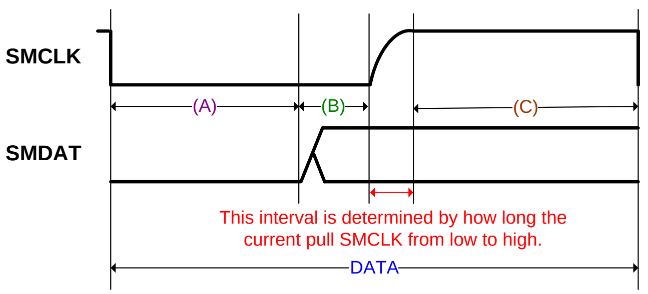
Table 7-11. SMBus Interrupt Events Expression

SMBus Interrupt Events	Interrupt Register	Description	
SMBus A Interrupt (Master)	b4@1C0Dh[MSTFCTRL1] & b0@1C41h[HOCTL]	Block Done Status 1	
	b7@1C40h[HOSTA] & b0@1C41h[HOCTL]	Byte Done Status	
	b6@1C40h[HOSTA] & b0@1C41h[HOCTL]	Time-out Error	
	b5@1C40h[HOSTA] & b0@1C41h[HOCTL]	Not Response ACK	
	b4@1C40h[HOSTA] & b0@1C41h[HOCTL]	Fail	
	b3@1C40h[HOSTA] & b0@1C41h[HOCTL]	Bus Error	
	b2@1C40h[HOSTA] & b0@1C41h[HOCTL]	Device Error	
	b1@1C40h[HOSTA] & b0@1C41h[HOCTL]	Finish Interrupt	
	b0@1C4Bh[SLSTA] & b0@1C4Ch[SICR]	Host Notify Status	
	b7@1C16h[MFTISTA]	Master A Rx Interrupt Detected (for FIFO threshold)	
	b3@1C16h[MFTISTA]	Master A Tx Interrupt Detected (for FIFO threshold)	
	b0@1C13h[IWRFISTA] & b0@1C12h[I2CW2RF]	Master A I2C FIFO Interrupt Detected	
SMBus A Interrupt (Slave)	b1@1C4Bh[SLSTA] & b5@1C50h[HOCTL2] & b1@1C4Ch[SICR]	Slave Data Status	
	b2@1C4Bh[SLSTA] & b5@1C50h[HOCTL2] & b1@1C4Ch[SICR]	Slave Timeout Status	
	b5@1C4Bh[SLSTA] & b3@1C4Ch[SICR] & b5@1C50h[HOCTL2] & b1@1C4Ch[SICR]	Stop Condition Detect Status	
	b1@1C19h[SFTISTA] & b1@1C18h[SFTHEN] & b5@1C50h[HOCTL2] & b1@1C4Ch[SICR]	Rx Interrupt Detected for Slave A (for FIFO threshold)	
	b0@1C19h[SFTISTA] & b0@1C18h[SFTHEN] & b5@1C50h[HOCTL2] & b1@1C4Ch[SICR]	Tx Interrupt Detected for Slave A (for FIFO threshold)	

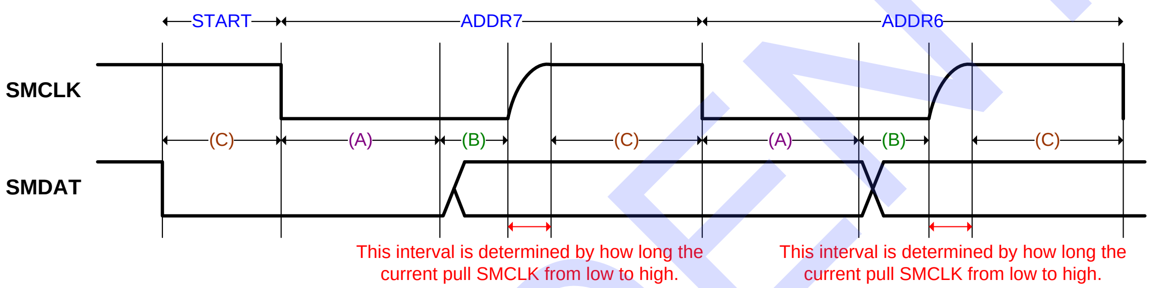
SMBus Interrupt Events	Interrupt Register	Description	
SMBus B Interrupt (Master)	b4@1C0Fh[MSTFCTRL2] & b0@1C81h[HOCTL] & (b1-0@1C0Fh[MSTFCTRL2] = 00b)	Block Done Status 2	
	b7@1C80h[HOSTA] & b0@1C81h[HOCTL]	Byte Done Status	
	b6@1C80h[HOSTA] & b0@1C81h[HOCTL]	Time-out Error	
	b5@1C80h[HOSTA] & b0@1C81h[HOCTL]	Not Response ACK	
	b4@1C80h[HOSTA] & b0@1C18h[HOCTL]	Fail	
	b3@1C80h[HOSTA] & b0@1C81h[HOCTL]	Bus Error	
	b2@1C80h[HOSTA] & b0@1C81h[HOCTL]	Device Error	
	b1@1C80h[HOSTA] & b0@1C81h[HOCTL]	Finish Interrupt	
	b0@1C8Bh[HOCTL] & b0@1C8Ch[HOCTL]	Host Notify Status	
	b6@1C16h[MFTISTA]	Master B Rx Interrupt Detected (for FIFO threshold)	
	b2@1C16h[MFTISTA]	Master B Tx Interrupt Detected (for FIFO threshold)	
	b1@1C13h[IWRFISTA] & b1@1C12h[I2CW2RF]	Master B I2C FIFO Interrupt Detected	
SMBus B Interrupt (Slave)	b1@1C8Bh[SLSTA] & b5@1C90h[HOCTL2] & b1@1C8Ch[SICR]	Slave Data Status	
	b2@1C8B h[SLSTA] & b5@1C90h[HOCTL2] & b1@1C8C h[SICR]	Slave Timeout Status	
	b5@1C8Bh[SLSTA] & b3@1C8Ch[SICR] & b5@1C90h[HOCTL2] & b1@1C8Ch[SICR]	Stop Condition Detect Status	
SMBus C Interrupt (Master)	b4@1C0Fh[MSTFCTRL2] & b0@1CC1h[HOCTL] & (b1-0@1C0Fh[MSTFCTRL2] = 01b)	Block Done Status 2	
	b7@1CC0h[HOSTA] & b0@1CC1h[HOCTL]	Byte Done Status	
	b6@1CC0h[HOSTA] & b0@1CC1h[HOCTL]	Time-out Error	
	b5@1CC0h[HOSTA] & b0@1CC1h[HOCTL]	Not Response ACK	
	b4@1CC0h[HOSTA] & b0@1CC1h[HOCTL]	Fail	
	b3@1CC0h[HOSTA] & b0@1CC1h[HOCTL]	Bus Error	
	b2@1CC0h[HOSTA] & b0@1CC1h[HOCTL]	Device Error	
	b1@1CC0h[HOSTA] & b0@1CC1h[HOCTL]	Finish Interrupt	
	b5@1C16h[MFTISTA]	Master C Rx Interrupt Detected (for FIFO threshold)	
	b1@1C16h[MFTISTA]	Master C Tx Interrupt Detected (for FIFO threshold)	
	b2@1C13h[IWRFISTA] & b2@1C12h[I2CW2RF]	Master C I2C FIFO Interrupt Detected	

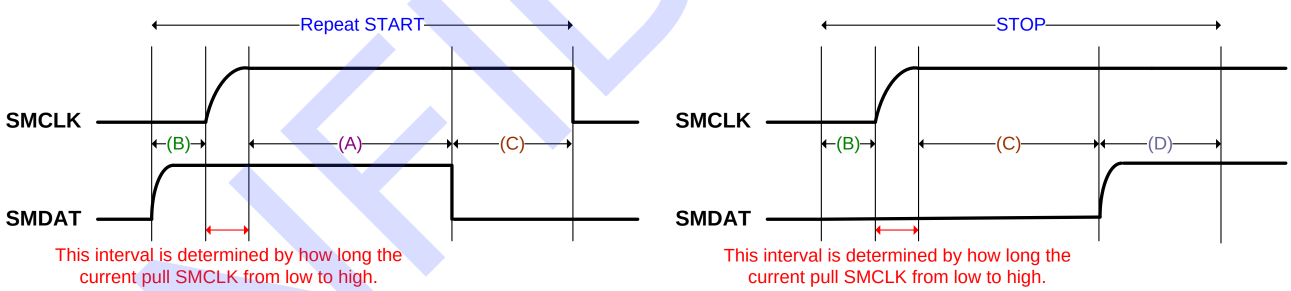
7.8.3.8 SMBus Waveform

Figure 7-11. SMBus Waveform versus SMBus Timing Registers



(A): ~=(VALUE_OF_4P7USREG / Freq_EC)
(B): ~=(VALUE_OF_250NSREG / Freq_EC)
(C): ~=(VALUE_OF_4P0USREG / Freq_EC)
(D): ~=(VALUE_OF_300NSREG / Freq_EC)
where VALUE_OF_4P7USREG consists of 4P7USH and 4P7USL.
VALUE_OF_4P0USREG consists of 4P0USH and 4P0USL.





Suggested setting of each register:

EC_Clk = 8M	Offset	1M	400K	100K	50K
4.7 µs Low Register (4P7USL)	00h	x	04h	22h	49h
4.0 µs Low Register (4P0USL)	01h	x	02h	1fh	42h
300 ns Register (300NS)	02h	x	01h	02h	05h
250 ns Register (250NS)	03h	x	01h	02h	05h
25 ms Register (25MS)	04h	19h			
45.3 µs Low Register (45P3USL)	05h	6ah			
45.3 µs High Register (45P3USH)	06h	01h			
4.7 µs and 4.0 µs High Register (4P7A4P0H)	07h	00h			

EC_Clk = 8M	Offset	1M	400K	100K	50K
SMCLK Timing Setting Register A	09h	04h	00h		
SMCLK Timing Setting Register B	0Ah	04h	00h		
SMCLK Timing Setting Register C	0Bh	04h	00h		

7.8.4 EC Interface Registers

The SMBus I/O registers are listed below. The base address for SMBus is 1C00h.
A, B, C are for channel A, B, C respectively.

Table 7-12. EC View Register Map, SMBus

7 0	Offset
Host Status (HOSTA)(A,B,C)	40h, 80h, C0h
Host Control (HOCTL)(A,B,C)	41h, 81h, C1h
Host Command (HOCMD)(A,B,C)	42h, 82h, C2h
Transmit Slave Address (TRASLA)(A,B,C)	43h, 83h, C3h
Host Data 0 (D0REG)(A,B,C)	44h, 84h, C4h
Host Data 1 (D1REG)(A,B,C)	45h, 85h, C5h
Host Block Data Byte (HOBDB)(A,B,C)	46h, 86h, C6h
Packet Error Check (PECERC)(A,B,C)	47h, 87h, C7h
Receive Slave Address (RESLADR) (A) (B)	48h, 88h
Receive Slave Address 2 (RESLADR2) (A) (B)	51h, 91h
Slave Data (SLDA) (A) (B)	49h, 89h
SMBus Pin Control (SMBPCTL)(A,B,C)	4Ah, 8Ah, CAh
Slave Status (SLSTA) (A) (B)	4Bh, 8Bh
Slave Interrupt Control (SICR) (A) (B)	4Ch, 8Ch
Notify Device Address (NDADR) (A) (B)	4Dh, 8Dh
Notify Data Low Byte (NDLB) (A) (B)	4Eh, 8Eh
Notify Data High Byte (NDHB) (A) (B)	4Fh, 8Fh
Host Control2 (HOCTL2)(A,B,C)	50h, 90h, D0h
4.7 μs Low Register (4P7USL)	00h
4.0 μs Low Register (4P0USL)	01h
300 ns Register (300NS)	02h
250 ns Register (250NS)	03h
25 ms Register (25MS)	04h
45.3 μs Low Register (45P3USL)	05h
45.3 μs High Register (45P3USH)	06h
4.7 μs and 4.0 μs High Register (4P7A4P0H)	07h
Slave Interface Select Register (SLVISEL)	08h
SMCLK Timing Setting Register A (SCLKTS_A)	09h
SMCLK Timing Setting Register B (SCLKTS_B)	0Ah
SMCLK Timing Setting Register C (SCLKTS_C)	0Bh
SMBus FIFO Control 1 Register (MSTFCTRL1)	0Dh
SMBus FIFO Status 1 Register (MSTFSTS1)	0Eh
SMBus FIFO Control 2 Register (MSTFCTRL2)	0Fh
SMBus FIFO Status 2 Register (MSTFSTS2)	10h
HOST Nack Source (HONACKSRC) (A,B,C)	54h, 94h, D4h
I2C Wr To Rd FIFO Register (I2CW2RF)	12h
I2C Wr To Rd FIFO Interrupt Status (IWRFISTA)	13h
Master FIFO Threshold (MSTFTH)	14h
Master FIFO Threshold Enable (MFTHEN)	15h
Master FIFO Threshold Interrupt Status (MFTISTA)	16h
Slave A FIFO Threshold (SLVFTH)	17h
Slave A FIFO Threshold Enable (SFTHEN)	18h

7	0	Offset
Slave A FIFO Threshold Interrupt Status (SFTISTA)		19h
Slave A FIFO Control Register (SFFCTL) (A)		55h
Slave A FIFO Status (SFFSTA) (A)		56h
Bridge Timeout (A,C)		2Fh
SMB0/1 Channel Select Register (SMB01CHS)		20h
SMB2/3 Channel Select Register (SMB23CHS)		21h
SMB4/5 Channel Select Register (SMB45CHS)		11h

7.8.4.1 Host Status Register (HOSTA)

All status bits are set by hardware and cleared by writing a one to the particular bit position by the software. Software can read this register to know the source of the interrupt (Master Interface).

Address Offset: Channel A: 40h
Channel B: 80h
Channel C: C0h

	R/W	Default	Description
7	R/WC	0b	**Byte Done Status (BDS)** This bit will be set to 1 when the host controller has received a byte (for Block Read commands and I2C-compatible cycles) or if it has completed the transmission of a byte (for Block Write commands and I2C-compatible cycles).
6	R/WC	0b	**Time-out Error (TMOE)** 0: This bit is cleared by writing a 1 to its position. 1: This bit is set when 25ms time-out error occurs.
5	R/WC	0b	**Not Response ACK (NACK)** 0: This bit is cleared by writing a 1 to its position. 1: This bit is set when the device does not respond ACK.
4	R/WC	0b	**Fail (FAIL)** 0: This bit is cleared by writing a 1 to the bit position. 1: Reading this bit will return 1 if KILL is set and a processing transmission is successfully killed.
3	R/WC	0b	**Bus Error (BSER)** 0: This bit is cleared by writing a 1 to the bit position. 1: The source of the interrupt is that the SMBus has lost arbitration.
2	R/WC	0b	**Device Error (DVER)** 0: This bit is cleared by writing a 1 to this bit's position. 1: This bit is set in one of the following conditions: (1) 25ms Time-out Error. (2) Not response ACK.
1	R/WC	0b	**Finish Interrupt (FINTR)** This bit will be set by termination of a command. 0: This bit is cleared by writing 1 to this position. 1: The source of the interrupt is the stop condition detected.
0	R	0b	**Host Busy (HOBY)** 0: This bit is cleared when the current transaction is completed. 1: This bit is set while the command is in operation.

7.8.4.2 Host Control Register (HOCTL)

Address Offset: **Channel A: 41h**
Channel B: 81h
Channel C: C1h

	R/W	Default	Description
7	R/W	0b	**PEC Enable (PEC_EN)** 0: The transaction without the PEC (Packet Error Checking) phase0 appended 1: The transaction with the PEC phase appended.
6	W	0b	**Start (SRT)** 0: This bit will always return 0 on reads. 1: When this bit is set, the SMBus host controller will perform the requested transaction.
5	W	0b	**Last Byte (LABY)** This bit is used for Block Read command and I2C-compatible read cycle. Read returns 1 if the next byte is the last byte to be received for the block read command and I2C-compatible read cycle. The firmware shall write 1 to this bit when the next byte will be the last byte to be received for the block read command and I2C-compatible cycle.
4-2	R/W	000b	**SMBus Command (SMCD)** These bits indicate which command will be performed. Bit 0 of the Transmit Slave Address Register determines if this is a read or write command. 000:Quick Command 001:Send Byte/ Receive Byte 010:Write Byte/ Read Byte 011:Write Word/ Read Word 100:Process Call 101:Block Read/ Block Write 110:I2C Block Read 111:Extend Command
1	R/W	0b	**Kill (KILL)** 0: Normal SMBus Host controller functionality. 1: When this bit is set, kill the current host transaction. This bit, once set, has to be cleared by software to allow the SMBus Host controller to function normally.
0	R/W	0b	**Host Interrupt Enable (INTREN)** 0: Disable 1: Enable the generation of an interrupt for the master interface

7.8.4.3 Host Command Register (HOCMD)

Address Offset: **Channel A: 42h**
Channel B: 82h
Channel C: C2h

	R/W	Default	Description
7-0	R/W	00h	**Host Command Register (HCREG)** These bits are transmitted in the command field of the SMBus protocol.

7.8.4.4 Transmit Slave Address Register (TRASLA)

Address Offset: **Channel A: 43h**
Channel B: 83h
Channel C: C3h

	R/W	Default	Description
7-1	R/W	00h	**Address (ADR)** Address of the targeted slave.
0	R/W	0b	**Direction (DIR)** Direction of the host transfer. 0: Write 1: Read

7.8.4.5 Data 0 Register (D0REG)

Address Offset: **Channel A: 44h**
Channel B: 84h
Channel C: C4h

	R/W	Default	Description
7-0	R/W	00h	**Data 0 (D0)** These bits contain the data sent in the DATA0 (The first transaction date byte) field of the SMBus protocol. For block write commands, this register reflects the number (from 1 to 32) of bytes to transfer.

7.8.4.6 Data 1 Register (D1REG)

Address Offset: **Channel A: 45h**
Channel B: 85h
Channel C: C5h

	R/W	Default	Description
7-0	R/W	00h	**Data 1 (D1)** These bits contain the data sent in the DATA1 (Data Byte High) field of the SMBus protocol.

7.8.4.7 Host Block Data Byte Register (HOBDB)

Address Offset: **Channel A: 46h**
Channel B: 86h
Channel C: C6h

	R/W	Default	Description
7-0	R/W	00h	**Block Data (BLDT)** For a block write command, data is sent from this register. On block read command, the received data is stored in this register.

7.8.4.8 Packet Error Check Register (PECERC)

Address Offset: **Channel A: 47h**
Channel B: 87h
Channel C: C7h

	R/W	Default	Description

	R/W	Default	Description
7-0	R/W	00h	**PEC Data (PECD)** These bits are written with the 8-bit CRC value that is used as the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software.

7.8.4.9 Receive Slave Address Register (RESLADR)

Address Offset: 48h (Only for Channel A)
88h (Only for Channel B)

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6-0	R/W	00h	**Slave Address (SADR)** These bits are the slave address decoded for read and write cycles.

7.8.4.10 Receive Slave Address Register 2 (RESLADR2)

Address Offset: 51h (Only for Channel A)
91h (Only for Channel B)

Bit	R/W	Default	Description
7	R/W	0b	**Slave Address 2 Enable** 0: SADR2 field is ignored. 1: SADR2 field holds a valid address and enables the function to decode SADR2 for comparison with the received address.
6-0	R/W	00h	**Slave Address 2 (SADR2)** These bits are the slave address 2 decoded for read and write cycles.

7.8.4.11 Slave Data Register (SLDA)

Address Offset: 49h (Only for Channel A)
89h (Only for Channel B)

Bit	R/W	Default	Description
7-0	R/W	00h	**Slave Data Byte0 (SDB0)** This register stores the data received from the external master. When this register is served, software must write/read data stored in this register twice to release the SCL line. (See also section 7.8.3.3 SMBus Porting Guide on page 275)

7.8.4.12 SMBus Pin Control Register (SMBPCTL)

Address Offset: Channel A: 4Ah
Channel B: 8Ah
Channel C: CAh

	R/W	Default	Description
7-5	-	0h	**Reserved**
4	W	0b	**SMDAT Control Enable (SDACTLE)** This bit is used to enable the SMDAT Control (SDACTL) bit setting. It is write-only, and always returns 0 on reads.

	R/W	Default	Description
3	R/W	1b	**SMDAT Control (SDACTL)** Only when the SMDAT Control Enable (SDACTLE) bit is set to 1 to 1 at the same time, this bit can be written as the following: 0: The SMDAT0/1/2 pin will be driven low regardless of the other SMBus logic. 1: The SMDAT0/1/2 pin will not be driven low. The other SMBus logic controls this pin.
2	R/W	1b	**SMCLK Control (SCLCTL)** 0: The SMCLK0/1/2 pin will be driven low regardless of the other SMBus logic. 1: The SMCLK0/1/2 pin will not be driven low. The other SMBus logic controls this pin.
1	R	-	**SMDAT Current State (SMBDCS)** This bit returns the value of the SMDAT0/1/2 pin. 0: Low 1: High
0	R	-	**SMCLK Current State (SMBCS)** This bit returns the value of the SMCLK0/1/2 pin. 0: Low 1: High

7.8.4.13 Slave Status Register (SLSTA)

Software can read this register to know the source of the interrupt (Slave Interface).

Address Offset: 4Bh (Only for Channel A)
8Bh (Only for Channel B)

Bit	R/W	Default	Description
7	R/WC	0b	Slave Stretch SMBCLK Low Status (SSSLS) 1: SMB Slave A is stretching SMBCLK low. 0: This bit will be auto-cleared if SSCL bit is disabled. Refer to the above, if offset is 8Bh, Slave A is replaced with Slave B.
6	-	1b	**Reserved**
5	R/WC	0b	**Stop Condition Detect Status (SPDS)** 0: Cleared by writing a 1 to this bit. 1: Indicate Stop Condition detected.
4	R	0b	**Match Slave Address 2 (MSLA2)** 0: The received address matches SADR. 1: The received address matches SADR2. Don't care when Host notifies command.
3	R	0b	**Read Cycle Status (RCS)** Direction of the slave transfer. 0: Write. 1: Read.
2	R/WC	0b	**Slave Timeout Status (STS)** 0: Cleared by writing a 1 to this bit. 1: Timeout status occurs.

Bit	R/W	Default	Description
1	R/WC	0b	**Slave Data Status (SDS)** 0: Cleared by writing a 1 to this bit. 1: Slave Data Register is waiting for read or write. When this bit is set and the Read Cycle Status (RCS) bit is low, the software shall read the data from the slave Data Register. When this bit is set and the Read Cycle Status (RCS) bit is high, the software shall write the data to the slave Data Register.
0	R/WC	0b	**Host Notify Status (HONOST)** This bit will be set to a 1 when a Host Notify Command has been completely received. Software can read this bit to determine that the source of the interrupt is the reception of the Host Notify Command.

7.8.4.14 Slave Interrupt Control Register (SICR)

Address Offset: 4Ch (Only for Channel A)
8Ch (Only for Channel B)

Bit	R/W	Default	Description
7-4	-	00h	**Reserved**
3	R/W	0b	**Slave Detect STOP Condition Interrupt Enable (SDSEN)** 0: Disable 1: Enable the generation of an interrupt for STOP detected by slave
2	R/W	0b	**Slave SMDAT Low Timeout Enable (SDLTOEN)** This bit controls the reset mechanism of SMBus Slave to handle the SMDAT line low if 25ms timeout. 0: SMCLK will be released if timeout. 1: SMCLK/SMDAT will be released if timeout.
1	R/W	0b	**Slave Interrupt Enable (SITEN)** 0: Disable 1: Enable the generation of an interrupt for the slave interface.
0	R/W	0b	**Host Notify Interrupt Enable (HONOIN)** 0: Disable 1: Enable the generation of an interrupt when Host Notify Status is set and it dose not affect the setting of the Host Notify Status bit.

7.8.4.15 Notify Device Address Register (NDADR)

Address Offset: 4Dh (Only for Channel A)
8Dh (Only for Channel B)

Bit	R/W	Default	Description
7-1	R	00h	**Device Address (DVADR)** These bits contain the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 Specification.
0	-	0b	**Reserved**

7.8.4.16 Notify Data Low Byte Register (NDLB)

Address Offset: 4Eh (Only for Channel A)
8Eh (Only for Channel B)

Bit	R/W	Default	Description
7-0	R	00h	**Data Low Byte (DALB)** These bits contain the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 Specification.

7.8.4.17 Notify Data High Byte Register (NDHB)

Address Offset: 4Fh (Only for Channel A)
8Fh (Only for Channel B)

Bit	R/W	Default	Description
7-0	R	00h	**Data High Byte (DAHB)** These bits contain the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 Specification.

7.8.4.18 Host Control Register 2 (HOCTL2)

Address Offset: Channel A: 50h
Channel B: 90h
Channel C: D0h

Bit	R/W	Default	Description
7	W	0b	**Slave Stretch Clock Low (SSCL)** 1: Enable "SMBus slave hold clock after the start bit received". 0: Disable "SMBus slave hold clock after the start bit received". Only for 50h and 90h (Slave A and Slave B)
6	-	0h	**Reserved**
5	W	0b	**SMBus Slave Enable (SLVEN)** 0: Disable the SMBus Slave Device. 1: Enable the SMBus Slave Device. The SMBus Host Controller is disabled when this bit is set. This bit only exists in address offset 50h and 90h.
4	R/W	0b	**SMDAT Timeout Enable (SMD_TO_EN)** This bit controls the reset mechanism of SMBus Master to handle the SMDAT line low if 25ms timeout. 0: SMCLK will be released if timeout. 1: SMCLK/SMDAT will be released if timeout.
3	R/W	0b	**I2C Switch Direction Enable (I2C_SW_EN)** 0: Disable I2C Switch Direction. 1: Enable I2C Switch Direction.
2	R/W	0b	**I2C Switch Direction Wait (I2C_SW_WAIT)** 0: Disable I2C Switch Direction Wait. 1: Enable I2C Switch Direction Wait.
1	R/W	0b	**I2C Enable (I2C_EN)** 0: SMBus behavior. 1: Enable to communicate with I2C device and support I2C-compatible cycles. When this bit is set, the SMBus logic will instead be set to communicate with I2C devices and support I2C-compatible cycles. This forces the following changes: (1) The Process Call command will skip the Command code. (2) The Block Write command will skip sending the Byte Count. (3) The Extend command can be used to support I2C-compatible cycles.
0	R/W	0b	**SMBus Host Enable (SMHEN)** 0: Disable the SMBus Host Controller. 1: The SMBus Host interface is enabled to execute commands.

7.8.4.19 Slave Interface Select Register (SLVISELR)

Address Offset: 08h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0b	**Override Debug Mode through SMBus (OVRSMDBG)** This bit overrides Debug Mode function enabled by hardware strap in SMBus interface and disables it.
3-0	-	-	**Reserved**

7.8.4.20 4.7 µs Low Register (4P7USL)

The following registers (00h-07h) define the SMCLK0/1/2 and SMDAT0/1/2 timing.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**4.7 µs Low Register (4P7USL)** This 4.7 µs Low Register and 4.7 µs high bit (in the 4.7 µs and 4.0 µs High Register) define the count number for the 4.7 µs counter. The 4.7 µs is (count number / FreqEC). (FreqEC is listed in **Table 10-2** on page 570)

7.8.4.21 4.0 µs Low Register (4P0USL)

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**4.0 µs Low Register (4P0USL)** This 4.0 µs Low Register and 4.0 µs high bit (in the 4.7 µs and 4.0 µs High Register) define the count number for the 4.0 µs counter. The 4.0 µs is (count number / FreqEC). (FreqEC is listed in **Table 10-2** on page 570)

7.8.4.22 300 ns Register (300NSREG)

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	00h	**300ns Register (300NS)** This field defines the SMDAT0/1/2 hold time. This byte is the count number of the counter for 300 ns. The 300 ns is calculated by (count number / FreqEC). (FreqEC is listed in Table 10-2 on page 570)

7.8.4.23 250 ns Register (250NSREG)

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	00h	**250ns Register (250NS)** This field defines the SMDAT0/1/2 setup time. This byte is the count number of the counter for 250 ns. The 250 ns is calculated by (count number / FreqEC). (FreqEC is listed in Table 10-2 on page 570)

7.8.4.24 25 ms Register (25MSREG)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	00h	**25 ms Register (25MS)** This field defines the SMCLK0/1/2 clock low timeout. This byte is the count number of the counter for 25 ms. The 25 ms is calculated by (count number *1.024 kHz).

7.8.4.25 45.3 µs Low Register (45P3USLREG)

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/W	00h	**45.3 µs Low Register (45P3USLOW)** This 45.3 µs Low Register, 45.3 µs High Register, 4.7us Low Register and 4.7us high bit (in the 4.7µs And 4.0 µs High Register) define the SMCLK0/1/2 high periodic (maximal). (45.3µs + 4.7µs=50µs) This byte is the count number bits [7:0] of the counter for 45.3 µs. The 45.3 µs is calculated by (count number[15:0] / FreqEC). (FreqEC is listed in Table 10-2 on page 570)

7.8.4.26 45.3 µs High Register (45P3USHREG)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	00h	**45.3 µs High Register (45P3USHGH)** This 45.3 µs Low Register, 45.3 µs High Register, 4.7us Low Register and 4.7us high bit (in the 4.7µs And 4.0 µs High Register) define the SMCLK0/1/2 high periodic (maximal). (45.3 µs + 4.7µs=50µs). This byte is the count number bits [15:8] of the counter for 45.3 µs. The 45.3 µs is calculated by (count number[15:0] / FreqEC). (FreqEC is listed in Table 10-2 on page 570)

7.8.4.27 4.7 µs And 4.0 µs High Register (4p7A4P0H)

Address Offset: 07h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	0b	**4.0 µs High Bit (4P0USH)** This bit is bit 8 of the count number for the 4.0 µs counter. This 4.0 µs Low Register and 4.0µs High Bit define the count number for the 4.0 µs counter.
0	R/W	0b	**4.7 µs High Bit (4P7USH)** This bit is bit 8 of the count number for the 4.7 µs counter. This 4.7 µs Low Register and 4.7µs High Bit define the count number for the 4.7 µs counter.

7.8.4.28 SMCLK Timing Setting Register A (SCLKTS_A)

Address Offset: 09h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**

Bit	R/W	Default	Description
4	R/W	0b	**Fix Repeat Start Setup Time (FRSST)** 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 2us. Please refer to Figure 7-11 on page 278 for Repeat Start period (A).
3	-	-	**Reserved**
2	R/W	1b	**Master AOperate In 1M** 0: Disable 1: Master A is able to operate at 1M
1-0	R/W	00b	**SMCLK Setting (SCLKS)** These bits are to determine which SMCLK rate is for channel A. If this these bits are disabled, the SMCLK rate depends on the setting of original timing registers. 00b: Disable 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

7.8.4.29 SMCLK Timing Setting Register B (SCLKTS_B)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Fix Repeat Start Setup Time (FRSST)** 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 2us. Please refer to Figure 7-11 on page 278 for Repeat Start period (A).
3	-	-	**Reserved**
2	R/W	0b	**Master B Operate In 1M** 0: Disable 1: Master B is able to operate at 1M
1-0	R/W	00b	**SMCLK Setting (SCLKS)** These bits are to determine which SMCLK rate is for channel B. If these bits are disabled, the SMCLK rate depends on the setting of original timing registers. 00b: Disable 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

7.8.4.30 SMCLK Timing Setting Register C (SCLKTS_C)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Fix Repeat Start Setup Time (FRSST)** 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 2us. Please refer to Figure 7-11 on page 278 for Repeat Start period (A).
3	-	-	**Reserved**

Bit	R/W	Default	Description
2	R/W	0b	**Master C Operate In 1M** 0: Disable 1: Master B is able to operate at 1M.
1-0	R/W	00b	**SMCLK Setting (SCLKS)** These bits are to determine which SMCLK rate is for channel C. If these bits are disabled, the SMCLK rate depends on the setting of original timing registers. 00b: Disable 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

7.8.4.31 SMBus FIFO Control 1 Register (MSTFCTRL1)

Address Offset: 0Dh

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/WC	0b	**Block Done Status 1 (BLKDS1)** This bit will be set to 1 when the host controller has received or transmitted one block of 32 bytes while the byte count is set larger than 32 for I2C-compatible FIFO Mode cycles. Write to clear, then HW automatically do the successive read/write cycle. (This is for channel a dedicated FIFO)
3	R/W	0b	**FIFO 1 Enable (FF1EN)** 0: Disable SMB channel A in FIFO Mode. 1: Enable SMB channel A in FIFO Mode. (This is for channel a dedicated FIFO)
2-0	R/W	000b	**Reserved**

7.8.4.32 SMBus FIFO Status 1 Register (MSTFSTS1)

Address Offset: 0Eh

Bit	R/W	Default	Description
7	R	-	**FIFO 1 Empty** (This is for channel a dedicated FIFO)
6	R	-	**FIFO 1 Full** (This is for channel a dedicated FIFO)
5-0	R	-	**FIFO 1 Byte Count** (This is for channel a dedicated FIFO)

7.8.4.33 SMBus FIFO Control 2 Register (MSTFCTRL2)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-5	-	-	**Reserved**

Bit	R/W	Default	Description
4	R/WC	0b	**Block Done Status 2 (BLKDS2)** This bit will be set to 1 when the host controller has received or transmitted one block of 32 bytes while the byte count is set larger than 32 for I2C-compatible FIFO Mode cycles. Write to clear, then HW automatically do the successive read/write cycle. (This is for the second FIFO, which can be used by channel b or channel c.)
3	R/W	0b	**FIFO 2 Enable (FFEN2)** 0: Disable FIFO 2. 1: Enable FIFO 2. (This is for the second FIFO, which can be used by channel b or channel c.)
2	-	-	**Reserved**
1-0	R/W	00b	**FIFO 2 Channel Select (FFCHSEL2)** 00b: Switch FIFO to Channel B. 01b: Switch FIFO to Channel C. 11b: no action

7.8.4.34 SMBus FIFO Status 2 Register (MSTFSTS2)

Address Offset: 10h

Bit	R/W	Default	Description
7	R	-	**FIFO 2 Empty** (This is for the second FIFO, which can be used by channel b or channel c.)
6	R	-	**FIFO 2 Full** (This is for the second FIFO, which can be used by channel b or channel c.)
5-0	R	-	**FIFO 2 Byte Count** (This is for the second FIFO, which can be used by channel b or channel c.)

7.8.4.35 HOST Nack Source (HONACKSRC)

Address Offset: Channel A: 54h
Channel B: 94h
Channel C: D4h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R/WC	00h	**HOST Nack Source** 000: no nack_error 001: slave address nack error 010: command nack erro 011: slave address read nack error 100: data low byte nack error (DL) 101: data high byte nack error (DH) 110: data nack error (for block write) 111: PEC nack error (Writing 111b can be cleard.)

7.8.4.36 HOST Nack Source (HONACKSRC)

Address Offset: Channel A: 54h
Channel B: 94h
Channel C: D4h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R/WC	00h	**HOST Nack Source** 000: no nack_error 001: slave address nack error 010: command nack erro 011: slave address read nack error 100: data low byte nack error (DL) 101: data high byte nack error (DH) 110: data nack error (for block write) 111: PEC nack error (Writing 111b can be cleard.)

7.8.4.37 I2C Wr To Rd FIFO Register (I2CW2RF)

Address Offset: 12h

Bit	R/W	Default	Description
7	R/W	0	**Master A I2C Wr->Rd FIFO Function (MAIF)** 1: Eenabled. 0: Disable
6	R/W	0	**Master BC I2C Wr->Rd FIFO Function (MBCIF)** 1: Enable 0: Disable
5-3	-	-	**Reserved**
2	R/W	0	**Master C I2C Wr->Rd FIFO Interrupt (MCIFI)** 1: Enable 0: Disable
1	R/W	0	**Master B I2C Wr->Rd FIFO Interrupt (MBIFI)** 1: Enable 0: Disable
0	R/W	0	**Master A I2C Wr->Rd FIFO Interrupt (MAIFI)** 1: Enable 0: Disable

7.8.4.38 I2C Wr To Rd FIFO Interrupt Status (IWRFISTA)

Address Offset: 13h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/WC	0	**Master C I2C FIFO Interrupt Detected (MCIFID)** 0: Cleared by writing a 1 to this bit. 1: I2C Wr->Rd FIFO Interrupt Detected for Master C
1	R/WC	0	**Master B I2C FIFO Interrupt Detected (MBIFID)** 0: Cleared by writing a 1 to this bit. 1: I2C Wr->Rd FIFO Interrupt Detected for Master B

Bit	R/W	Default	Description
0	R/WC	0	**Master A I2C FIFO Interrupt Detected (MAIFID)** 0: Cleared by writing a 1 to this bit. 1: I2C Wr->Rd FIFO Interrupt Detected for Master A

7.8.4.39 Master FIFO Threshold (MSTFTH)

Address Offset: 14h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	01h	**Master FIFO Threshold (MFTH)** 00: The threshold is 8 bytes. 01: The threshold is 16 bytes. 10: The threshold is 24 bytes.

7.8.4.40 Master FIFO Threshold Enable (MFTHEN)

Address Offset: 15h

Bit	R/W	Default	Description
7	R/W	0	**Master A Receive Data Available Function (MARDA)** 0: Disable 1: Enable
6	R/W	0	**Master B Receive Data Available Function (MBRDA)** 0: Disable 1: Enable
5	R/W	0	**Master C Receive Data Available Function (MCRDA)** 0: Disable 1: Enable
4	-	-	Reserved
3	R/W	0	**Master A Transmitter Data Available Function (MATDA)** 0: Disable 1: Enable
2	R/W	0	**Master B Transmitter Data Available Function (MBTDA)** 0: Disable 1: Enable
1	R/W	0	**Master C Transmitter Data Available Function (MCTDA)** 0: Disable 1: Enable
0	-	-	**Reserved**

7.8.4.41 Master FIFO Threshold Interrupt Status (MFTISTA)

Address Offset: 16h

Bit	R/W	Default	Description
7	R/WC	0	**Master A Rx Interrupt Detected (MARID)** 0: Cleared by writing a 1 to this bit. 1: Master A Receive Data Available Interrupt Detected
6	R/WC	0	**Master B Rx Interrupt Detected (MBRID)** 0: Cleared by writing a 1 to this bit. 1: Master B Receive Data Available Interrupt Detected

Bit	R/W	Default	Description
5	R/WC	0	**Master C Rx Interrupt Detected (MCRID)** 0: Cleared by writing a 1 to this bit. 1: Master C Receive Data Available Interrupt Detected
4	-	-	**Reserved**
3	R/WC	0	**Master A Tx Interrupt Detected (MATID)** 0: Cleared by writing a 1 to this bit. 1: Master A Transmitter Data Available Interrupt Detected
2	R/WC	0	**Master B Tx Interrupt Detected (MBTID)** 0: Cleared by writing a 1 to this bit. 1: Master B Transmitter Data Available Interrupt Detected
1	R/WC	0	**Master C Tx Interrupt Detected (MCTID)** 0: Cleared by writing a 1 to this bit. 1: Master C Transmitter Data Available Interrupt Detected
0	-	-	**Reserved**

7.8.4.42 Slave A FIFO Threshold (SLVFTH)

Address Offset: 17h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	01h	**Slave A FIFO Threshold (SFTH)** 00: The threshold is 4 bytes. 01: The threshold is 8 bytes. 10: The threshold is 12 bytes.

7.8.4.43 Slave A FIFO Threshold Enable (SFTHEN)

Address Offset: 18h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	0	**Receive Data Available Function (RDAF)** 0: Disable 1: Enable
0	R/W	0	**Transmitter Data Available Function (TDAF)** 0: Disable 1: Enable

7.8.4.44 Slave A FIFO Threshold Interrupt Status (SFTISTA)

Address Offset: 19h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/WC	0	**Rx Interrupt Detected for Slave A (RIDSA)** 0: Cleared by writing a 1 to this bit. 1: Receive data available interrupt detected for Slave A
0	R/WC	0	**Tx Interrupt Detected for Slave A (TXIDSA)** 0: Cleared by writing a 1 to this bit. 1: Transmitter data available interrupt detected for Slave A

7.8.4.45 Slave A FIFO Control Register (SFFCTL)

Address Offset: 55h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	1	**Hardware Slave A (For Pre-defined) Enable (HSAPE)** 1: Enable 0: Disable
0	R/W	0	**Slave A FIFO Enable (SAFE)** 1: Enable 0: Disable

7.8.4.46 Slave A FIFO Status (SFFSTA)

Address Offset: 56h

Bit	R/W	Default	Description
7	R	-	**FIFO Empty**
6	R	-	**FIFO Full**
5	-	-	**Reserved**
4-0	R	-	**FIFO Byte Count**

7.8.4.47 Bridge Timeout

Address Offset: 2fh

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0	**Bridge Master Timeout Enable**
4	R/W	0	**Bridge Slave Timeout Enable**
3-2	-	-	**Reserved**
1	R/WC	0	**Bridge Master Timeout**
0	R/WC	0	**Bridge Slave Timeout**

7.8.4.48 SMB0/1 Channel Select Register (SMB01CHS)

Address Offset: 20h

Bit	R/W	Default	Description
7-4	R/W	1h	**Channel Switch Select of SMB1 Pin** These bits are to decide which channel is switched to SMB1 pin. 000b: Channel A is located at SMCLK1/SMDAT1. 001b: Channel B is located at SMCLK1/SMDAT1. 010b: Channel C is located at SMCLK1/SMDAT1. 011b: Channel D is located at SMCLK1/SMDAT1. 100b: Channel E is located at SMCLK1/SMDAT1. 101b: Channel F is located at SMCLK1/SMDAT1.
3-0	R/W	0h	**Channel Switch Select of SMB0 Pin** These bits are to decide which channel is switched to SMB0 pin. 000b: Channel A is located at SMCLK0/SMDAT0. 001b: Channel B is located at SMCLK0/SMDAT0. 010b: Channel C is located at SMCLK0/SMDAT0. 011b: Channel D is located at SMCLK0/SMDAT0. 100b: Channel E is located at SMCLK0/SMDAT0. 101b: Channel F is located at SMCLK0/SMDAT0.

7.8.4.49 SMB2/3 Channel Select Register (SMB23CHS)

Address Offset: 21h

Bit	R/W	Default	Description
7-4	R/W	3h	**Channel Switch Select of SMB3 Pin** These bits are to decide which channel is switched to SMB3 pin. 000b: Channel A is located at SMCLK3/SMDAT3. 001b: Channel B is located at SMCLK3/SMDAT3. 010b: Channel C is located at SMCLK3/SMDAT3. 011b: Channel D is located at SMCLK3/SMDAT3. 100b: Channel E is located at SMCLK3/SMDAT3. 101b: Channel F is located at SMCLK3/SMDAT3.
3-0	R/W	2h	**Channel Switch Select of SMB2 Pin** These bits are to decide which channel is switched to SMB2 pin. 000b: Channel A is located at SMCLK2/SMDAT2. 001b: Channel B is located at SMCLK2/SMDAT2. 010b: Channel C is located at SMCLK2/SMDAT2. 011b: Channel D is located at SMCLK2/SMDAT2. 100b: Channel E is located at SMCLK2/SMDAT2. 101b: Channel F is located at SMCLK2/SMDAT2.

7.8.4.50 SMB4/5 Channel Select Register (SMB45CHS)

Address Offset: 11h

Bit	R/W	Default	Description
7-4	R/W	5h	**Channel Switch Select of SMB5 Pin** These bits are to decide which channel is switched to SMB5 pin. 000b: Channel A is located at SMCLK5/SMDAT5. 001b: Channel B is located at SMCLK5/SMDAT5. 010b: Channel C is located at SMCLK5/SMDAT5. 011b: Channel D is located at SMCLK5/SMDAT5. 100b: Channel E is located at SMCLK5/SMDAT5. 101b: Channel F is located at SMCLK5/SMDAT5.
3-0	R/W	4h	**Channel Switch Select of SMB4 Pin** These bits are to decide which channel is switched to SMB4 pin. 000b: Channel A is located at SMCLK4/SMDAT4. 001b: Channel B is located at SMCLK4/SMDAT4. 010b: Channel C is located at SMCLK4/SMDAT4. 011b: Channel D is located at SMCLK4/SMDAT4. 100b: Channel E is located at SMCLK4/SMDAT4. 101b: Channel F is located at SMCLK4/SMDAT4.

7.9 Enhanced SMBus/I2C Interface

7.9.1 Overview

The enhanced SMbus/ I2C channel D, E, and F are three controllers which are designed to support the I2C protocol, which is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices. Devices controlling the buses are called as master, which is responsible for generation of bus control and synchronizing signals. Slaves just follow the master. Any I2C device can be either receiver or transmitter. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

7.9.2 Features

I2C controller serves both as I2C compatible master and slave. It supports the following functionality:

- Supports three I2C channels.
- Both master and slave operation.
- Both interrupt and non-interrupt data transfers.
- Start/Stop/Repeated Start generation.
- Fully support arbitration process.
- Software programmable acknowledge bit.
- Software programmable time out feature.
- Programmable addresses register.
- Programmable SCL frequency.
- Soft reset of I2C Master/Slave.
- Programmable maximum SCL low period.
- Supports SMBUS burst read and write.
- Programmable Command Queue mode.
- Support fast plus I2C spec.
- Support four IDs in slave.
- Support four I2C devices in auto, interrupt enable and power saving mode.
- Support monitor mode.

7.9.3 Functional Description

7.9.3.1 Command Queue

7.9.3.1.1 Command Type

Commands have four types in this design module, and they are listed below:
(1). 'ID': Target slave address is send out by master transmitter.
(2). 'CMD_L': RS (Repeat Start) is the I2C Repeat Start condition,
R/W (Read/ Write) decides the I2C read or write direction,
P (STOP) is the I2C STOP condition,
E (End) is this device end flag,
LA (Last ACK) is Last ACK in master receiver,
and bit[2:0] are number of transfer out or receive data which depends on R/W.
(3). 'CMD_H': Number of transfer out or receive data
(4). 'WData': Data is send out by master transmitter.

Command Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
ID	ID[7:0]							
CMD_L	RS	R/W	P	E	LA	NUM[2:0]		
CMD_H	NUM[10:3]							
WData	WData[7:0]							

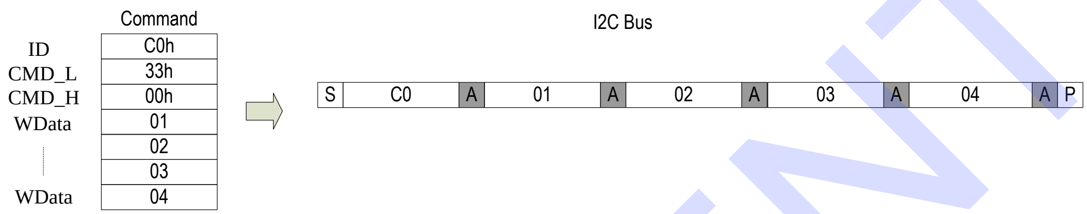
7.9.3.1.2 Using Guide

The first command always is ‘ID’, the second is ‘CMD_L ’, and then is ‘CMD_H’.

Single Transmitter

(1). Set target slave address in ‘ID’.
(2). Set ‘CMD_L’ and ‘CMD_H: RS sets low, R/W sets low for write direction, P sets high to stop the I2C after the I2C wdata transfer done, E sets high to finish this device commands because it is single transmitter, and then set number of write data.
(3). Set ‘WDatas’ for sending out.

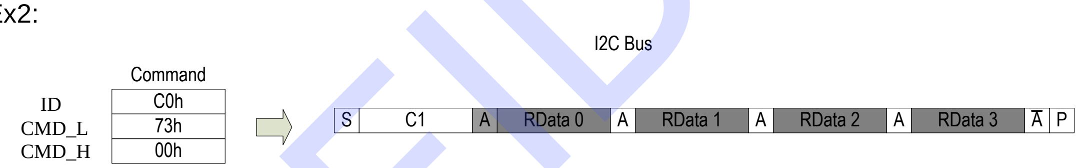
Ex1:



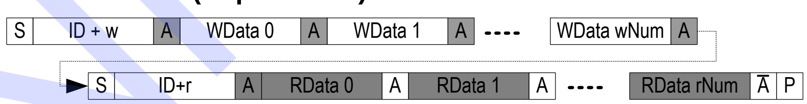
Single Receiver

(1). Set target slave address in ‘ID’.
(2). Set ‘CMD_L’ and ‘CMD_H: RS sets low, R/W sets high for read direction, P sets high to stop the I2C after the I2C wdata transfer done, E sets high to finish this device commands because it is single transmitter, LA set low for NACK, and then set number of read data.

Ex2:

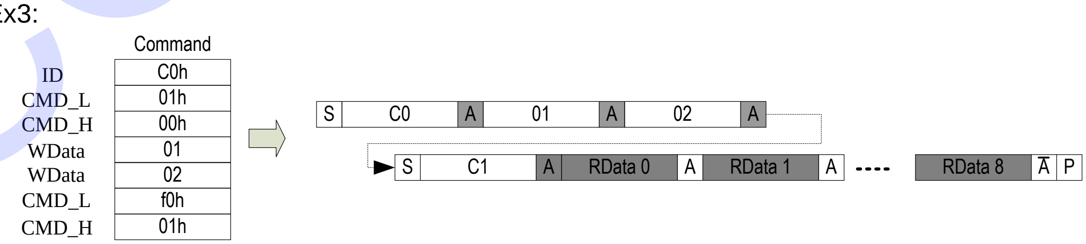


Single Transmitter and Receiver (Repeat Start)

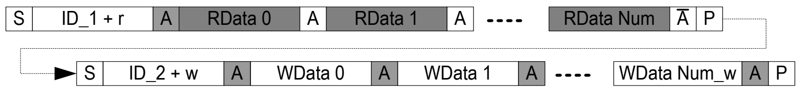


(1). Set target slave address in ‘ID’.
(2). Set ‘CMD_L’ and ‘CMD_H: RS sets low, R/W sets low for write direction, P and E set low, and then set number of write data.
(3). Set ‘WDatas’ for sending out.
(4). Set ‘CMD_L’ and ‘CMD_H: RS sets high for Repeat Start, R/W sets high for read direction, P sets high to stop the I2C after the I2C wdata transfer done, E sets high to finish this device commands because it is single transmitter, LA set low for NACK, and then set number of read data.

Ex3:

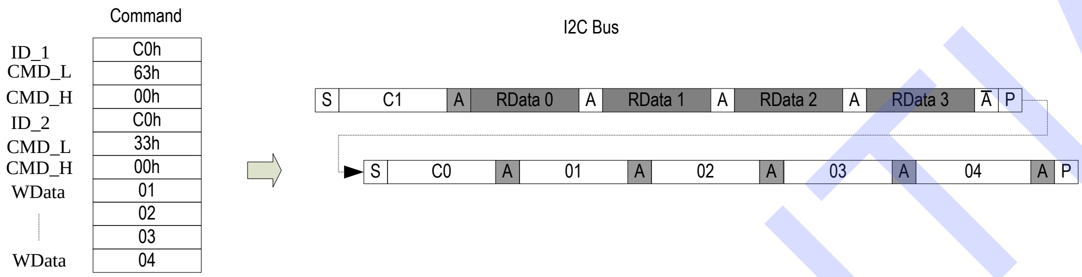


Receiver and then Transmitter



(1). Step same as ‘Single Receiver’, but E sets low to continue command list.
(2). Step same as ‘Single Transmitter’.

Ex4:



Transmitter and Receiver and then Transmitter
(1). Step same as ‘Single Transmitter and Receiver’, but E sets low to continue command list.
(2). Step same as ‘Single Transmitter’.

7.9.3.2 I2C Porting Guide

7.9.3.2.1 Master Interface

The “PSR” (01h) should be programmed before the transaction starts.

Here are the steps as follows. The software shall follow to program the registers for various modes.

Master mode
(1). Set ‘PSR’ registers to decide the I2C speed.
(2). Set ‘DTR’ to send out.
(3). Set CTR1 to enable the I2C Controller, and select number of devices.
(4). Start the transaction (Write 6Ch to CTR, which will select the “Master and ACK”, enable the interrupts, and start the transaction).
(5). When an interrupt is generated, set send out data ‘DTR’ or read received data ‘DRR’, and then set HALT to be 1, Start to be 0, and next byte ACK for send out.
(6). Repeat step (4), till the I2C need STOP condition.
(7). When an interrupt is generated, read received data ‘DRR’, and then set HALT and STOP to be 1.
(8). When an interrupt is generated, the cycle is completed.

Master in Command Queue mode
(1). Set ‘PSR’ registers to decide the I2C speed.
(2). Set ‘Command Address Register’ to get commands and set ‘’Address Register” to store the I2C data.
(3). Set commands in SRAM.
(4). Set CTR1 to COMQ_EN to be one, enable the I2C Controller, and select number of devices.
(5). Set registers of devices: ‘CSR’ and ‘WCSR_i’ are used for period time in the auto mode, ‘LNGRH_i’ and ‘LNGRL_i’ are used to decide stored data length.
(6). Set MODE_SEL and then CTR2 to assign the I2C start run condition [(1)].
(7). Start the transaction (Write 6Ch to CTR, which will select the “Master and ACK”, enable the interrupts, and start the transaction).
(8). When an interrupt is generated, the cycle is completed.

Note:
(1) Run condition:

a) One shot mode, OS: the I2C only run one time when write one into CTR2
b) Inter_in mode, EN: If input enable pin is trigger edge, I2C run one time.
c) Power_save mode, PS: If input enable pin is trigger level, run auto mode.
d) Auto mode, AU: the I2C period run, timing set by CSR, WCSR_i registers(1Fh, 22h)
e) Trigger edge and level is set by EN_TRIG.

7.9.3.2.2 Slave Interface

Slave mode

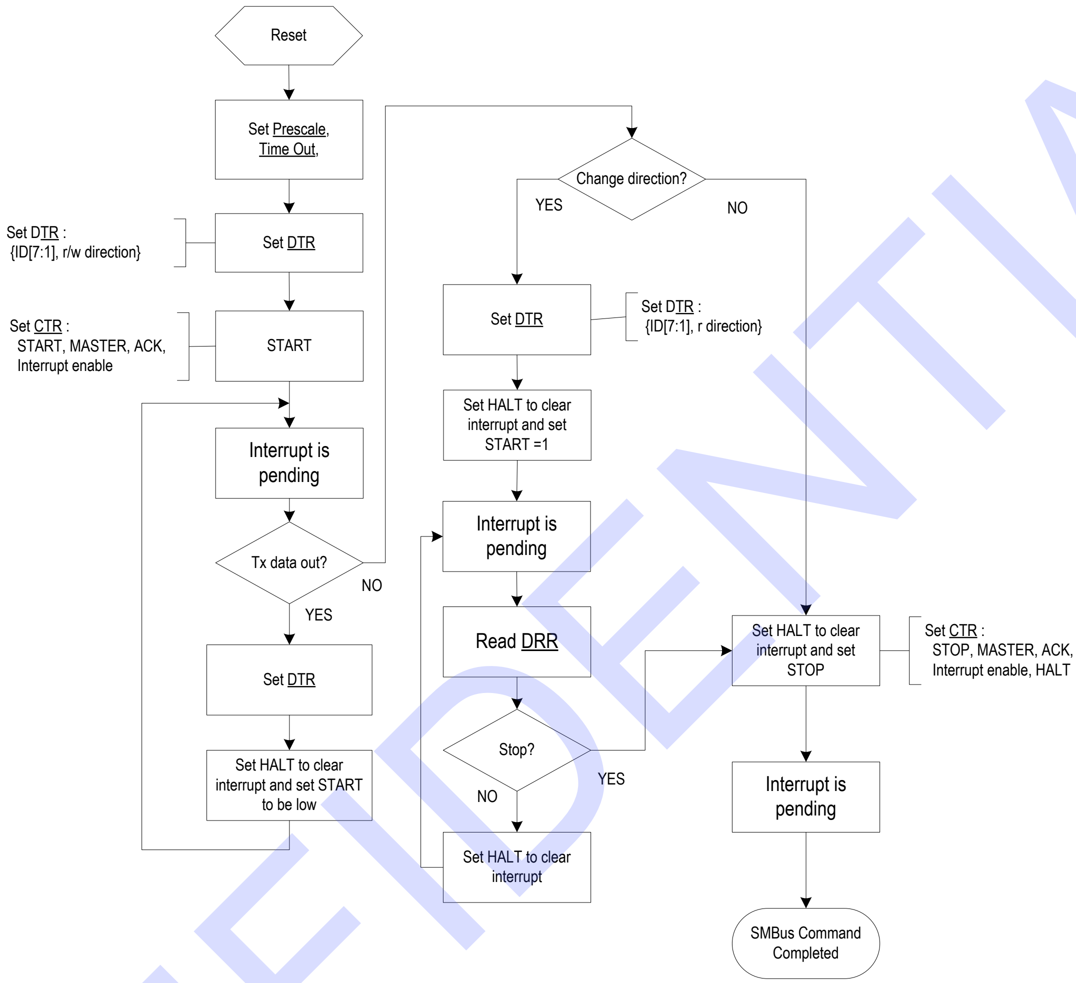
(1). Set Slave ID registers (06h, 01h, 22h, and 2bh).
(2). Set CTR1 to enable the I2C Controller.
(3). Set CTR to be 48h, which will select the "Slave and ACK", and enable the interrupts.
(4). When an interrupt is generated and bus busy, detect R/W direction. If it is read direction, set transmit out data by DTR and then set HALT =1 to clear interrupt. If it's write direction, read received data by "DRR' and then set HALT to clear interrupt.
(5). Repeat step (4).
(6). When an interrupt is generated and bus is not busy, the cycle is completed, and then set HALT to clear interrupt.

Slave in Command Queue mode

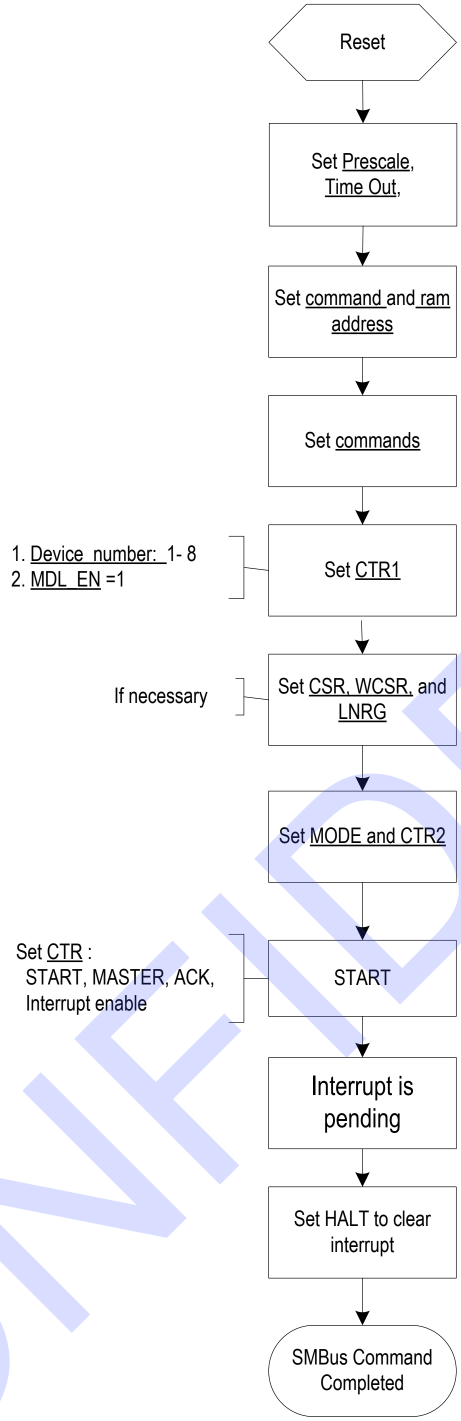
(1). Set Slave ID registers (06h, 01h, 22h, and 2bh).
(2). Set CTR1 to COMQ_EN to be one, and enable the I2C Controller.
(3). Set CTR to be 48h, which will select the "Slave and ACK", and enable the interrupts.
(4). Set 'Address Register 2' (2bh and 2ch) to get transfer out data and set ''Address Register" (23h and 24h) to store the I2C received data.
(5). When an interrupt is generated and bus busy, detect R/W direction. Read 'Interrupt Status' to judge the I2C status. If 'Slave Write Data Flag' asserts that is mean the I2C slave has write data in SRAM. If it is read direction, set transmit out data in SRAM and then set IDR_CLR =1 to clear interrupt. If it is write direction, set IDW_CLR =1 to clear interrupt. If 'Slave Finish' asserts, it is mean the cycle is completed and then set P_CLR =1 to clear interrupt.

7.9.3.3 Master Programming Guide

Program Flow Chart of Master Interface



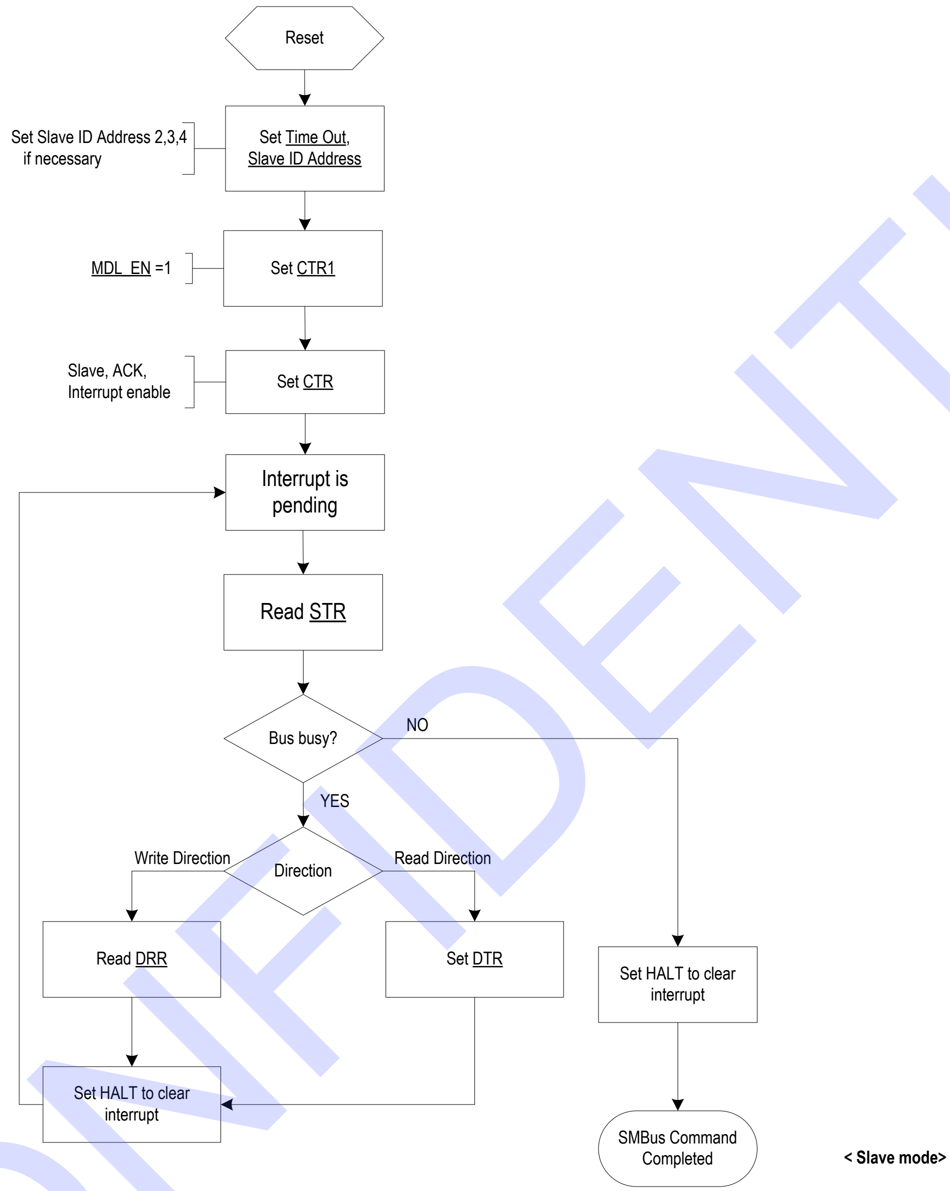
< Slave mode>

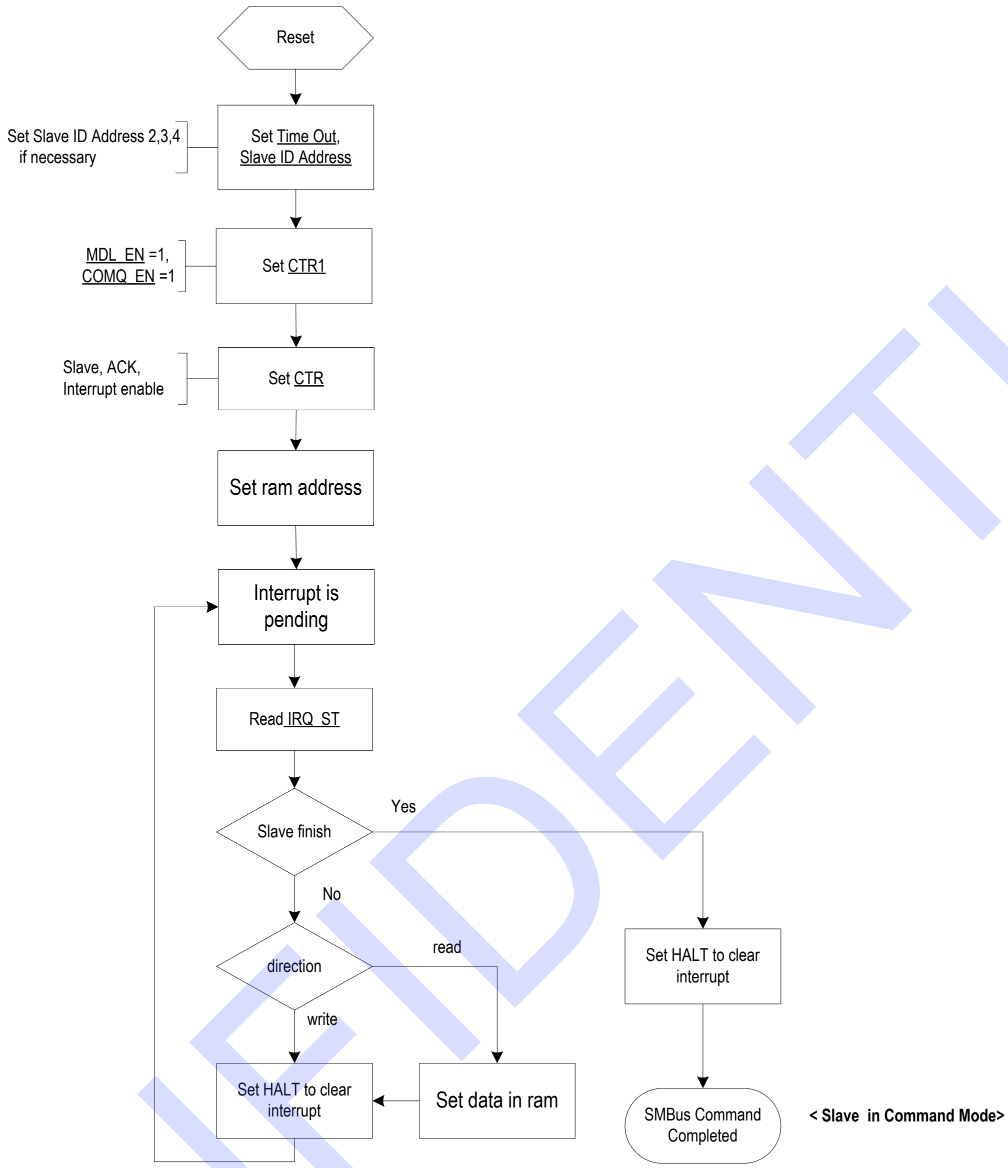


< Master in Command Mode>

7.9.3.4 Slave Programming Guide

Program Flow Chart of Slave Interface




Reset
Set Slave ID Address 2,3,4 if necessary
Set Time Out, Slave ID Address
MDL_EN =1, COMQ_EN =1
Set CTR1
Slave, ACK, Interrupt enable
Set CTR
Set ram address
Interrupt is pending
Read IRQ_ST
Slave finish
Yes
No
direction
read
write
Set HALT to clear interrupt
Set data in ram
Set HALT to clear interrupt
SMBus Command Completed
< Slave in Command Mode>

7.9.4 EC Interface Registers for All Channel

The SMBus I/O registers are listed below. The base address for SMBus is 1C00h.

Table 7-13 EC View Register Map, I2C

7 ... 0	Offset
Channel Select Monitor Register (CHSMOT)	23h
Monitor Write Destination Address Low (MOT_ADDRL)	24h
Monitor Write Destination Address High (MOT_ADDRH)	25h
Monitor Write Pointer Address Low (MOT_IDXL)	26h
Monitor Write Pointer Address High (MOT_IDXH)	27h
Monitor Length Control Register (MOT_LC)	28h
Monitor Length Low Register (MOT_LNGL)	29h
Monitor Length High Register (MOT_LNGH)	2Ah
SCL SDA Swap Register (SW_SCL_SDA)	2Bh
Channel Select combinnation Register (CH_COMB)	2Ch

7.9.4.1 Channel Select Monitor Register (CHSMOT)

Address Offset: 23h

Bit	R/W	Default	Description
7	W	0	**Monitor Reset & Setup**
6-4	-	-	**Reserved**
3	R/W	0	**Monitor Enable**
2-0	R/W	0h	**Monitor** 000b: Monitor is located at Channel A. 001b: Monitor is located at Channel B. 010b: Monitor is located at Channel C. 011b: Monitor is located at Channel D. 100b: Monitor is located at Channel E. 101b: Monitor is located at Channel F.

7.9.4.2 Monitor Write Destination Address Low (MOT_ADDRL)

Address Offset: 24h

Bit	R/W	Default	Description
7-0	R/W	0	**Destination Address Low** Write destination

7.9.4.3 Monitor Write Destination Address High (MOT_ADDRH)

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	0	**Destination Address High** Write destination

7.9.4.4 Monitor Write Pointer Address Low (MOT_IDXL)

Address Offset: 26h

Bit	R/W	Default	Description
7-0	R	0	**Write Pointer Address Low**

7.9.4.5 Monitor Write Pointer Address High (MOT_IDXH)

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R	0	**Write Pointer Address High**

7.9.4.6 Monitor Length Control Register (MOT_LC)

Address Offset: 28h

Bit	R/W	Default	Description
7	R/WC	0	**Buffer 0 full**
6	R/WC	0	**Buffer 1 full**
5	R/WC	0	**All Full Status**
4	R/W	0	**R: Buffer Interrupt Status/ W: Interrupt Enable**
3-0	-	-	**Reserved**

7.9.4.7 Monitor Length Low Register (MOT_LNGL)

Address Offset: 29h

Bit	R/W	Default	Description
7-0	R/W	0	**Write Length Low Byte**

7.9.4.8 Monitor Length High Register (MOT_LNGH)

Address Offset: 2ah

Bit	R/W	Default	Description
7-0	R/W	0	**Write Length High Byte**

Note: {MOT_LNGH, MOT_LNGL} = 1fh -> length = 32,
3fh -> length = 64,
7fh -> length = 128….

7.9.4.9 SCL SDA Swap Register (SW_SCL_SDA)

Address Offset: 2bh

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0	**SMCLK5/SMDAT5 Swap**
4	R/W	0	**SMCLK4/SMDAT4 Swap**
3	R/W	0	**SMCLK3/SMDAT3 Swap**
2	R/W	0	**SMCLK2/SMDAT2 Swap**
1	R/W	0	**SMCLK1/SMDAT1 Swap**
0	R/W	0	**SMCLK0/SMDAT0 Swap**

7.9.4.10 Channel Select combinnation Register (CH_COMB)

Address Offset: 2ch

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0	**CHF & CHE & CHD** Channel F link with Channel E & Channel D and output default pins are SMCLK5/SMDAT5. (only slave mode)
3	-	-	**Reserved**
2	R/W	0	**CHE & CHF** Channel F link with Channel E and output default pins are SMCLK5/SMDAT5.
1	R/W	0	**CHE & CHD** Channel E link with Channel D and output default pins are SMCLK3/SMDAT3.
0	-	-	**Reserved**

7.9.5 EC Interface Registers for Each Channel

The Enhanced SMBus/I2C Controller registers are listed below. Note that all registers can be Byte access. The base addresses are **0x3680 for channel D, 0x3500 for channel E, 0x3580 for channel F.**(**Note:** channel F supports only one master setting)

Table 7-14 EC View Register Map, I2C

7 0	Offset
Data Receive Register (DRR)	00h
Prescale Register for SCL Low (PSRL)	01h
Prescale Register for SCL High (PSRH)	02h
Status Register (STR)	03h
Data Hold Time Register (DHTR)	04h
Time Out Register (TOR)	05h
ID Address Register (IDR)	06h
Time Out Status (TOS)	07h
Data Transmit Register (DTR)	08h
Control Register (CTR)	09h
Control Register 1 (CTR1)	0Ah
Byte Counter Register (BYTE_CNT_H)	0Bh
Byte Counter Register (BYTE_CNT_L)	0Ch
Interrupt Status (IRQ_ST)	0Dh
Number of Receive High Data (SLV_NUM_H)	10h
Number of Receive Low Data (SLV_NUM_L)	11h
Status Register 2 (STR2)	12h
Nack Status Register (NST)	13h
Time Buffer Register (T_BUF)	14h
Four Devices, [i = 1,2,3, or 4]	-
Threshold Status Register (TH_ST)	16h
Threshold Full Status Register (THF_ST)	17h
Timeout and Arbiter Status Register (TO_ARB_ST)	18h
Error Status Register (ERR_ST)	19h
I2C Enable Trigger Level (EN_TRIG)	1Ah
Finish Status Register (FST)	1Bh
Error Mask Register (EM)	1Ch
Mode Select Register (MODE_SEL)	1Dh

7 0	Offset
Clock Scale Register (CSR) / ID Address Register 2 (IDR2)	1Fh
Control Register 2 (CTR2) / Command Index 1 (CMD_IDX_1)	20h
Command Index 2 (CMD_IDX_2)	21h
Wait time Scale Register i (WCSR_i), [i = 1, 2, 3 or 4] / ID Address Register 2+i (IDR2+i), [i = 1, 2]	22h + [9(i-1)]d
High Byte Address Register (RAMHA_i)	23h + [9(i-1)]d
Low Byte Address Register (RAMLA_i)	24h + [9(i-1)]d
High Byte Command Address Register (CMD_ADDH_i)	25h + [9(i-1)]d
Low Byte Command Address Register (CMD_ADDL_i)	26h + [9(i-1)]d
High Byte Data Length i (LNGRH_i)	27h + [9(i-1)]d
Low Nibble Data Length i/ Status (LNGRL_i/ST)	28h + [9(i-1)]d
Data Length Status High i (LNGSTH_i)	29h + [9(i-1)]d
Threshold Control Register (TH_CTR_i)	2Ah + [9(i-1)]d
High byte 2 Address Register (RAMH2A_i)	50h + [6(i-1)]d
High Byte 2 Command Address Register (CMD_ADDH2_i)	52h + [6(i-1)]d
High Byte 2 of Write Memory Address Register (WM_ADDRH2_i)	54h + [6(i-1)]d

7.9.5.1 Data Receive Register (DRR)

This register presents the receiving 8-bit data which transmits or receives before NACK or ACK term on the I2C bus.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R	00h	**Data Receive** Indicates the received data for the I2C controller.

7.9.5.2 Prescale Register for SCL Low (PSRL)

This register is used to program the I2C speed for SCL low period and it includes the standard, fast, and fast plus speed in the master mode.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	2h	**Prescale Register for SCL Low** This register is used to prescale SCL clock line. 02h: 1 SCL cycle = 2 x (2+2) SMB clock cycle. 03h: 1 SCL cycle = 2 x (3+2) SMB clock cycle. … FD h: 1 SCL cycle = 2 x (253 +2) SMB clock cycle.

7.9.5.3 Prescale Register for SCL High (PSRH)

This register is used to program the I2C speed for SCL high period and it includes the standard, fast, and fast plus speed in the master mode.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	2h	**Prescale Register for SCL High** This register is used to prescale the SCL clock line. 02h: 1 SCL cycle = 2 x (2+2) SMB clock cycle. 03h: 1 SCL cycle = 2 x (3+2) SMB clock cycle. … FD h: 1 SCL cycle = 2 x (253 +2) SMB clock cycle.

7.9.5.4 Status Register (STR)

All status bits are set by hardware and cleared by writing a one to the particular bit position by the software.

Address Offset: 03h

Bit	R/W	Default	Description
7	R	0	**Byte Transfer Done** This bit indicates that one byte of data is being transferred. It is set to 1 when one byte data is transferred and cleared to 0 when HALT is set. 0: Byte transfer in progress. 1: Byte transfer completed.
6	R	0	**Address Match** This bit will be set when the address of the core matches.
5	R	0	**Bus Busy (BB)** This bit indicates the bus is involved in transaction. This will be set at START condition and cleared at STOP condition.
4	R	0	**Arbitration Lost (ARB)** This bit will go high if the master has lost its arbitration in the master mode.
3	R	0	**Time Out (Time_out)** This bit indicates that maximum time, for which SCL or SDA can be in low state, has elapsed.
2	R	0	**Read/Write** 0: Master transmitting / Slave receiving. 1: Master receiving / Slave transmitting.
1	R	0	**Interrupt Pending** This bit is set when the interrupt is pending The interrupt is as follows, and cleared when HALT is set. PIO mode: finish transaction of one byte or the I2C stop condition. ComQ mode: the I2C and the DMA end to transmit or receive data. Other: see the IRQ_ST
0	R	0	**ACK Receive** This bit is set to 1 when an ACK is received and set to 0 when a NACK is received. It will be updated after the transaction of each byte.

7.9.5.5 Data Hold Time Register (DHTR)

Address Offset: 04h

Bit	R/W	Default	Description
7	W	0	**Software Reset**

Bit	R/W	Default	Description
6	R/W	0	**Arbiter Interrupt Mask**
5	-	-	**Reserved**
4	R	0	**DMA IDLE**
3	R	0	**IRQ_All** This bit is set to 1 when timeout, arbitration lost, interrupt, or error status occurs.
2-0	R/W	0	**Data hold time** 0: 3T smb_clk 1: (3+1)T smb_clk 2: (3+2)T smb_clk …. 7: (3+7)T smb_clk **Note:** T = 1/smb_clk (sec)

7.9.5.6 Time Out Register (TOR)

The time-out feature starts whenever the SCL or the SDA goes low. If the SCL or the SDA stays low for a period greater than the time-out value, the core concludes there is a bus error and generates an interrupt. Then it needs to read the status register and reset the controller.

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/W	ffh	**Time Out Register** This register is used to determine the maximum time that the SCL or the SDA is allowed to be low before the I2C controller is reset. 01h: 1 1KHz clock cycle. 02h: 2 1KHz clock cycle. … FFh: 255 1KHz clock cycle.

7.9.5.7 ID Address Register (IDR)

The contents of this register are irrelevant when core is in a master mode. In the slave mode, the seven most significant bits must be loaded with the micro-controller's address.

The most significant bit corresponds to the first bit received from the I2C bus after a START condition. The least significant bit is not used but should be programmed with a "0".

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	0	**ID Register** Indicates the address of I2C slave.

7.9.5.8 Time Out Status (TOS)

Address Offset: 07h

Bit	R/W	Default	Description
7	R/W	0	**Clock Stretching** 0: Byte Stretching 1: Bit stretching
6	R	0	**SCL Time out** Time out is occurred by the SCL, and it cleared by State_reset

Bit	R/W	Default	Description
5	R	0	**SDA Time out** Time out is occurred by the SDA, and it cleared by State_reset
4	R	0	**SCL_O** The SCL output signal
3	R	0	**SCL_OE** The SCL output Enable signal
2	R	1	**SCL_IN** The SCL input signal
1	R	0	**SDA_OE** The SDA output Enable signal
0	R	1	**SDA_IN** The SDA input signal

7.9.5.9 Data Transmit Register (DTR)

This register presents the next 8-bit data transmitted out by the I2C bus or writing data into FIFO set by writing a one to the particular bit position by the software.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	0	**Data Transmit** Indicates the transmitted data for the I2C controller.

7.9.5.10 Control Register (CTR)

This register is used to generate I2C start or stop signal and set transmit or receive based situation.

Address Offset: 09h

Bit	R/W	Default	Description
7	R/W	0	**Rx_MODE** 0: Standard mode. 1: Receive mode. Do not need to compare ID and always receive data in this mode.
6	R/W	0	**I2C Interrupt Enable** 0: Interrupt disabled. 1: Interrupt enabled.
5	R/W	0	**Mode Select (MODE)** 0: Slave mode. 1: Master mode.
4	WC	0	**State Reset**
3	R/W	0	**Acknowledge (ACK)** This bit specifies the value of SDA line during acknowledge cycle (9th SCL pulse).
2	R/W	0	**Start & Repeat Start (START)** This bit indicates that controller wants a repeated START. 0: No start. 1: Start.
1	R/W	0	**Stop** This bit indicates that controller wants a repeated STOP. 0: No stop. 1: Stop.

Bit	R/W	Default	Description
0	R/WC	0	**Hardware Reset (HALT)** This bit must be set to start the next transmission whenever the controller has transmitted 8 bits and acknowledge bit. Set this bit to reset the halt condition and then clear it to 0.

7.9.5.11 Control Register 1 (CTR1)

Address Offset: 0Ah

Bit	R/W	Default	Description
7	R/W	0	**COMQ_EN**
6-4	R/W	0	**Supported Number of Devices**
3	-	-	**Reserved**
2	R/W	0	**Sleep mode Enable** Masters wake up interrupt enable in the auto mode or slave detects start signal and then hangs on SCL to low.
1	R/W	0	**Module Enable(MDL_EN)** Turn on I2C, which is a protect bit**.** It must be set one when this I2C module is used.
0	-	-	**Reserved**

7.9.5.12 Byte Counter Register (BYTE_CNT_H)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	R/W	0h	**Byte Counter Register** This byte indicates byte_cnt[10:3]

7.9.5.13 Byte Counter Register (BYTE_CNT_L)

Address Offset: 0Ch

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0	**Disable Stop Interrupt**
5	R/W	0	**DMA Address reload** Master and Slave write use
4	R/W	0	**DMA Address reload** Slave read use
3	R/W	0	**Byte Counter Enable**
2-0	R/W	0	**Byte Counter Register** This byte indicates byte_cnt[2:0]

7.9.5.14 Interrupt Status (IRQ_ST)

Address Offset: 0Dh

Bit	R/W	Default	Description
7	R/WC	0	**Buffer 0 Empty** Using in slave transmitter. This bit presents that the first half of transfer data is empty in SRAM.
6	R/WC	0	**Buffer 1 Empty** Using in slave transmitter. This bit presents that the latter half of transfer out data is empty in SRAM.

5	R/WC	0	**Master Finish** This bit will be high when the DMA and the I2C done.
4	R/WC	0	**Count Hold Flag** This bit will be high when Byte_Counter_Enable is turn on, and byte transfer done in command queue
3	R/WC	0	**Slave ID write Flag**(IDW_CLR) This bit will be high when the I2C receives ID and write direction.
2	R/WC	0	**Slave ID read Flag**(IDR_CLR) This bit will be high when the I2C receives ID and read direction.
1	R/WC	0	**Slave received Data Flag** In Slave mode, the I2C has unprocessed write data.
0	R/WC	0	**Slave Finish**(P_CLR) This bit will be high when the DMA and the I2C done.

7.9.5.15 Number of Receive High Data in Slave Mode (SLV_NUM_H)

Address Offset: 10h

Bit	R/W	Default	Description
7-0	R	0	**Number of High Data** Record the number of received high data in slave mode. slv_dat_num[10:8]

7.9.5.16 Number of Receive Low Data in Slave Mode (SLV_NUM_L)

Address Offset: 11h

Bit	R/W	Default	Description
7-0	R	0	**Number of Data** Record the number of received low data in slave mode. slv_dat_num[7:0]

7.9.5.17 Status Register 2 (STR2)

Address Offset: 12h

Bit	R/W	Default	Description
7-4	R	0	**ID Match Status** [7]: Slave ID4 match (ID4 offset: 2bh) [6]: Slave ID3 match (ID3 offset: 22h) [5]: Slave ID2 match (ID2 offset: 1fh) [4]: Slave ID1 match (ID1 offset: 06h) And they are cleared by hardware when the I2C bus appears start signal.
3	R	1	**Module IDLE** Nothing to do in this module
2	R	1	**Command Queue IDLE**
1	R	0	**Controller Busy Status**
0	R/WC	0	**Wake Up** Master uses in the auto mode and slave uses to detect start signal. This bit clear by sleep_mode_enable.

7.9.5.18 Nack Status Register (NST)

Address Offset: 13h

Bit	R/W	Default	Description
7	W	-	**Clear Nack Status**

6	-	-	**Reserved**
5	R/W	0	**SCL Drive Low** 1: The SMCLK pin will be driven low regardless of the other SMBus logic. 0: The SMCLK pin will not be driven low. The other SMBus logic controls this pin.
4	R/W	0	**SDA Drive Low** 1: The SMDAT pin will be driven low regardless of the other SMBus logic. 0: The SMDAT pin will not be driven low. The other SMBus logic controls this pin.
3-0	R	0	**Nack Receive Status** [3]: ID [2]: First data [1]: Middle data [0]: Last data

7.9.5.19 Time Buffer Register (T_BUF)

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R/W	0	**Time Buffer** This register is used to set the I2C timing for STOP to START.

7.9.5.20 Threshold Status Register (TH_ST)

Address Offset: 16h

Bit	R/W	Default	Description
7-4	R	0	**Length Full** [3]: Device 4 [2]: Device 3 [1]: Device 2 [0]: Device 1
3-0	R	0	**Threshold Interrupt Pending** [3]: Device 4 [2]: Device 3 [1]: Device 2 [0]: Device 1

7.9.5.21 Threshold Full Status Register (THF_ST)

Address Offset: 17h

Bit	R/W	Default	Description
3-0	R	0	**Length Full** [3]: Device 4 [2]: Device 3 [1]: Device 2 [0]: Device 1

7.9.5.22 Timeout and Arbiter Status Register (TO_ARB_ST)

Address Offset: 18h

Bit	R/W	Default	Description
7	R/W	1	**SCL Timeout Enable**
6	R/W	1	**SDA Timeout Enable**

5	R/WC	0	**SCL Timeout** SCL timeout status and write one clear
4	R/WC	0	**SDA Timeout** SDA timeout status and write one clear
3	R/W	0	**Arbitration Enable**
2	R	0	**Arbitration Lost**
1-0	R/WC	0	**Arbitration Status** arbitration status and write 1h to clear 3h: Device 4 2h: Device 3 1h: Device 2 0h: Device 1

7.9.5.23 Error status Register (ERR_ST)

Address Offset: 19h

Bit	R/W	Default	Description
7	R	0	**Wake up IRQ** Slave wake up by start signal
6	R	0	**Threshold IRQ**
5	R	0	**Timeout IRQ**
4	R	0	**Arbitration IRQ**
3-0	R/WC	0	**Error IRQ** Error occurs when NACK (read data phase not included) received, and write one clear. [3]: Device 4 Error have occurred [2]: Device 3 Error have occurred [1]: Device 2 Error have occurred [0]: Device 1 Error have occurred

7.9.5.24 I2C Enable Trigger Level (EN_TRIG)

Address Offset: 1Ah

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	1	**Trigger Mode for Device 4 Interrupt Input** 1: High trigger 0: Low trigger
2	R/W	1	**Trigger Mode for Device 3 Interrupt Input** 1: High trigger 0: Low trigger
1	R/W	1	**Trigger Mode for Device 2 Interrupt Input** 1: High trigger 0: Low trigger
0	R/W	1	**Trigger Mode for Device 1 Interrupt Input** 1: High trigger 0: Low trigger

7.9.5.25 Finish Status (FST)

Address Offset: 1Bh

Bit	R/W	Default	Description
	R	0	**Master Finish IRQ (IRQ_M)** [7]: Device 4 Fin, clear by write one in b3

7-4			[6]: Device 3 Fin, clear by write one in b2 [5]: Device 2 Fin, clear by write one in b1 [4]: Device 1 Fin, clear by write one in b0 or clear by halt reset[b0@xx09h] or stop clear [b5@xx0dh]. Disable in [b7-4@xx1ch]
3-0	R/WC	0	**Which Master Finish** [3]: Device 4 Fin [2]: Device 3 Fin [1]: Device 2 Fin [0]: Device 1 Fin

7.9.5.26 Error Mask Register (EM)

Address Offset: 1Ch

Bit	R/W	Default	Description
7-4	R/W	0	**Master Finish IRQ Disable Register** This register is used to disable IRQ_M. [3]: Device 4 [2]: Device 3 [1]: Device 2 [0]: Device 1
3-0	R/W	0	**Error Mask Register** This register is used to mask error. [3]: Device 4 [2]: Device 3 [1]: Device 2 [0]: Device 1

7.9.5.27 Mode Select Register (MODE_SEL)

Address Offset: 1Dh

Bit	R/W	Default	Description
7-6	R/W	0	**Device 4** 00b: **One shot**: I2C only runs one time. 01b: **Enable mode**: If interruput_in is asserted, I2C runs one time. 10b: **Power saving mode**: If interruput_in is in the trigger level, I2C period runs. 11b: **Auto mode**: I2C period runs. **Note**: The period can be setup by Wait time Scale Register, and please refer to the following for the detail.
5-4	R/W	0	**Device 3** Same as the above
3-2	R/W	0	**Device 2** Same as the above
1-0	R/W	0	**Device 1** Same as the above

7.9.5.28 Clock Scale Register (CSR) / ID Address Register 2 (IDR2)

In the master mode (SMB/I2C/BLK), the I2C controller will be repeated execution. This register is used to program the clock scale.

Address Offset: 1Fh

Bit	R/W	Default	Description
7-0	R/W	0	**Master: Clock Scale Register** This register is used to scale clock. 1 prescale clock cycle = M x APB clock cycle. 01h: 1 x 32KHz clock cycles. 02h: 2 x 32KHz clock cycles. … FFh: 255 x 32KHz clock cycles. **Slave: ID Register 2** Indicates the address of I2C slave.

7.9.5.29 Control Register 2 (CTR2) / Command Index 1 (CMD_IDX_1)

Address Offset: 20h

Bit	R/W	Default	Description
7-0	W	0	**CPU one Shot** One shot mode. [3]: Device 4 [2]: Device 3 [1]: Device 2 [0]: Device 1
7-4	R	0	**Command Index** These bits record the command number implemented by the current I2C bus in the command queue mode in Device 2.
3-0	R	0	**Command Index** These bits record the command number implemented by the current I2C bus in the command queue mode in Device 1.

7.9.5.30 Command Index 2 (CMD_IDX_2)

Address Offset: 21h

Bit	R/W	Default	Description
7-4	R	0	**Command Index** These bits record the command number implemented by the current I2C bus in the command queue mode in Device 4.
3-0	R	0	**Command Index** These bits record the command number implemented by the current I2C bus in the command queue mode in Device 3.

7.9.5.31 Wait time Scale Register i (WCSR_i), [i = 1, 2, 3 or 4] / ID Address Register 2+i (IDR2+i), [i = 1, 2]

Address Offset: **22h** + [9(i-1)]d

Bit	R/W	Default	Description
7-0	R/W	0	**Master: Waiting Time** This register is used to scale waiting time. Waiting time = N x 1 prescale clock cycle. **Slave: ID Register 2+i , [i = 1,2]** Indicates the address of I2C slave.

7.9.5.32 High Byte Address Register (RAMHA_i)

Address Offset: **23h** + [9(i-1)]d

Bit	R/W	Default	Description
7-0	R/W	0	**RAM High Address** Indicates the high address of RAM for Rx data in Master mode.

Note: Low addresses are listed below.

7.9.5.33 Low Byte Address Register (RAMLA_i)

Address Offset: **24h** + [9(i-1)d

Bit	R/W	Default	Description
7-0	R/W	0	**RAM Low Address** Indicates the low address of RAM for Rx data in Master mode.

Note: Slave Tx data is on 2ch and 2dh, and Rx data on 23h and 24h.

7.9.5.34 High Byte Command Address Register (CMD_ADDH_i)

Address Offset: **25h** + [9(i-1)d

Bit	R/W	Default	Description
7-0	R/W	0	**CMD RAM High Address** Indicates the high address of RAM for Tx data in Master mode.

Note: Low addresses are listed below.

7.9.5.35 Low Byte Command Address Register (CMD_ADDL_i)

Address Offset: **26h** + [9(i-1)]d

Bit	R/W	Default	Description
7-0	R/W	0	**CMD RAM Low Address** Indicates the low address of RAM for Tx data in Master mode.

7.9.5.36 Data Length High (LNGRH_i)

Address Offset: **27h** + [9(i-1)]d

Bit	R/W	Default	Description
7-0	R/W	0	**Receiver Length** The length of burst data stored in RAM. Lengthi[11:4]

7.9.5.37 Data Length Low Nibble /ST (LNGRL_i/ST)

Address Offset: **28h** + [9(i-1)]d

Bit	R/W	Default	Description
7-4	R	0	**Length Status Low Nibble** Record the length status for latest data. Length_STi[3:0]
3-0	R/W	0	**Receiver Length** The length of burst data stored in RAM. Lengthi[3:0]

7.9.5.38 DMA Data Length High Status (LNGSTH_i)

Address Offset: **29h** + [9(i-1)]d

Bit	R/W	Default	Description
7-0	R	0	**Length Status High Byte** Record the length status for latest data. Length_STi[11:4]

7.9.5.39 Threshold Control Register (TH_CTR_i)

Address Offset: **2Ah** + [9(i-1)]d

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	W	-	**Read Pointer Controller** After CPU read out data from RAM, write one into this bit to control or mark read pointer.
5	R/WC	0	**Full & Threshold Reset**
4	R/W	0	**Threshold Enable**
3	-	-	**Reserved**
2-0	R/W	0	**Threshold Size** When (write pointer - read pointer) > threshold size, the interrupt will assert. 3'h0: 1/2 * (Data Length[11:0] +1) 3'h1: 3/4 * (Data Length[11:0] +1) 3'h2: 7/8 * (Data Length[11:0] +1)

7.9.5.40 High Byte 2 Address Register (RAMH2A_i)

Address Offset: **50h** + [6(i-1)]d

Bit	R/W	Default	Description
7-0	R/W	0	**RAM High Byte 2 Address** Indicates the high byte 2 address of RAM for Rx data in Master mode.

7.9.5.41 High Byte 2 Command Address Register (CMD_ADDH2_i)

Address Offset: **52h** + [6(i-1)]d

Bit	R/W	Default	Description
7-0	R/W	0	**CMD RAM High Byte 2 Address** Indicates the high byte 2 address of RAM for Tx data in Master mode.

7.9.5.42 High Byte 2 of Write Memory Address Register (WM_ADDRH2_i)

Address Offset: **54h** + [6(i-1)]d

Bit	R/W	Default	Description
7-0	R/W	0	**High Byte 2 of Write Memory Address** Indicates the high byte 2 address of Write Memory Address for Tx data in Master mode. Combined with WM_ADDRH3_i, wr_ptr_h and wr_ptr_l in Command Queue.

7.10 Platform Environment Control Interface (PECI)

7.10.1 Overview

The Platform Environment Control Interface (PECI) can maintain bi-directional communication with external devices through the PECI pin. It is compatible with the PECI 2.0/3.0/3.1 specification.

7.10.2 Features

- Supports both Host and EC side.
- Supports PECI 2.0/3.0/3.1
- Supports 16-byte write/read length
- Supports FCS checking mechanism
- Supports AW_FCS hardwired mechanism
- Supports adjustable V_{TT} level

7.10.3 Functional Description

The PECI module can maintain bi-directional communication with PECI devices (e.g. Intel processor). The PECI host controller supports all command protocols as listed in the PECI 2.0/3.0/3.1 specification, including Ping(), GetDIB(), GetTemp() and so on. In addition, it supports FCS checking mechanism and PECI Assured Write Message as well.

This function only works if PLLFREQ == 0100b. (Refer to those listed in Table 10-2 on page 570.)

7.10.3.1 PECI Porting Guide

The PECI host controller requires that target address, write length, read length, command, and write data be setup for various commands to be sent out. Based on the PECI 2.0/3.0/3.1 specification, software must setup data and command (as mentioned above) before START. When the START bit in the Host Control Register is set, the PECI host controller will perform the requested transaction. Any register values needed for computation purposes should be saved prior to issuing a new command.

Here are the steps the software shall follow to program the registers for various commands.

(1). After system resets, switch the related GPIO to the PECI function mode, and then enable the PECI Host Controller (the PECIHEN bit in Host Control Register is set to 1).
(2). Depending on the desired command, software shall write data to the Host Target Address Register, Host Write Length Register, Host Read Length Register, Host Command Register, and Host Write Data Register.
(3). Start the transaction (Write 09h to the Host Control Register, which will enable the PECI Host, and start the transaction).
(4). During the transaction, software shall read the Host Status Register to check whether the transaction is being performed or not (the Host Busy bit in the Host Status Register will be set during the transaction).
(5). For the polling mode, software continues reading the Host Status Register to check whether the transaction is completed or not (the Finish bit in the Host Status Register will be set when the transaction is completed). For the interrupt mode, the Host Status Register will be available after data-valid event occurs resulting from PECI interrupt.
(6). When the transaction is completed, software can read the Host Read Data Register to get the received data if necessary.
(7). If the programmer requires that hardware support the AW_FCS calculation in the commands supporting the Assured Write Message during the transaction, the AWFCS_EN or AWFCS_FRC_CTRL bit in the Host Control Register shall be set before START.

7.10.3.2 PECI Programming Guide

Figure 7-12. Program Flow Chart for Polling Mode

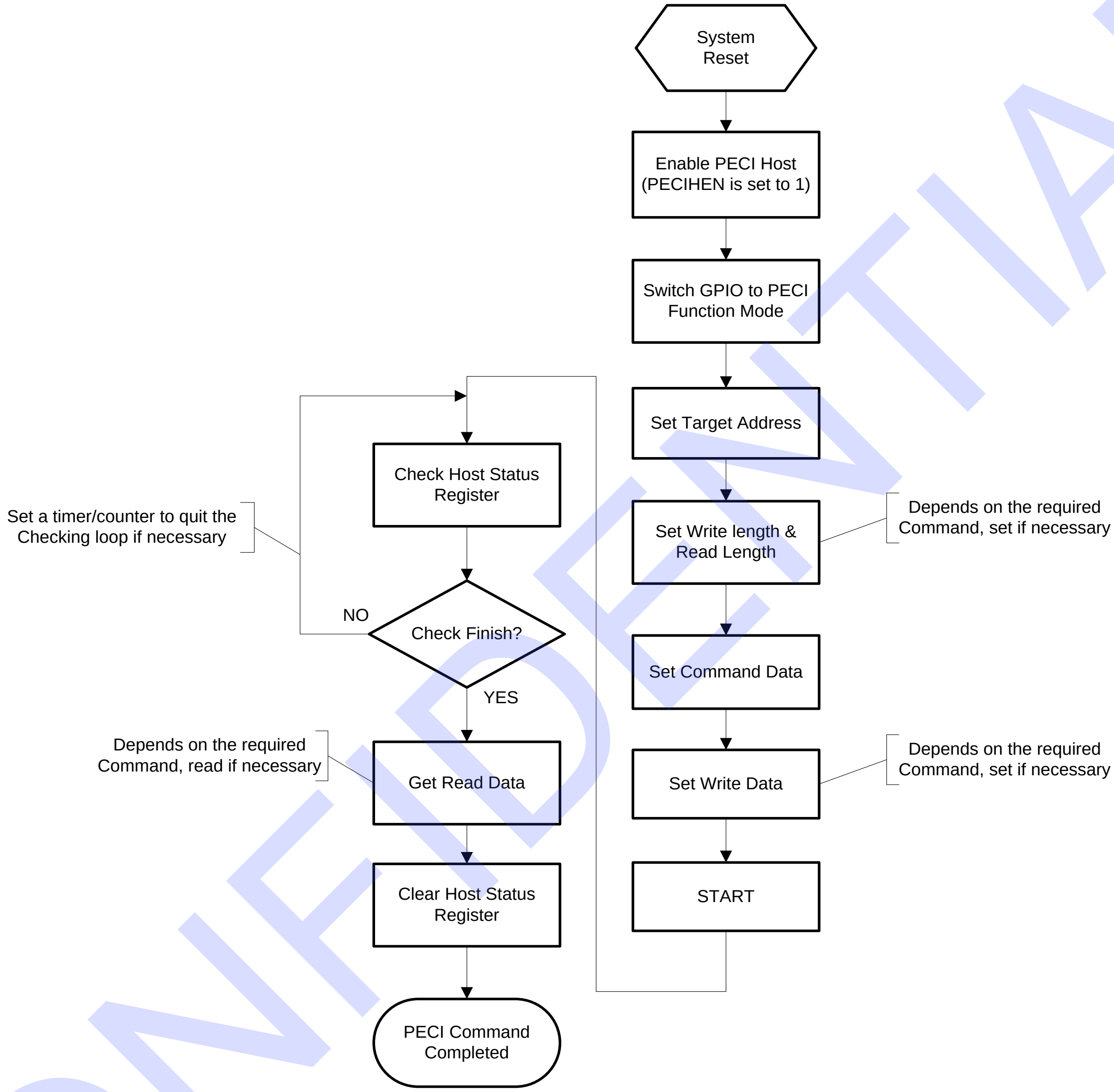
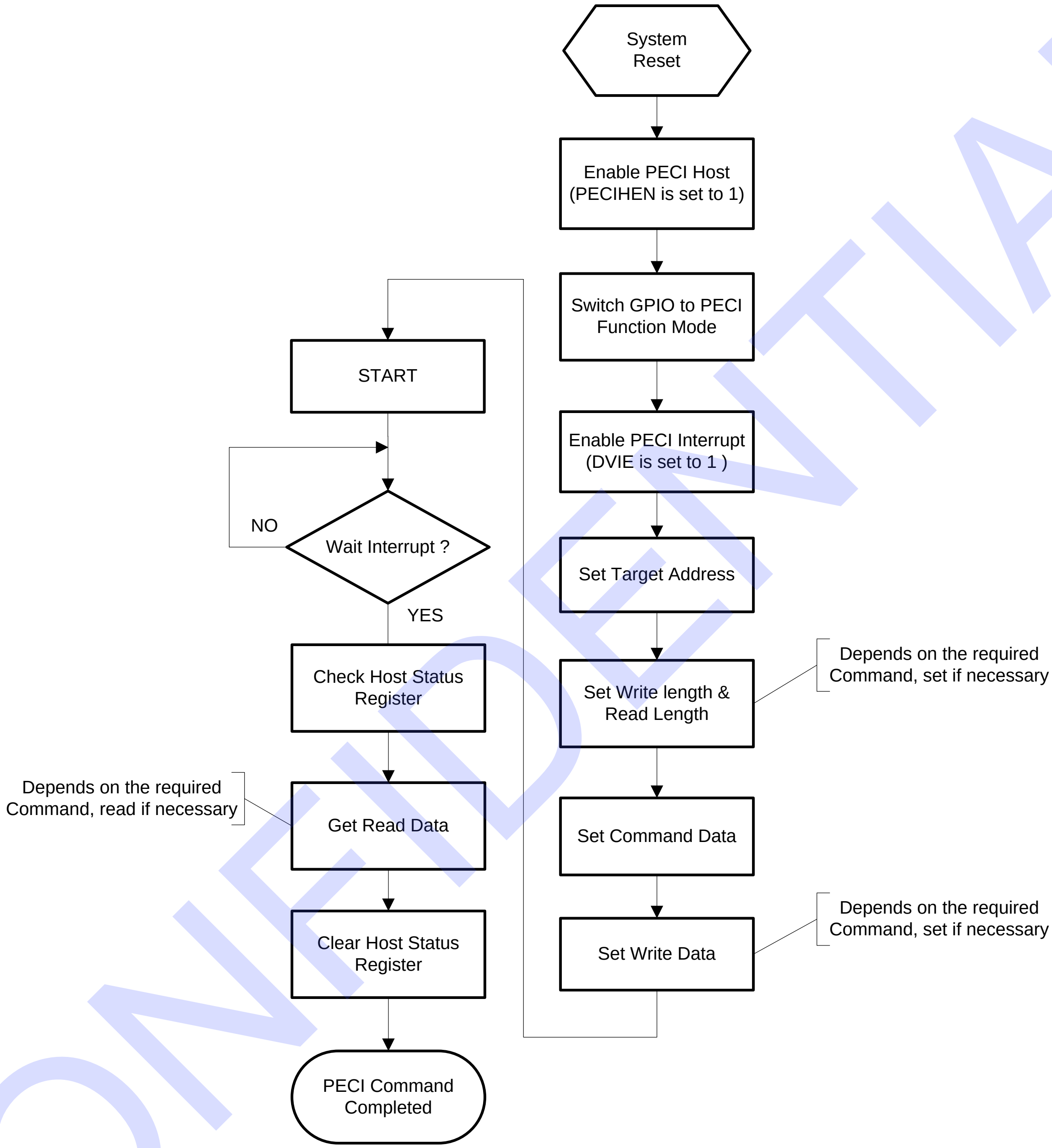


Figure 7-13. Program Flow Chart for Interrupt Mode



7.10.4 Host Interface Registers

The registers of PECI can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.
The PECI resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below:

Table 7-15. Host View Register Map, PECI

7	0	Offset
Host Status Register (HOSTAR)		00h

7	0	Offset
Host Control Register (HOCTLR)	HHRAE = 0	01h
Host Command Register (HOCMDR)		02h
Host Target Address Register (HOTRADDR)		03h
Host Write Length Register (HOWRLR)		04h
Host Read Length Register (HORDLR)		05h
Host Write Data Register (HOWRDR)		06h
Host Read Data Register (HORDDR)		07h
Host Control 2 Register (HOCTL2R)	HHRAE = 1	01h
Pad Control Register (PADCTLR)	HHRAE = 1	07h
Received Write FCS Value (RWFCSV)	HHRAE = 1	02h
Received Read FCS Value (RRFCSV)	HHRAE = 1	03h
Write FCS Value (WFCSV)	HHRAE = 1	04h
Read FCS Value (RFCSV)	HHRAE = 1	05h
Assured Write FCS Value (AWFCSV)	HHRAE = 1	06h

All registers are double mapped into the host and EC side; however, the PECI function should be controlled by a side only.

The definition of all registers are the same as their identical register names in the EC side except HHRAE (Host Side High Range Address Enable) bit. HHRAE bit is located in bit 7 in the registers with offset 01h (HOCTLR or HOCTL2R). HHRAE bit is used to select different registers if they have the same offset number.

7.10.5 EC Interface Registers

The register map of EC interface is listed below. The base address for PECI is 2C00h.

Table 7-16. EC View Register Map, PECI

7 0	Offset
Host Status Register (HOSTAR)	00h
Host Control Register (HOCTLR)	01h
Host Command Register (HOCMDR)	02h
Host Target Address Register (HOTRADDR)	03h
Host Write Length Register (HOWRLR)	04h
Host Read Length Register (HORDLR)	05h
Host Write Data Register (HOWRDR)	06h
Host Read Data Register (HORDDR)	07h
Host Control 2 Register (HOCTL2R)	08h
Pad Control Register (PADCTLR)	0Eh
Received Write FCS Value (RWFCSV)	09h
Received Read FCS Value (RRFCSV)	0Ah
Write FCS Value (WFCSV)	0Bh
Read FCS Value (RFCSV)	0Ch
Assured Write FCS Value (AWFCSV)	0Dh

Other related register(s):

- General Control 2 Register (GCR2), PECIE bit
- General Control 3 Register (GCR3), PECIPDG bit

7.10.5.1 Host Status Register (HOSTAR)

All status bits are set by hardware and cleared by writing a one to the particular bit position by the software. Software can read this register to know the status of the command.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/WC	0b	**PECI GetTemp() Command Receive Error Code (RCV_ERRCODE)** This bit reports the status of receiving the error code (8000h ~ 81FFh). 0: No error. 1: The error code in the GetTemp() command is received.
6	R/WC	0b	**PECI Bus Abnormal/Contention Error (BUSERR)** This bit reports the PECI line status. 0: No error. 1: Abnormal/Contention error occurs.
5	R/WC	0b	**PECI Slave Message Phase t-bit Extend over Error (EXTERR)** This bit reports the PECI line status. 0: No error 1: T-bit extend over error occurs.
4	-	0b	**Reserved**
3	R/WC	0b	**Write_FCS Error (WR_FCS_ERR)** This bit reports if the write FCS error occurs in the communication or not. 0: No error. 1: Write_FCS error occurs.
2	R/WC	0b	**Read_FCS Error (RD_FCS_ERR)** This bit reports if the read FCS error occurs in the communication or not. 0: No error. 1: Read_FCS error occurs.
1	R/WC	0b	**Finish (FINISH)** 0: This bit is cleared by writing 1 to this position. 1: The bit is set by termination of a command.
0	R	0b	**Host Busy (HOBY)** 0: This bit is cleared when the current transaction is completed. 1: This bit is set while the command is in operation.

7.10.5.2 Host Control Register (HOCTLR)

Address Offset: Host: 01h (HHRAE = 0) / EC: 01h

Bit	R/W	Default	Description
7	R/W	0b	**Host Side High Range Address Enable (HHRAE)** This bit is only available in host side. 0: Host Side High Range Address is disabled. 1: Host Side High Range Address is enabled.
6	R/W	0b	**AW_FCS Force Control (AWFCS_FRC_CTRL)** This bit forces the AW_FCS hardwired mechanism no matter what PECI command (except the Ping() command) is issued. When this bit is set, the hardware will handle the calculation of AW_FCS. The programmer should set this bit based on the command to be issued. This bit will be cleared when the command is finished or aborted. 0: Disable 1: Enable

Bit	R/W	Default	Description
5	W	0b	**Data FIFO Pointer Clear (FIFOCLR)** Writing a 1 to this bit clears the Write/Read Data FIFO pointers. 0: No action; it always returns 0 when reading it. 1: Both Write and Read Data FIFO pointers will be cleared. Write Data pointer will point to Write Data 2, and Read Data pointer will point to Read Data 1.
4	R/W	0b	**PECI Host Auto-abort at FCS_Error (FCSERR_ABT)** This bit enables the PECI host to abort the transaction when FCS error occurs. 0: Disable 1: Enable
3	R/W	0b	**PECI Host Enable (PECIHEN)** This bit enables the PECI host controller. 0: Disable 1: Enable
2	R/W	0b	**PECI Contention Control (CONCTRL)** This bit enables the contention mechanism of the PECI bus. When this bit is set, the host will abort the transaction if the PECI bus is contentious. 0: Disable 1: Enable
1	R/W	0b	**Assured Write FCS Enable (AWFCS_EN)** This bit enables the AW_FCS hardwired mechanism based on the PECI command. This bit is functional only when the AW_FCS supported command of PECI 2.0/3.0/3.1 is issued. When this bit is set, the hardware will handle the calculation of AW_FCS. 0: Disable 1: Enable
0	W	0b	**Start (START)** This bit is write-only. Writing a 1 to it during the NOT Host Busy state will start a transaction. Writing a 1 to it during the Host Busy state will not issue any transaction. So, the programmer should check the Host Busy state before issuing a transaction. 0: This bit always returns 0 on reads. 1: When this bit is set, the PECI host controller will perform the desired transaction.

7.10.5.3 Host Command (Write Data 1) Register (HOCMDR)

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Command Register (HCMD[7:0])** This register is the command field of the PECI protocol. In the PECI protocol, it is the command (Write Data 1) byte. If the host controller is busy, the programmer should not change the value of this register, or the PECI host controller will send the wrong command. If the value of the register is out of definition, the host will transfer it as the normal value and no error will be detected by the PECI host controller.

7.10.5.4 Host Target Address Register (HOTRADDR)

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Target Address (HAddr[7:0])** This register is the Target Address field of the PECI protocol.

7.10.5.5 Host Write Length Register (HOWRLR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Write Length Register (HW_Length[7:0])** This register is the Write Length field of the PECI protocol.

7.10.5.6 Host Read Length Register (HORDLR)

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Read Length Register (HR_Length[7:0])** This register is the Read Length field of the PECI protocol.

7.10.5.7 Host Write Data (2-16) Register (HOWRDR)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	00h	**Write Data (2-16) (WR_DAT[7:0])** These are 15-byte FIFO registers, which are the Write Data field of the PECI protocol.

7.10.5.8 Host Read Data (1-16) Register (HORDDR)

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/W	00h	**Read Data (1-16) (RD_DAT[7:0])** These are 16-byte FIFO registers, which are the Read Data field of the PECI protocol.

7.10.5.9 Host Control 2 Register (HOCTL2R)

Address Offset: Host: 01h (HHRAE = 1) / EC: 08h

Bit	R/W	Default	Description
7	R/W	0b	**Host Side High Range Address Enable (HHRAE)** This bit is only available in host side. 0: Host Side High Range Address is disabled. 1: Host Side High Range Address is enabled.
6-3	-	-	**Reserved**
2-0	R/W	000b	**Host Optimal Transfer Rate Setting (HOPTTRS)** These bits are used to set PECI host's optimal transfer rate. 000b: 2MHz. 001b: 1MHz. 100b: 1.6MHz. Otherwise: Reserved

7.10.5.10 Pad Control Register (PADCTLR)

Address Offset: Host: 07h (HHRAE = 1) / EC: 0Eh

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4-3	R/W	00b	**Host V_{TT} Setting MSB (HOVTTSM)** These bits are used to set the PECI V_{TT} level. (Combined with VCMP2CSELM)
2	R/W	0b	**Data Valid Interrupt Enable (DVIE)** Enable to the PECI Interrupt generated by Data Valid event from PECI. This bit is only available in EC side. 0: Disabled (default). 1: Enable
1-0	R/W	00b	**Host V_{TT} Setting (HOVTTS)** These bits are used to set the PECI V_{TT} level. (Combined with HOVTTSM) { HOVTTSM, HOVTTS }: 0000b: 0.85V. 0001b: 0.90V. 0010b: 0.95V. 0011b: 1.00V. 0100b: 1.05V. 0101b: 1.10V. 0110b: 1.15V. 0111b: 1.20V. 1000b: 1.25V.

7.10.5.11 Received Write FCS Value (RWFCSV)

Address Offset: Host: 02h (HHRAE = 1) / EC: 09h

Bit	R/W	Default	Description
7-0	R	00b	**Received Write FCS Value (RWFCSV)** RWFCSV is used in storing the Write FCS generated by the PECI client. A new received Write FSC will automatically update this field.

7.10.5.12 Received Read FCS Value (RRFCSV)

Address Offset: Host: 03h (HHRAE = 1) / EC: 0Ah

Bit	R/W	Default	Description
7-0	R	00b	**Received Read FCS Value (RRFCSV)** RRFCSV is used in storing the Read FCS generated by the PECI client. A new received Read FSC will automatically update this field.

7.10.5.13 Write FCS Value (WFCSV)

Address Offset: Host: 04h (HHRAE = 1) / EC: 0Bh

Bit	R/W	Default	Description
7-0	R	00b	**Write FCS Value (WFCSV)** WFCSV is used in storing the Write FCS generated by EC. This field will be automatically updated while WRFCSV is updated.

7.10.5.14 Read FCS Value (RFCSV)

Address Offset: Host: 05h (HHRAE = 1) / EC: 0Ch

Bit	R/W	Default	Description
7-0	R	00b	**Read FCS Value (RFCSV)** RFCSV is used in storing the Read FCS generated by EC. This field will be automatically updated while RRFCSV is updated.

7.10.5.15 Assured Write FCS Value (AWFCSV)

Address Offset: Host: 06h (HHRAE = 1) / EC: 0Dh

Bit	R/W	Default	Description
7-0	R	00b	**Assured Write FCS Value (AWFCSV)** AWFCSV is used in storing the Assured Write FCS generated by EC. This field will be automatically updated while WRFCSV is updated.

7.11 Analog to Digital Converter (ADC)

7.11.1 Overview

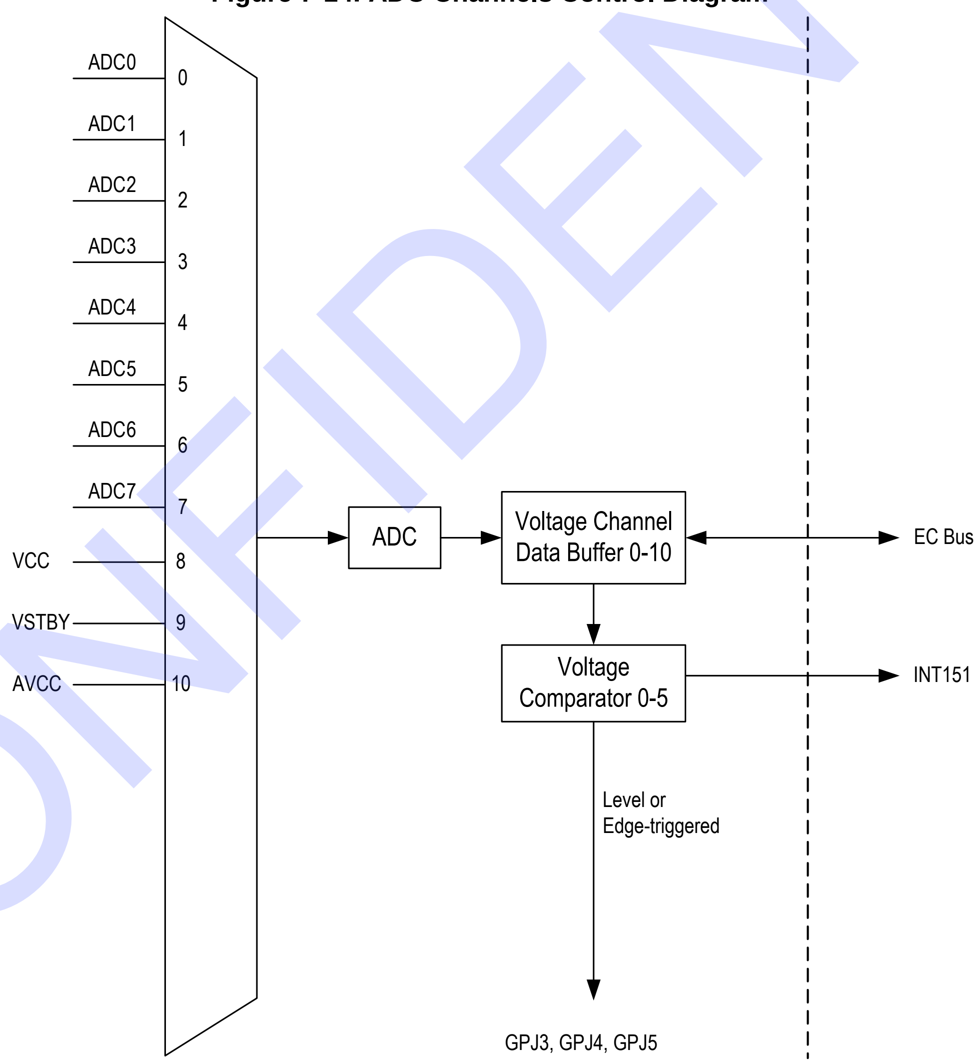
The ADC (analog to digital converter) provides an accurate method for measuring slow changing voltages. The module can measure the channel up to eleven-voltages with 10-bit resolution.

7.11.2 Features

- Supports 10-bit resolution and 0 to AVCC/1.1 or AVCC input voltage range
- Supports 11 voltage buffers
- Supports fast AD conversion of 11 channels
- Supports 6 voltage comparators, even EC in Sleep mode
- Polling or interrupt-driven interface

7.11.3 Functional Description

Figure 7-14. ADC Channels Control Diagram



7.11.3.1 ADC General Description

Inputs

The ADC has 11 inputs (ADC0-7, ADC8-10) divided into two groups described as the following:

• External Voltage (ADC0-7):

These are for DC voltage sources.

• Internal Voltage (ADC8-10):

These are connected to the internal supply voltages of the device (VCC, VSTBY and AVCC).

A/D Converter

The high-resolution A/D converter receives the selected input with a 11 to 1 analog multiplier and converts it. The result of the conversion is a 10-bit unsigned integer.

ADC Cycle

The ADC has 11 output buffers, which are for the voltage channel. The buffer for voltage measurement channels holds the current data until the next same volt channel measurement is completed after one ADC cycle is finished. An ADC cycle includes measurements of all active channels. If all 11 channels are enabled, the first measurement is a voltage channel 0 and followed by voltage channel 1, 2, 3, … 10. After an A/D conversion is completed for a certain active channel, its related bit in the Data Valid (DATVAL bit in VCH0CTL - VCH7CTL) flag is set, which represents the channel of data is available and EC can read out.

Channel Conversion Time

The channel conversion time of ADC is listed bellow.

Table 7-17. ADC Channel Conversion Time

{ADCCTS1, ADCCTS0}	= 11b	= 01b	= 00b or 10b
Conversion Time (μs)	200*(SCLKDIV + 1)	103.2*(SCLKDIV + 1)	30.8*(SCLKDIV + 1)

Interrupt to INTC

ADC interrupt (INT8) will be active if end-of-cycle or voltage channel 0-7 data valid is true. See also INTECEN and INTDVEN.

The voltage comparator interrupt (INT151) will be active if the value stored in the selected voltage channel data buffer reaches the threshold level of the comparator.

7.11.3.2 Voltage Measurement and Automatic Hardware Calibration

The ADC converts the input voltage signal ranging from 0V to AVCC/1.1 or AVCC into a 10-bit unsigned integer. This 10-bit integer then will be stored in data buffer VCHiDATL and VCHiDATM.

Changing the input selection for a new measurement channel (voltage), the software needs to set a delay time to prevent the result of an unintended ADC operation. The ADC waits for a programmable delay time between the selection of the input to be measured and the beginning of the A/D conversion.

7.11.3.3 ADC Operation

Reset
The ADC is disabled, and all interrupt is masked and all event status bits are reset. The selected input for all four-voltage channels is disabled (Bit4-0 of the VCHiCTL register is set to 0Fh).

Initializing the ADC
The ADC has to be initialized before ADC is enabled (ADCEN in the ADCCFG register is set to 1). The followings need to be done before the ADC is enabled.
1. Set AINITB@ADCSTS = 1 then clear it (only once after VSTBY power on)
2. Channel Select in VCHiCTL register
3. ADCEN bit in ADCCFG register is cleared.

Enabling the ADC
After the ADC is enabled, the voltage channel is measured as long as the ADCEN is set 1 and when the voltage channel is selected. The measurement operations may be enabled or disabled individually.

Disabling the ADC
ADC analog circuit has less power consumption if it is disabled. ADCEN bit in ADCCFG register controls this and it’s cleared at EC Domain Reset.

The firmware should clear ADCEN bit before entering Doze/Deep Doze/Sleep mode.

7.11.4 EC Interface Registers

The ADC control/status and data out registers set interfaces with the EC through the EC Dedicated bus. These registers are mapped in the address space of the EC. The registers are listed below and the base address is 1900h.

Table 7-18. EC View Register Map, ADC

7 0	Offset
ADC Status Register (ADCSTS)	00h
ADC Configuration Register (ADCCFG)	01h
ADC Clock Control Register (ADCCTL)	02h
ADC General Control Register (ADCGCR)	03h
Voltage Channel 0 Control Register (VCH0CTL)	04h
Calibration Data Control Register (KDCTL)	05h
Voltage Channel 1 Control Register (VCH1CTL)	06h
Voltage Channel 1 Data Buffer LSB (VCH1DATL)	07h
Voltage Channel 1 Data Buffer MSB (VCH1DATM)	08h
Voltage Channel 2 Control Register (VCH2CTL)	09h
Voltage Channel 2 Data Buffer LSB (VCH2DATL)	0Ah
Voltage Channel 2 Data Buffer MSB (VCH2DATM)	0Bh
Voltage Channel 3 Control Register (VCH3CTL)	0Ch
Voltage Channel 3 Data Buffer LSB (VCH3DATL)	0Dh
Voltage Channel 3 Data Buffer MSB (VCH3DATM)	0Eh
Voltage Channel 0 Data Buffer LSB (VCH0DATL)	18h
Voltage Channel 0 Data Buffer MSB (VCH0DATM)	19h
Voltage Comparator Scan Period (VCMPSCP)	37h
Voltage Channel 4 Control Register (VCH4CTL)	38h
Voltage Channel 4 Data Buffer MSB (VCH4DATM)	39h
Voltage Channel 4 Data Buffer LSB (VCH4DATL)	3Ah
Voltage Channel 5 Control Register (VCH5CTL)	3Bh
Voltage Channel 5 Data Buffer MSB (VCH5DATM)	3Ch
Voltage Channel 5 Data Buffer LSB (VCH5DATL)	3Dh

7 ... 0	Offset
Voltage Channel 6 Control Register (VCH6CTL)	3Eh
Voltage Channel 6 Data Buffer MSB (VCH6DATM)	3Fh
Voltage Channel 6 Data Buffer LSB (VCH6DATL)	40h
Voltage Channel 7 Control Register (VCH7CTL)	41h
Voltage Channel 7 Data Buffer MSB (VCH7DATM)	42h
Voltage Channel 7 Data Buffer LSB (VCH7DATL)	43h
ADC Data Valid Status (ADCDVSTS)	44h
Voltage Comparator Status (VCMPSTS)	45h
Voltage Comparator 0 Control Register (VCMP0CTL)	46h
Voltage Comparator 0 Threshold Data Buffer MSB (VCMP0THRDATM)	47h
Voltage Comparator 0 Threshold Data Buffer LSB (VCMP0THRDATL)	48h
Voltage Comparator 1 Control Register (VCMP1CTL)	49h
Voltage Comparator 1 Threshold Data Buffer MSB (VCMP1THRDATM)	4Ah
Voltage Comparator 1 Threshold Data Buffer LSB (VCMP1THRDATL)	4Bh
Voltage Comparator 2 Control Register (VCMP2CTL)	4Ch
Voltage Comparator 2 Threshold Data Buffer MSB (VCMP2THRDATM)	4Dh
Voltage Comparator 2 Threshold Data Buffer LSB (VCMP2THRDATL)	4Eh
Voltage Comparator Output Type Register (VCMPOTR)	4Fh
Voltage Comparator 0 Hysteresis Data Buffer MSB (VCMP0HYDATM)	50h
Voltage Comparator 0 Hysteresis Data Buffer LSB (VCMP0HYDATL)	51h
Voltage Comparator Lock Register (VCMPLR)	52h
ADC Input Voltage Mapping Full-Scale Code Selection 1 (ADCIVMFSCS1)	55h
ADC Input Voltage Mapping Full-Scale Code Selection 2 (ADCIVMFSCS2)	56h
Voltage Comparator Status 2 (VCMPSTS2) (for channel 3~5)	6Dh
Voltage Comparator 3 Control Register (VCMP3CTL)	6Eh
Voltage Comparator 3 Threshold Data Buffer MSB (VCMP3THRDATM)	6Fh
Voltage Comparator 3 Threshold Data Buffer LSB (VCMP3THRDATL)	70h
Voltage Comparator 4 Control Register (VCMP4CTL)	71h
Voltage Comparator 4 Threshold Data Buffer MSB (VCMP4THRDATM)	72h
Voltage Comparator 4 Threshold Data Buffer LSB (VCMP4THRDATL)	73h
Voltage Comparator 5 Control Register (VCMP5CTL)	74h
Voltage Comparator 5 Threshold Data Buffer MSB (VCMP5THRDATM)	75h
Voltage Comparator 5 Threshold Data Buffer LSB (VCMP5THRDATL)	76h
Voltage Comparator 0 Channel Select MSB (VCMP0CSELM)	77h
Voltage Comparator 1 Channel Select MSB (VCMP1CSELM)	78h
Voltage Comparator 2 Channel Select MSB (VCMP2CSELM)	79h
Voltage Comparator 3 Channel Select MSB (VCMP3CSELM)	7Ah
Voltage Comparator 4 Channel Select MSB (VCMP4CSELM)	7Bh
Voltage Comparator 5 Channel Select MSB (VCMP5CSELM)	7Ch

For a summary of the abbreviations used for register type, see “Register Abbreviations and Access Rules”

7.11.4.1 ADC Status Register (ADCSTS)

This register indicates the global status of the ADC module. ADCSTS is cleared (00h) on VSTBY Power-Up reset; on other resets, bit 2 is unchanged and other bits are cleared.

Address Offset: 00h

Bit	R/W	Default	Description
7	-	1b	**ADC Conversion Time Select 1 (ADCCTS1)** Change this bit to increase or decrease the ADC conversion time.
6	-	0b	**Reserved**

Bit	R/W	Default	Description
5	R/W	0b	**Clock Source Select (SDIVSRC)** This bit provides selection of the clock source of ADC clock. See also SCLKDIV field in ADCCTL register. 0: Select EC Clock (frequency = FreqEC) 1: Select PLL Clock (frequency = FreqPLL) FreqPLL/FreqEC is listed in Table 10-2 on page 570.
4	-	0b	**Reserved**
3	R/W	0b	**Analog Accuracy Initialization Bit (AINITB)** Write 1 to this bit and write 0 to this bit immediately once and only once during the firmware initialization and do not write 1 again after initialization since IT81202 takes much power consumption if this bit is set as 1. Writing steps about this bit should be done before ADCEN bit is set in ADCCFG register. 1: Start ADC accuracy initialization. 0: Stop ADC accuracy initialization.
2	R/W	0b	**ADC Power Statement (ADCPS)** This bit remains zero when ADC power is in a normal state. When ADC power shuts down or failure occurs, the software must program this bit to one. The program has to be waited at least 200usec for ADC internal initialization after power on. 0: Indicate the ADC power in a normal state. 1: Indicate the ADC power in a shut-down or failure state.
1	R/WC	0b	**Data Overflow Event (DOVE)** Measurement data from the previous cycle was overwritten with data From the current cycle before being read. In the event of a data overflow, the DATVAL bit remains set and new data is placed in Channel Data Buffer register. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No overflow (default) 1: Overflow
0	R/WC	0b	**End-of-Cycle Event (EOCE)** End of ADC cycle; all enabled measurements (up to four) are completed. For each of the enabled channels, the DATVAL bit is set to 1 and the data stored in Channel Data Buffer register respectively. 0: Cycle in progress (default) 1: End of ADC cycle

7.11.4.2 ADC Configuration Register (ADCCFG)

This register controls the operation and global configuration of the ADC module.

Address Offset: 01h

Bit	R/W	Default	Description
7-6		10b	**Reserved**
5	-	0b	**ADC Conversion Time Select 0 (ADCCTS0)** Change this bit to increase or decrease the ADC conversion time.
4-3	-	-	**Reserved**
2	R/W	0b	**Interrupt from End-of-Cycle Event Enable (INTECEN)** This bit enables an ADC interrupt generated by End-of ADC-cycle event (EOCE in ADCSTS register). 0: Disabled (Default) 1: Enabled interrupt by EOCE event

Bit	R/W	Default	Description
1	R/W	0b	**Reserved**
0	R/W	0b	**ADC Module Enable (ADCEN)** Controls ADC operation or not 0: ADC disabled (default), power-down 1: ADC enabled

7.11.4.3 ADC Clock Control Register (ADCCTL)

This register controls the EC clock to ADC clock division.

Address Offset: 02h

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-0	R/W	15h	**Select Clock Division Factor (SCLKDIV)** This field is used in selecting the divisor for the ADC clock divider. **Note:** SCLKDIV has to be equal to or greater than 1h.

7.11.4.4 ADC General Control Register (ADCGCR)

This register controls the ADC Data kept in VCHxDATL/VCHxDATM.

Address Offset: 03h

Bit	R/W	Default	Description
7	R/W	0b	**ADC Data Buffer Keep Enable (ADCDBKEN)** Enable this bit, and VCHxDATL/VCHxDATM will be kept until DATVAL is cleared (write 1 clear) especially for that conversion time is short. 0: Disabled (default). 1: Enable
6-3	-	-	**Reserved**
2-0	R/W	2h	**Reserved** **Note**: Do not modify this default value.

7.11.4.5 Voltage Channel 0 Control Register (VCH0CTL)

This register controls the operation as well as indicates the status of the Voltage channel.

Address Offset: 04h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The VCH0DATL/VCH0DATM is available for reading when DATVAL is set. This bit is cleared when the ADC module is disabled (ADCEN in ADCCFG register is cleared) or by writing 1 to it. 0: No valid data in VCH0DATL/VCH0DATM register (Default) 1: End of conversion – new data is available in VCH0DATL/VCH0DATM
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt generated by Data valid event of voltage channel 0. 0: Disabled (Default) 1: Enabled – ADC Interrupt from local DATVAL

Bit	R/W	Default	Description
4-0	R/W	11111b	**Selected Input (SELIN)** Indicates which Volt channel input is selected for measurement. The channel selection has to be programmed before the channel is measured. **Bits** 43210 Description 00000: Channel 0 00001: Channel 1 .... 01010: Channel 10 Others: Reserved 11111: Channel Disabled (Default)

7.11.4.6 Calibration Data Control Register (KDCTL)

This register controls the operation as well as indicates the status of the Calibration channel.

Address Offset: 05h

B it	R/W	Default	Description
7	R/W	0b	**Automatic Hardware Calibration Enable(AHCE)** 0: Disable automatic hardware calibration. 1: Enable automatic hardware calibration.
6-0	-	0000000b	**Reserved**

7.11.4.7 Voltage Channel 1 Control Register (VCH1CTL)

This register controls the operation as well as indicates the status of voltage channel 1.

Address Offset: 06h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH1DATL/VCH1DATM register (Default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 1. 0: Disabled (Default) 1: Enabled – ADC Interrupt from local DATVAL
4-0	R/W	11111b	**Selected Input (SELIN)** Indicates which Volt channel input is selected for measurement. Channel selected has to be done before beginning to measure the channel. **Bits** 4 3 2 1 0 Description 0 0 0 0 0: Channel 0 0 0 0 0 1: Channel 1 .... 0 1 0 1 0: Channel 10 Others: Reserved 1 1 1 1 1: Channel Disabled (Default)

7.11.4.8 Voltage Channel 1 Data Buffer LSB (VCH1DATL)

This register (buffer) holds the data(LSB 8bits) measured by the volt channel 1.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** The data of the volt channel is measured by the volt channel 1. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.9 Voltage Channel 1 Data Buffer MSB (VCH1DATM)

This register (buffer) holds the data(MSB 6bits) measured by the volt channel 1.

Address Offset: 08h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** The data of the volt channel is measured by the volt channel 1. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.10 Voltage Channel 2 Control Register (VCH2CTL)

This register controls the operation as well as indicates the status of voltage channel 2.

Address Offset: 09h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The same as Volt channel 1.
6	R/W	0b	**Reserved** The same as Volt channel 1.
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** The same as Volt channel 1.
4-0	R/W	11111b	**Selected Input (SELIN)** The same as Volt channel 1.

7.11.4.11 Voltage Channel 2 Data Buffer LSB (VCH2DATL)

This register (buffer) holds the data(LSB 8bits) measured by the volt channel 2.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** The data of the volt channel is measured by the volt channel 2. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.12 Voltage Channel 2 Data Buffer MSB (VCH2DATM)

This register (buffer) holds the data(MSB 6bits) measured by the volt channel 2.

Address Offset: 0Bh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** The data of the volt channel is measured by the volt channel 2. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.13 Voltage Channel 3 Control Register (VCH3CTL)

This register controls the operation as well as indicates the status of voltage channel 3.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The same as Volt channel 1.
6	R/W	0b	**Reserved** The same as Volt channel 1.
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** The same as Volt channel 1.
4-0	R/W	11111b	**Selected Input (SELIN)** The same as Volt channel 1.

7.11.4.14 Voltage Channel 3 Data Buffer LSB (VCH3DATL)

This register (buffer) holds the data(LSB 8bits) measured by the volt channel 3.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** The data of the volt channel is measured by the volt channel 3. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.15 Voltage Channel 3 Data Buffer MSB (VCH3DATM)

This register (buffer) holds the data(MSB 6bits) measured by the volt channel 3.

Address Offset: 0Eh

Bit	R/W	Default	Description
7-2		-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** The data of the volt channel is measured by the volt channel 3. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.16 Voltage Channel 0 Data Buffer LSB (VCH0DATL)

This register (buffer) holds the data (LSB 7-0) measured by the voltage channel 0.

Address Offset: 18h

Bit	R/W	Default	Description
7-0	R	-	**Voltage Channel Data (VCHDAT7-0)** The data of the volt channel is measured by the volt channel 0. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.17 Voltage Channel 0 Data Buffer MSB (VCH0DATM)

This register (buffer) holds the data (MSB 6 bits) measured by the voltage channel 0.

Address Offset: 19h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R	-	**Voltage Channel Data (VCHDAT9-8)** The data of the volt channel is measured by the volt channel 0. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.18 Voltage Comparator Scan Period (VCMPSCP)

This register defines the scan period of Voltage Comparator 0 ~ 2.

Address Offset: 37h

Bit	R/W	Default	Description
7-4	R/W	0110b	**Comparator 0/1/2 Scan Period (CMPSNP)** 0001b: 100 uS 0010b: 200 uS 0011b: 400 uS 0100b: 600 uS 0101b: 800 uS 0110b: 1mS 0111b: 1.5 mS 1000b: 2 mS 1001b: 2.5 mS 1010b: 3 mS 1011b: 4 mS 1100b: 5 mS
3-0	-	-	**Reserved**

7.11.4.19 Voltage Channel 4 Control Register (VCH4CTL)

This register controls the operation as well as indicates the status of voltage channel 4.

Address Offset: 38h

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH4DATL/VCH4DATM register (Default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 4. 0: Disabled (Default) 1: Enabled – ADC Interrupt from local DATVAL
4	R/W	0b	**Voltage Channel Enable (VCHEN)** **Note:** Only for ADC input channel 4 0: Disabled (Default) 1: Enabled
3-0	R/W	0000b	**Reserved**

7.11.4.20 Voltage Channel 4 Data Buffer MSB (VCH4DATM)

This register (buffer) holds the data(MSB 2bits) measured by the volt channel 4.

Address Offset: 39h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** The data of the volt channel is measured by the volt channel 4. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.21 Voltage Channel 4 Data Buffer LSB (VCH4DATL)

This register (buffer) holds the data(LSB 8bits) measured by the volt channel 4.

Address Offset: 3Ah

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** The data of the volt channel is measured by the volt channel 4. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.22 Voltage Channel 5 Control Register (VCH5CTL)

This register controls the operation as well as indicates the status of voltage channel 5.

Address Offset: 3Bh

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH5DATL/VCH5DATM register (Default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**

Bit	R/W	Default	Description
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 5. 0: Disabled (Default) 1: Enabled – ADC Interrupt from local DATVAL
4	R/W	0b	**Voltage Channel Enable (VCHEN)** **Note:** Only for ADC input channel 5 0: Disabled (Default) 1: Enabled
3-0	R/W	0000b	**Reserved**

7.11.4.23 Voltage Channel 5 Data Buffer MSB (VCH5DATM)

This register (buffer) holds the data(MSB 2bits) measured by the volt channel 5.

Address Offset: 3Ch

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** The data of the volt channel is measured by the volt channel 5. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.24 Voltage Channel 5 Data Buffer LSB (VCH5DATL)

This register (buffer) holds the data(LSB 8bits) measured by the volt channel 5.

Address Offset: 3Dh

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0**) The data of the volt channel is measured by the volt channel 5. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.25 Voltage Channel 6 Control Register (VCH6CTL)

This register controls the operation as well as indicates the status of voltage channel 6.

Address Offset: 3Eh

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH6DATL/VCH6DATM register (Default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 6. 0: Disabled (Default) 1: Enabled – ADC Interrupt from local DATVAL

Bit	R/W	Default	Description
4	R/W	0b	**Voltage Channel Enable (VCHEN)** **Note:** Only for ADC input channel 6 0: Disabled (Default) 1: Enabled
3-0	R/W	0000b	**Reserved**

7.11.4.26 Voltage Channel 6 Data Buffer MSB (VCH6DATM)

This register (buffer) holds the data(MSB 2bits) measured by the volt channel 6.

Address Offset: 3Fh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** The data of the volt channel is measured by the volt channel 6. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.27 Voltage Channel 6 Data Buffer LSB (VCH6DATL)

This register (buffer) holds the data(LSB 8bits) measured by the volt channel 6.

Address Offset: 40h

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** The data of the volt channel is measured by the volt channel 6. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.28 Voltage Channel 7 Control Register (VCH7CTL)

This register controls the operation as well as indicates the status of voltage channel 7.

Address Offset: 41h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH7DATL/VCH7DATM register (Default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 7. 0: Disabled (Default) 1: Enabled – ADC Interrupt from local DATVAL
4	R/W	0b	**Voltage Channel Enable (VCHEN)** **Note:** Only for ADC input channel 7 0: Disabled (Default) 1: Enabled
3-0	R/W	0000b	**Reserved**

7.11.4.29 Voltage Channel 7 Data Buffer MSB (VCH7DATM)

This register (buffer) holds the data(MSB 2bits) measured by the volt channel 7.

Address Offset: 42h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** The data of the volt channel is measured by the volt channel 7. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.30 Voltage Channel 7 Data Buffer LSB (VCH7DATL)

This register (buffer) holds the data(LSB 8bits) measured by the volt channel 7.

Address Offset: 43h

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** The data of the volt channel is measured by the volt channel 7. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.31 ADC Data Valid Status (ADCDVSTS)

This register indicates the data valid status of Voltage Channel 0 ~ 7.

Address Offset: 44h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid of Channel 7 (DAT7VAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH7DATL/VCH7DATM register (Default) 1: End of conversion – New data is available. **Note**: The same as DATVAL in VCH7CTL
6	R/WC	0b	**Data Valid of Channel 6 (DAT6VAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH6DATL/VCH6DATM register (Default) 1: End of conversion – New data is available. **Note**: The same as DATVAL in VCH6CTL
5	R/WC	0b	**Data Valid of Channel 5 (DAT5VAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH5DATL/VCH5DATM register (Default) 1: End of conversion – New data is available. **Note**: The same as DATVAL in VCH5CTL
4	R/WC	0b	**Data Valid of Channel 4 (DAT4VAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH4DATL/VCH4DATM register (Default) 1: End of conversion – New data is available. **Note**: The same as DATVAL in VCH4CTL

Bit	R/W	Default	Description
3	R/WC	0b	**Data Valid of Channel 3 (DAT3VAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH3DATL/VCH3DATM register (Default) 1: End of conversion – New data is available. **Note**: The same as DATVAL in VCH3CTL
2	R/WC	0b	**Data Valid of Channel 2 (DAT2VAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH2DATL/VCH2DATM register (Default) 1: End of conversion – New data is available. **Note**: The same as DATVAL in VCH2CTL
1	R/WC	0b	**Data Valid of Channel 1 (DAT1VAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH1DATL/VCH1DATM register (Default) 1: End of conversion – New data is available. **Note**: The same as DATVAL in VCH1CTL
0	R/WC	0b	**Data Valid of Channel 0 (DAT0VAL)** The data may be read immediately when this bit is set to 1. This bit can be cleared by disabling the ADC module or writing 1 to it. 0: No valid data in VCH0DATL/VCH0DATM register (Default) 1: End of conversion – New data is available. **Note**: The same as DATVAL in VCH0CTL

7.11.4.32 Voltage Comparator Status (VCMPSTS)

This register indicates the status of Voltage Comparator 0 - 2.

Address Offset: 45h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/WC	0b	**Comparator 2 Reach Threshold Status (CMP2RTS)** This bit indicates the GPIO(GPJ5) status of comparator 2 reach voltage threshold. This bit is cleared when writing 1 to it. If CMP2GPOL is set to 0b (active-high), 0: Not reach the voltage threshold 1: Reach the voltage threshold. If CMP2GPOL is set to 1b (active-low), 0: Reach the voltage threshold 1: Not reach the voltage threshold

Bit	R/W	Default	Description
5	R/WC	0b	**Comparator 1 Reach Threshold Status (CMP1RTS)** This bit indicates the GPIO(GPJ4) status of comparator 1 reach voltage threshold. This bit is cleared when writing 1 to it. If CMP1GPOL is set to 0b (active-high), 0: Not reach the voltage threshold 1: Reach the voltage threshold. If CMP1GPOL is set to 1b (active-low), 0: Reach the voltage threshold 1: Not reach the voltage threshold
4	R/WC	0b	**Comparator 0 Reach Threshold Status (CMP0RTS)** This bit indicates the GPIO(GPJ3) status of comparator 0 reach voltage threshold. This bit is cleared when writing 1 to it. If CMP0GPOL is set to 0b (active-high), 0: Not reach the voltage threshold 1: Reach the voltage threshold. If CMP0GPOL is set to 1b (active-low), 0: Reach the voltage threshold 1: Not reach the voltage threshold
3	-	-	**Reserved**
2	R/WC	0b	**Comparator 2 Reach Threshold Interrupt Status (CMP2RTIS)** This bit indicates the interrupt status of comparator 2 reach voltage threshold. This bit is cleared when writing 1 to it. 0: Not reach the voltage threshold 1: Reach the voltage threshold.
1	R/WC	0b	**Comparator 1 Reach Threshold Interrupt Status (CMP1RTIS)** This bit indicates the interrupt status of comparator 1 reach voltage threshold. This bit is cleared when writing 1 to it. 0: Not reach the voltage threshold 1: Reach the voltage threshold.
0	R/WC	0b	**Comparator 0 Reach Threshold Interrupt Status (CMP0RTIS)** This bit indicates the interrupt status of comparator 0 reach voltage threshold. This bit is cleared when writing 1 to it. 0: Not reach the voltage threshold 1: Reach the voltage threshold.

7.11.4.33 Voltage Comparator 0 Control Register (VCMP0CTL)

This register controls the operation of voltage comparator 0.

Address Offset: 46h

Bit	R/W	Default	Description
7	R/W	0b	**Comparator 0 Enable (CMP0EN)** 0: Disable 1: Enable
6	R/W	0b	**Comparator 0 Interrupt Enable (CMP0INTEN)** 0: Disabled 1: Enabled

Bit	R/W	Default	Description
5	R/W	0b	**Comparator 0 Trigger Mode (CMP0TMOD)** This bit is to select the trigger condition. 0: Less then or equal to CMP0THRDAT [9:0] 1: Greater then CMP0THRDAT [9:0]
4	R/W	0b	**Comparator 0 Edge/Level Sense Mode (CMP0ELSM)** This bit determines the sensed mode of the comparator 0. 0: Level-sensed 1: Edge-sensed
3	R/W	0b	**Comparator 0 GPIO Polarity (CMP0GPOL)** This bit determines the GPIO(GPJ3) active high/low of the comparator 0. 0: Active-high 1: Active-low
2-0	R/W	000b	**Comparator 0 Channel Select LSB (CMP0CSELL)** These bits are to select the ADC channel for the comparator 0. (Combined with VCMP0CSELM) 0000b: ADC0 0001b: ADC1 0010b: ADC2 0011b: ADC3 0100b: ADC4 0101b: ADC5 0110b: ADC6 0111b: ADC7

7.11.4.34 Voltage Comparator 0 Threshold Data Buffer MSB (VCMP0THRDATM)

Address Offset: 47h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 0 Threshold Data (CMP0THRDAT9-8)** The MSB (2 Bits) of CMP0THRDAT.

7.11.4.35 Voltage Comparator 0 Threshold Data Buffer LSB (VCMP0THRDATL)

Address Offset: 48h

Bit	R/W	Default	Description
7-0	R/W	00h	**Comparator 0 Threshold Data (CMP0THRDAT7-0)** The LSB (8 Bits) of CMP0THRDAT.

7.11.4.36 Voltage Comparator 1 Control Register (VCMP1CTL)

This register controls the operation of voltage comparator 1.

Address Offset: 49h

Bit	R/W	Default	Description
7	R/W	0b	**Comparator 1 Enable (CMP1EN)** 0: Disable 1: Enable
6	R/W	0b	**Comparator 1 Interrupt Enable (CMP1INTEN)** 0: Disable 1: Enable

Bit	R/W	Default	Description
5	R/W	0b	**Comparator 1 Trigger Mode (CMP1TMOD)** This bit is to select the trigger condition. 0: Less then or equal to CMP1THRDAT [9:0] 1: Greater then CMP1THRDAT [9:0]
4	R/W	0b	**Comparator 1 Edge/Level Sense Mode (CMP1ELSM)** This bit determines the sensed mode of the comparator 1. 0: Level-sensed 1: Edge-sensed
3	R/W	0b	**Comparator 1 GPIO Polarity (CMP1GPOL)** This bit determines the GPIO(GPJ4) active high/low of the comparator 1. 0: Active-high 1: Active-low
2-0	R/W	000b	**Comparator 1 Channel Select LSB (CMP1CSELL)** These bits are to select the ADC channel for the comparator 1. (Combined with VCMP1CSELM) 0000b: ADC0 0001b: ADC1 0010b: ADC2 0011b: ADC3 0100b: ADC4 0101b: ADC5 0110b: ADC6 0111b: ADC7

7.11.4.37 Voltage Comparator 1 Threshold Data Buffer MSB (VCMP1THRDATM)

Address Offset: 4Ah

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 1 Threshold Data (CMP1THRDAT9-8)** The MSB (2 Bits) of CMP1THRDAT.

7.11.4.38 Voltage Comparator 1 Threshold Data Buffer LSB (VCMP1THRDATL)

Address Offset: 4Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Comparator 1 Threshold Data (CMP1THRDAT7-0)** The LSB (8 Bits) of CMP1THRDAT.

7.11.4.39 Voltage Comparator 2 Control Register (VCMP2CTL)

This register controls the operation of voltage comparator 2.

Address Offset: 4Ch

Bit	R/W	Default	Description
7	R/W	0b	**Comparator 2 Enable (CMP2EN)** 0: Disable 1: Enable
6	R/W	0b	**Comparator 2 Interrupt Enable (CMP2INTEN)** 0: Disable 1: Enable

Bit	R/W	Default	Description
5	R/W	0b	**Comparator 2 Trigger Mode (CMP2TMOD)** This bit is to select the trigger condition. 0: Less then or equal to CMP2THRDAT [9:0] 1: Greater than CMP2THRDAT [9:0]
4	R/W	0b	**Comparator 2 Edge/Level Sense Mode (CMP2ELSM)** This bit determines the sensed mode of the comparator 1. 0: Level-sensed 1: Edge-sensed
3	R/W	0b	**Comparator 2 GPIO Polarity (CMP2GPOL)** This bit determines the GPIO(GPJ5) active high/low of the comparator 2. 0: Active-high 1: Active-low
2-0	R/W	000b	**Comparator 2 Channel Select LSB (CMP2CSELL)** These bits are to select the ADC channel for the comparator 2. (Combined with VCMP2CSELM) 0000b: ADC0 0001b: ADC1 0010b: ADC2 0011b: ADC3 0100b: ADC4 0101b: ADC5 0110b: ADC6 0111b: ADC7

7.11.4.40 Voltage Comparator 2 Threshold Data Buffer MSB (VCMP2THRDATM)

Address Offset: 4Dh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 2 Threshold Data (CMP2THRDAT9-8)** The MSB (2 Bits) of CMP2THRDAT.

7.11.4.41 Voltage Comparator 2 Threshold Data Buffer LSB (VCMP2THRDATL)

Address Offset: 4Eh

Bit	R/W	Default	Description
7-0	R/W	00b	**Comparator 2 Threshold Data (CMP2THRDAT7-0)** The LSB (8 Bits) of CMP2THRDAT.

7.11.4.42 Voltage Comparator Output Type Register (VCMPOTR)

Address Offset: 4Fh

Bit	R/W	Default	Description
7	R/W	0b	**Comparator 5 Output Type (CMP5OT)** This bit determines the output type of the comparator 5. 0: Push-pull 1: Open-drain
6	R/W	0b	**Comparator 4 Output Type (CMP4OT)** This bit determines the output type of the comparator 4. 0: Push-pull 1: Open-drain

Bit	R/W	Default	Description
5	R/W	0b	**Comparator 3 Output Type (CMP3OT)** This bit determines the output type of the comparator 3. 0: Push-pull 1: Open-drain
4	R/W	0b	**Comparator 0 Hysteresis Enable (CMP0HYSEN)** Hysteresis enable of comparator 0. 0: Disable 1: Enable
3	R/W	0b	**Reserved**
2	R/W	0b	**Comparator 2 Output Type (CMP2OT)** This bit determines the output type of the comparator 2. 0: Push-pull 1: Open-drain
1	R/W	0b	**Comparator 1 Output Type (CMP1OT)** This bit determines the output type of the comparator 1. 0: Push-pull 1: Open-drain
0	R/W	0b	**Comparator 0 Output Type (CMP0OT)** This bit determines the output type of the comparator 0. 0: Push-pull 1: Open-drain

7.11.4.43 Voltage Comparator 0 Hysteresis Data Buffer MSB (VCMP0HYDATM)

Address Offset: 50h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 0 Hysteresis Data (CMP0HYDAT9-8)** The MSB (2 Bits) of CMP0HYDAT.

7.11.4.44 Voltage Comparator 0 Hysteresis Data Buffer LSB (VCMP0HYDATL)

Address Offset: 51h

Bit	R/W	Default	Description
7-0	R/W	00b	**Comparator 0 Hysteresis Data (CMP0HYDAT7-0)** The LSB (8 Bits) of CMP0HYDAT.

7.11.4.45 Voltage Comparator Lock Register (VCMPLR)

This register lock the control register of the voltage comparator.

Address Offset: 52h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**Comparator 5 Lock Enable (CMP5LE)** Lock the control register of the comparator 5 (except CMP5INTEN). 0: Disable 1: Enable Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.

Bit	R/W	Default	Description
4	R/W	0b	**Comparator 4 Lock Enable (CMP4LE)** Lock the control register of the comparator 4 (except CMP4INTEN). 0: Disable 1: Enable Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.
3	R/W	0b	**Comparator 3 Lock Enable (CMP3LE)** Lock the control register of the comparator 3 (except CMP3INTEN). 0: Disable 1: Enable Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.
2	R/W	0b	**Comparator 2 Lock Enable (CMP2LE)** Lock the control register of the comparator 2 (except CMP2INTEN). 0: Disable 1: Enable Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.
1	R/W	0b	**Comparator 1 Lock Enable (CMP1LE)** Lock the control register of the comparator 1 (except CMP1INTEN). 0: Disable 1: Enable Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.
0	R/W	0b	**Comparator 0 Lock Enable (CMP0LE)** Lock the control register of the comparator 0 (except CMP0INTEN). 0: Disable 1: Enable Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.

7.11.4.46 ADC Input Voltage Mapping Full-Scale Code Selection 1 (ADCIVMFSCS1)

This register controls ADC Full-Scale code.

Address Offset: 55h

Bit	R/W	Default	Description
7	R/W	0b	**Channel7 Select Full-Scale Code (C7SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.
6	R/W	0b	**Channel6 Select Full-Scale Code (C6SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.
5	R/W	0b	**Channel5 Select Full-Scale Code (C5SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.
4	R/W	0b	**Channel4 Select Full-Scale Code (C4SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.

Bit	R/W	Default	Description
3	R/W	0b	**Channel3 Select Full-Scale Code (C3SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.
2	R/W	0b	**Channel2 Select Full-Scale Code (C2SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.
1	R/W	0b	**Channel1 Select Full-Scale Code (C1SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.
0	R/W	0b	**Channel0 Select Full-Scale Code (C0SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.

7.11.4.47 ADC Input Voltage Mapping Full-Scale Code Selection 2 (ADCIVMFSCS2)

This register controls ADC Full-Scale code.

Address Offset: 56h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**Channel10 Select Full-Scale Code (C10SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.
1	R/W	0b	**Channel9 Select Full-Scale Code (C9SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.
0	R/W	0b	**Channel8 Select Full-Scale Code (C8SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped into 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped into 0h-3FFh.

7.11.4.48 Voltage Comparator Status 2 (VCMPSTS2)

This register indicates the status of Voltage Comparator 3 - 5.

Address Offset: 6Dh

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/WC	0b	**Comparator 5 Reach Threshold Status (CMP5RTS)** This bit indicates the status of comparator 5 reach voltage threshold. This bit is cleared when writing 1 to it. If CMP5GPOL is set to 0b (active-high), 0: Not reach the voltage threshold 1: Reach the voltage threshold. If CMP5GPOL is set to 1b (active-low), 0: Reach the voltage threshold 1: Not reach the voltage threshold
5	R/WC	0b	**Comparator 4 Reach Threshold Status (CMP4RTS)** This bit indicates the status of comparator 4 reach voltage threshold. This bit is cleared when writing 1 to it. If CMP4GPOL is set to 0b (active-high), 0: Not reach the voltage threshold 1: Reach the voltage threshold. If CMP4GPOL is set to 1b (active-low), 0: Reach the voltage threshold 1: Not reach the voltage threshold
4	R/WC	0b	**Comparator 3 Reach Threshold Status (CMP3RTS)** This bit indicates the status of comparator 3 reach voltage threshold. This bit is cleared when writing 1 to it. If CMP3GPOL is set to 0b (active-high), 0: Not reach the voltage threshold 1: Reach the voltage threshold. If CMP3GPOL is set to 1b (active-low), 0: Reach the voltage threshold 1: Not reach the voltage threshold
3	-	-	**Reserved**
2	R/WC	0b	**Comparator 5 Reach Threshold Interrupt Status(CMP5RTIS)** This bit indicates the interrupt status of comparator 5 reach voltage threshold. This bit is cleared when writing 1 to it. 0: Not reach the voltage threshold 1: Reach the voltage threshold.
1	R/WC	0b	**Comparator 4 Reach Threshold Interrupt Status (CMP4RTIS)** This bit indicates the interrupt status of comparator 4 reach voltage threshold. This bit is cleared when writing 1 to it. 0: Not reach the voltage threshold 1: Reach the voltage threshold.

Bit	R/W	Default	Description
0	R/WC	0b	**Comparator 3 Reach Threshold Interrupt Status (CMP3RTIS)** This bit indicates the interrupt status of comparator 3 reach voltage threshold. This bit is cleared when writing 1 to it. 0: Not reach the voltage threshold 1: Reach the voltage threshold.

7.11.4.49 Voltage Comparator 3 Control Register (VCMP3CTL)

This register controls the operation of voltage comparator 3.

Address Offset: 6Eh

Bit	R/W	Default	Description
7	R/W	0b	**Comparator 3 Enable (CMP3EN)** 0: Disable 1: Enable
6	R/W	0b	**Comparator 3 Interrupt Enable (CMP3INTEN)** 0: Disable 1: Enable
5	R/W	0b	**Comparator 3 Trigger Mode (CMP3TMOD)** This bit is to select the trigger condition. 0: Less then or equal to CMP3THRDAT [9:0] 1: Greater then CMP3THRDAT [9:0]
4	R/W	0b	**Comparator 3 Edge/Level Sense Mode (CMP3ELSM)** This bit determines the sensed mode of the comparator 3. 0: Level-sensed 1: Edge-sensed
3	R/W	0b	**Comparator 3 GPIO Polarity (CMP3GPOL)** This bit determines the active high/low of the comparator 3. 0: Active-high 1: Active-low
2-0	R/W	000b	**Comparator 3 Channel Select LSB (CMP3CSELL)** These bits are to select the ADC channel for the comparator 3. (Combined with VCMP3CSELM) 0000b: ADC0 0001b: ADC1 0010b: ADC2 0011b: ADC3 0100b: ADC4 0101b: ADC5 0110b: ADC6 0111b: ADC7

7.11.4.50 Voltage Comparator 3 Threshold Data Buffer MSB (VCMP3THRDATM)

Address Offset: 6Fh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 3 Threshold Data (CMP3THRDAT9-8)** The MSB (2 Bits) of CMP3THRDAT.

7.11.4.51 Voltage Comparator 3 Threshold Data Buffer LSB (VCMP3THRDATL)

Address Offset: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Comparator 3 Threshold Data (CMP3THRDAT7-0)** The LSB (8 Bits) of CMP3THRDAT.

7.11.4.52 Voltage Comparator 4 Control Register (VCMP4CTL)

This register controls the operation of voltage comparator 4.

Address Offset: 71h

Bit	R/W	Default	Description
7	R/W	0b	**Comparator 4 Enable (CMP4EN)** 0: Disable 1: Enable
6	R/W	0b	**Comparator 4 Interrupt Enable (CMP4INTEN)** 0: Disable 1: Enable
5	R/W	0b	**Comparator 4 Trigger Mode (CMP4TMOD)** This bit is to select the trigger condition. 0: Less then or equal to CMP4THRDAT [9:0] 1: Greater then CMP4THRDAT [9:0]
4	R/W	0b	**Comparator 4 Edge/Level Sense Mode (CMP4ELSM)** Determines the sensed mode of the comparator 4. 0: Level-sensed 1: Edge-sensed
3	R/W	0b	**Comparator 4 GPIO Polarity (CMP4GPOL)** This bit determines the active high/low of the comparator 4. 0: Active-high 1: Active-low
2-0	R/W	000b	**Comparator 4 Channel Select LSB (CMP4CSELL)** Select the ADC channel for the comparator 4. (Combined with VCMP4CSELM) 0000b: ADC0 0001b: ADC1 0010b: ADC2 0011b: ADC3 0100b: ADC4 0101b: ADC5 0110b: ADC6 0111b: ADC7

7.11.4.53 Voltage Comparator 4 Threshold Data Buffer MSB (VCMP4THRDATM)

Address Offset: 72h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 4 Threshold Data (CMP4THRDAT9-8)** The MSB (2 Bits) of CMP4THRDAT.

7.11.4.54 Voltage Comparator 4 Threshold Data Buffer LSB (VCMP4THRDATL)

Address Offset: 73h

Bit	R/W	Default	Description
7-0	R/W	00h	**Comparator 4 Threshold Data (CMP4THRDAT7-0)** The LSB (8 Bits) of CMP4THRDAT.

7.11.4.55 Voltage Comparator 5 Control Register (VCMP5CTL)

This register controls the operation of voltage comparator 5.

Address Offset: 74h

Bit	R/W	Default	Description
7	R/W	0b	**Comparator 5 Enable (CMP1EN)** 0: Disable 1: Enable
6	R/W	0b	**Comparator 5 Interrupt Enable (CMP5INTEN)** 0: Disable 1: Enable
5	R/W	0b	**Comparator 5 Trigger Mode (CMP5TMOD)** This bit is to select the trigger condition. 0: Less then or equal to CMP5THRDAT [9:0] 1: Greater then CMP5THRDAT [9:0]
4	R/W	0b	**Comparator 5 Edge/Level Sense Mode (CMP5ELSM)** This bit determines the sensed mode of the comparator 5. 0: Level-sensed 1: Edge-sensed
3	R/W	0b	**Comparator 5 GPIO Polarity (CMP5GPOL)** This bit determines the active high/low of the comparator 5. 0: Active-high 1: Active-low
2-0	R/W	000b	**Comparator 5 Channel Select LSB (CMP5CSELL)** These bits are to select the ADC channel for the comparator 5. (Combined with VCMP5CSELM) 0000b: ADC0 0001b: ADC1 0010b: ADC2 0011b: ADC3 0100b: ADC4 0101b: ADC5 0110b: ADC6 0111b: ADC7

7.11.4.56 Voltage Comparator 5 Threshold Data Buffer MSB (VCMP5THRDATM)

Address Offset: 75h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 5 Threshold Data (CMP5THRDAT9-8)** The MSB (2 Bits) of CMP5THRDAT.

7.11.4.57 Voltage Comparator 5 Threshold Data Buffer LSB (VCMP5THRDATL)

Address Offset: 76h

Bit	R/W	Default	Description
7-0	R/W	00h	**Comparator 5 Threshold Data (CMP5THRDAT7-0)** The LSB (8 Bits) of CMP5THRDAT.

7.11.4.58 Voltage Comparator 0 Channel Select MSB (VCMP0CSELM)

Address Offset: 77h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Comparator 0 Channel Select MSB (CMP0CSELM)** This bit is to select the ADC channel for the comparator 0. (Combinded with VCMP0CSELL)

7.11.4.59 Voltage Comparator 1 Channel Select MSB (VCMP1CSELM)

Address Offset: 78h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Comparator 1 Channel Select MSB (CMP1CSELM)** This bit is to select the ADC channel for the comparator 1. (Combined with VCMP1CSELL)

7.11.4.60 Voltage Comparator 2 Channel Select MSB (VCMP2CSELM)

Address Offset: 79h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Comparator 2 Channel Select MSB (CMP2CSELM)** This bit is to select the ADC channel for the comparator 2. (Combined with VCMP2CSELL)

7.11.4.61 Voltage Comparator 3 Channel Select MSB (VCMP3CSELM)

Address Offset: 7Ah

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Comparator 3 Channel Select MSB (CMP3CSELM)** This bit is to select the ADC channel for the comparator 3. (Combined with VCMP3CSELL)

7.11.4.62 Voltage Comparator 4 Channel Select MSB (VCMP4CSELM)

Address Offset: 7Bh

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Comparator 4 Channel Select MSB (CMP4CSELM)** This bit is to select the ADC channel for the comparator 4. (Combined with VCMP4CSELL)

7.11.4.63 Voltage Comparator 5 Channel Select MSB (VCMP5CSELM)

Address Offset: 7Ch

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Comparator 5 Channel Select MSB (CMP5CSELM)** This bit is to select the ADC channel for the comparator 5. (Combined with VCMP5CSELL)

7.11.5 ADC Programming Guide

Table 7-19. Detailed Step of ADC Channel Conversion

Step	Description
1	Set AINITB@ADCSTS = 1 (only once after VSTBY power on)
2	Automatic hardware calibration enable (only once after VSTBY power on) AHCE@KDCTL = 1
3	Set AINITB@ADCSTS = 0 (only once after VSTBY power on)
4	Enable VCHiCTL for measuring desired channels; n = 0,1, 2, or 3
5	For example; To measure ADC0 voltage on voltage buffer 1 Set SELIN@VCH1CTL = 0
6	Start ADC channel conversion by setting ADCEN@ADCCFG =1
7	Wait for DATVAL@VCH1CTL = 1 IGet ADC0 output data **D**[9:0] by reading VCH1DATM and VCH1DATL **D**[9:0] = {VCH1DATM [1:0], VCH1DATL[7:0]}
8	Disable ADC to reduce power consumption by setting ADCEN@ADCCFG = 0

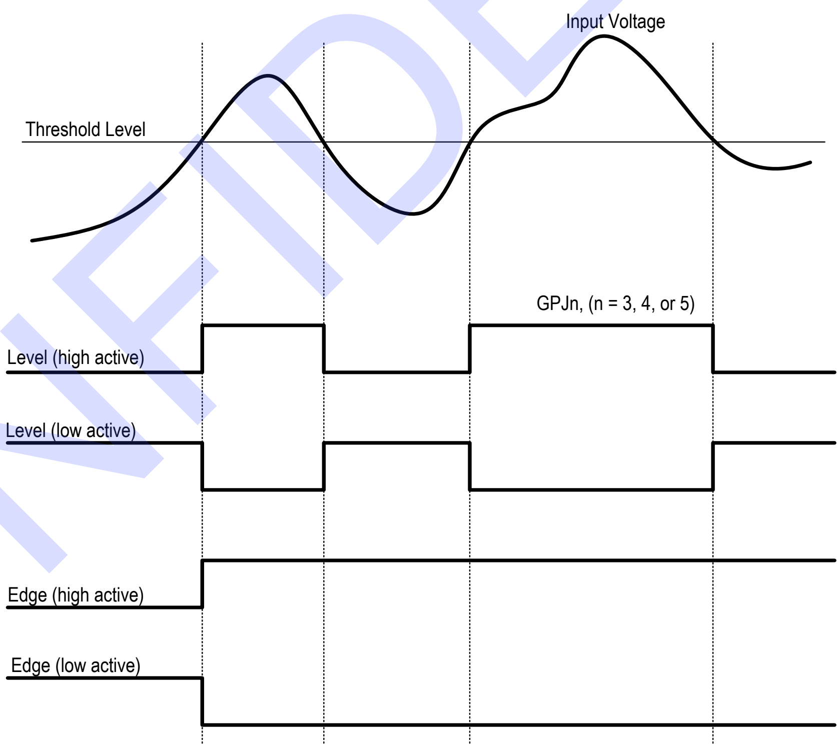
7.11.6 Voltage Comparator Programming Guide

Table 7-20. Detailed Step of Voltage Comparator Programming

Step	Description
1	**Set voltage comparator threshold level buffer:** Program CMP0THRDAT[9:0] to select the threshold level for voltage comparator 0. The equivalent threshold voltage is (3V * CMP0THRDAT/1023).
2	**Select voltage input channel:** Program CMP0CSEL to select one of the voltage input channels AD0-AD7. This sets voltage comparator 0 to monitor the selected voltage input channel. Note that the selected channel must be set to its alternate function for ADC application.
3	**Set voltage comparator trigger mode:** If CMP0TMOD is set 0, a event is produced while the voltage of the selected channel is lower than or equal to the threshold level. If CMP0TMOD is set 1, a event is produced while the voltage of the selected channel is higher than the threshold level.
4	**Set scan period of voltage comparator:** Set CMPSNP @ VCMPSCP to determine the interval per comparing operation for voltage comparator.
5	**Set event response:** Set CMP0INTEN = 1, the event in Step 3 would be propagated to INT151. or Set CMP0GPEN @ GCR15 and GPCRJ3 = 0x00 , the event in Step 3 would be propagated to GPJ3

Step	Description
6	**Start voltage comparator conversion** CMP0EN @ VCMP0CTL = 1
7	**Wait for intput voltage's reaching thershold level** If the input voltage reaches the threshold level, CMP0RTS @VCMPSTS will be set to 1 , and corresponding GPJ3 will change the output status if this function is enabled in Step 5. In Level-sensed mode, the input voltage far away from the threshold level, CMP0RTS / GPJ3 willl be reset immediately. In Edge-sensed mode, the input voltage is far away from the threshold level, CMP0RTS / GPJ3 only be reset when write 1 to CMP0RTS. If CMP0INTEN = 1, the input voltage reaches the threshold level, then generates INT151 , and CMP0RTIS @VCMPSTS will be set to 1. Write 1 to clear this bit and only the input voltage is far away from the threshold level. (Refer to Figure 7-15 , on page 381)

Figure 7-15. Voltage Comparator Operation Time



7.12 PWM

7.12.1 Overview

The PWM module generates eight 8-bit PWM outputs; each PWM output may have a different duty cycle. PWM2 & PWM 3 support 10-bit resolution and the others support 8-bit.

7.12.2 Features

- Supports eight PWM outputs.
- Two 10-bit channels, six 8-bit channels.
- Supports two sets tachometers; each set tachometer can be switched from two external pins.
- Supports PWM open-drain output.

7.12.3 Functional Description

7.12.3.1 General Description

Figure 7-16. PWM Diagram

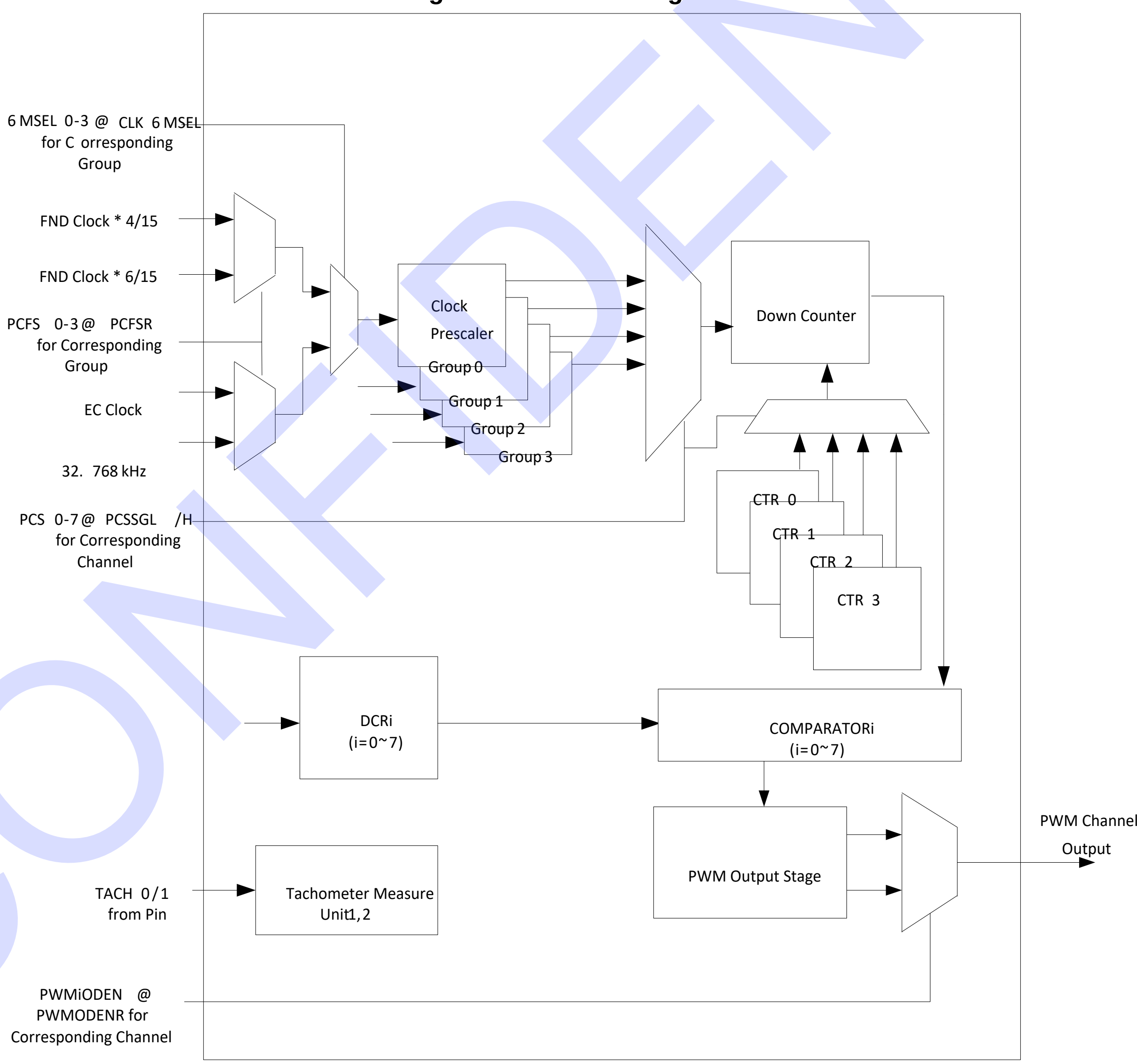
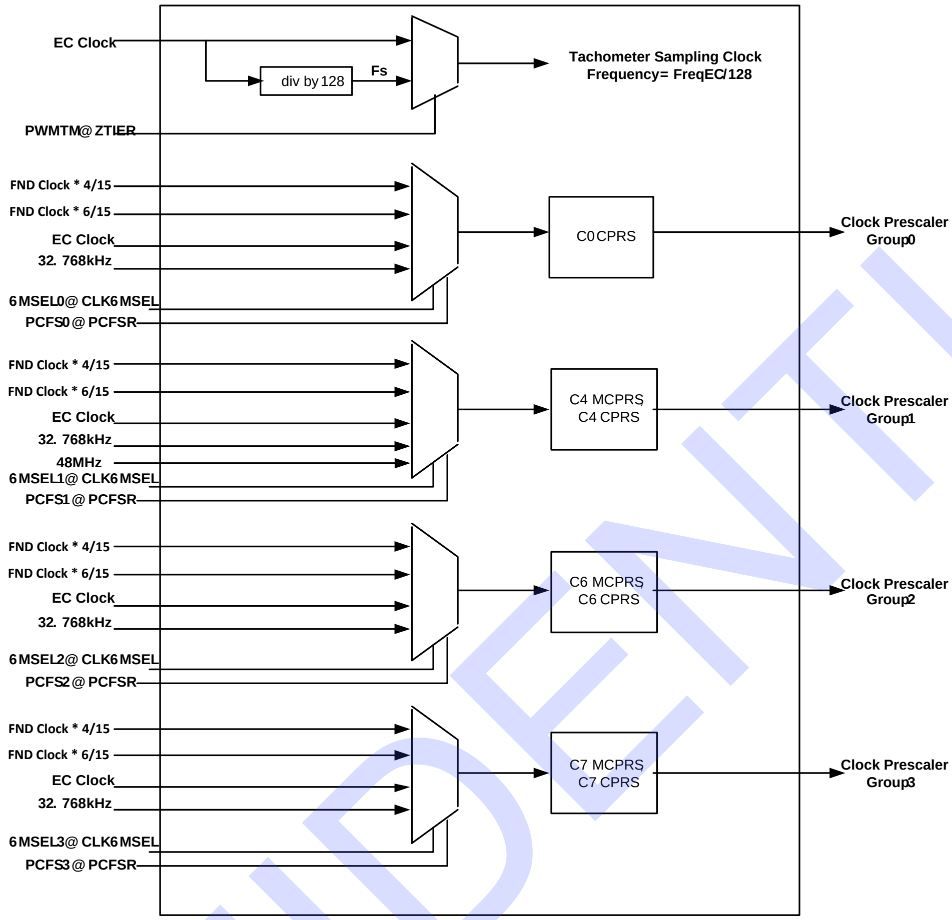


Figure 7-17. PWM Clock Tree



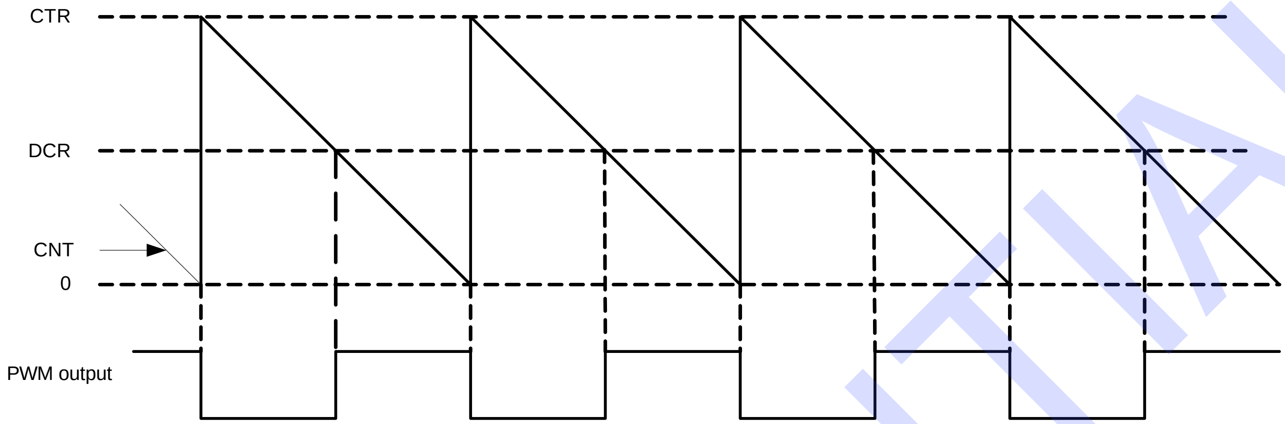
The PWM uses the 32.768 kHz Clock, EC Clock, or FND Clock as a reference for its PWM output. The prescaler divider values in CiCRPS register which divides the PWM input clock into its working clock respectively. Each channel can select their prescaler divider by {PCSSGH, PCSSGL} register. The prescaler divider C0CPRS register has 8-bit counter value; and the {CiMCRPS, CiCRPS}(i=4,6,7) has 16-bit counter value. The PWM provides eight 8-bit PWM outputs, which are PWM0 to PWM7. Each PWM output is controlled by its Duty Cycle registers (DCRi, i =0 to 7). All PWM output is controlled by a Cycle Time register (CTR).

When PWM working clock is enabled, the PWM cycle output is high when the value in the DCRi register is greater than the value in CTR down-counter. When the value of DCRi register is not greater than the value in CTR down-counter, the PWMi cycle output is on LOW and PWMi cycle output polarity can be inversed by INVPi register.

When the value in CTR counter down-counter reaches 0, the value in CTR counter will be reloaded then start down-counter until the PWM working clock is disabled.

Cycle Time and Duty Cycle

Figure 7-18. PWM Output Waveform



The PWM module supports duty cycles ranging from 0% to 100%.
The PWMi output signal cycle time is:

n(CiCPRS + 1) x (CTR + 1) x T clk

Where:

- T clk is the period of PWM input clock = (1 / 32.768 kHz) or (1 / FreqEC), which is selected by PCFS3-0 in PCFSR regiser. (FreqEC is listed in Table 10-2 on page 570)
- The PWMi output signal duty cycle (in %, when INVPi is 0) is:
  (DCRi) / (CTR + 1) x 100.

In the following cases, the PWMi output is hold at a state(low or high):
•PWMi output is still low when the content of DCRi is greater than the CTR value.
•PWMi output is still high when the content of DCRi is equal to the CTR value.
•PWMi output is still low when the content of DCRi =0 & INVPi = 0 is in PWMPOL register.

PWM Inhibit Mode

The PWM is in an inhibit mode when PCCE in ZTIER Register is 0. In this mode, the PWM input clock is disabled (stopped). The PWMi signal is 0 when INVPi bit is 0; it is 1 when INVPi bit is 1. It is recommended the PRSC and CTR registers should be updated in a PWM inhibit mode.

7.12.3.2 Manual Fan Control Mode

The content of the Tachometer Reading Register is still updated according to the sampling counter that samples the tachometer input (TACH0A/B pin for FAN1 of the local sensor zone). The sampling rate (fs) is FreqEC / 128. (FreqEC is listed in Table 10-2 on page 570)

Fan Speed (R.P.M.) = 60 / (1/fs sec * {FnTMRR, FnTLRR} * P)

n denotes 1 or 2
P denotes the numbers of square pulses per revolution.
And {FnTMRR, FnTLRR} = 0000h denotes Fan Speed is zero.

7.12.3.3 Manual Fan Backlight Function

The content of the Tachometer Reading Register is still updated based on the sampling counter that samples the tachometer input (TACH1A/B pin for FAN2 of the local sensor zone). The values of the Tachometer Reading Register represent the actual detected frequency and duty cycle based on sampling PWM clock (default 48Mhz, refer to definition of SCDCR4).

Frequency = {F2TMRR, F2TLRR}
Duty Cycle = {DMSBDCVF2T, DDRF2T} / 1024 = x %

7.12.3.4 Manual Color Frequency Control Mode or Backlight Function

In this mode, the software may monitor the Frequency Reading Register to control the frequency of the input signal.

The content of the Color Frequency Reading Register keeps being updated every 31.25 ms, and the sample counter is the input signal from GPJ0.

Color Frequency = 16 * {CFMRR, CFLRR}
The Frequency range is from 0Hz to 1.04MHz, but the Result is less precise if the frequency of the input signal is smaller.

In the Backlight mode b4~3@PWM5TOCTRL = 11b can enable the backlight mode, and the content of the Color Reading Register represents the actual detected frequency and duty cycle based on sampling PWM clock (default 48Mhz, refer to definition of SCDCR4).

Frequency = {CFMRR, CFLRR}
Duty Cycle = {BMSBDCVCS, BDRCS} / 1024 = x %

7.12.4 EC Interface Registers

These registers are mapped in the address space of EC. The registers are listed below and the base address is 1800h.

Table 7-21. EC View Register Map, PWM

7 ... 0	Offset
Channel 0 Clock Prescaler Register (C0CPRS)	00h
Cycle Time 0 (CTR0)	01h
PWM Duty Cycle (DCR0-7)	02h-09h
PWM Polarity (PWMPOL)	0Ah
Prescaler Clock Frequency Select Register (PCFSR)	0Bh
Prescaler Clock Source Select Group Low (PCSSGL)	0Ch
Prescaler Clock Source Select Group High (PCSSGH)	0Dh
Prescaler Clock Source Gating Register (PCSGR)	0Fh
Cycle Time 1 MSB Register (CTR1M)	10h
Fan 1 Tachometer LSB Reading (F1TLRR)	1Eh
Fan 1 Tachometer MSB Reading (F1TMRR)	1Fh
Fan 2 Tachometer LSB Reading (F2TLRR)	20h
Fan 2 Tachometer MSB Reading (F2TMRR)	21h
Zone Interrupt Status Control (ZINTSCR)	22h
PWM Clock Control Register (ZTIER)	23h
Channel 4 Clock Prescaler Register (C4CPRS)	27h
Channel 4 Clock Prescaler MSB Register (C4MCPRS)	28h
Channel 6 Clock Prescaler Register (C6CPRS)	2Bh
Channel 6 Clock Prescaler MSB Register (C6MCPRS)	2Ch
Channel 7 Clock Prescaler Register (C7CPRS)	2Dh
Channel 7 Clock Prescaler MSB Register (C7MCPRS)	2Eh
PWM Duty Cycle 2 MSB (DCR2M)	30h
PWM Duty Cycle 3 MSB (DCR3M)	31h
Detected Duty Register of Fan 2 Tachometer (DDRF2T)	3Ch
Detected MSB Duty Register of Fan 2 Tachometer (DMDRF2T)	3Eh
PWM Clock 6MHz Select Register (CLK6MSEL)	40h

7 0	Offset
Cycle Time 1 (CTR1)	41h
Cycle Time 2 (CTR2)	42h
Cycle Time 3 (CTR3)	43h
PWM5 Timeout Control Register (PWM5TOCTRL)	44h
Color Frequency LSB Register (CFLRR)	45h
Color Frequency MSB Register (CFMRR)	46h
Color Frequency Interrupt Control Register (CFINTCTRL)	47h
Tachometer Switch Control Register (TSWCTLR)	48h
PWM Output Open-Drain Enable Register (PWMODENR)	49h
Backlight Duty Register for Color Sensor (BDRCS)	4Ch
Backlight MSB Duty Register for Color Sensor (BMDRCS)	4Eh
Color Frequency Control Mode Register (CFCMR)	4Fh

Other related register(s):

- General Control 2 Register (GCR2), TACH2E bit
- General Control 5 Register (GCR5), T0BEN bit
- General Control 5 Register (GCR5), T1BEN bit

For a summary of the abbreviations used for register types, see “Register Abbreviations and Access Rules”

7.12.4.1 Channel 0 Clock Prescaler Register (C0CPRS)

This register controls the cycle time and the minimal pulse width of channel 0~3.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV)** PWM input clock is divided by the number of (C0CPRS+ 1). For example, the value of 01h results in a divisor of 1. The value of FFh results in a divisor of 256. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.12.4.2 Cycle Time Register 0 (CTR0)

This register controls the cycle time 0 and duty cycle steps.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 0 (CTV0)** The Prescaler output clock is divided by the number of (CTR0 + 1). For example, the value of 00h results in a divisor of 1. The value of FFh results in a divisor of 256. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.12.4.3 Cycle Time Register 1 (CTR1)

This register controls the LSB of cycle time 1 and duty cycle steps.

Address Offset: 41h

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 1 (CTV1)** The Prescaler output clock is divided by the number of ({CTR1M, CTR1} + 1). For example, the value of 00h results in a divisor of 1. The value of 3FFh results in a divisor of 1024. After writing data to the register, system will be changed to the 4-CTR mode. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.12.4.4 Cycle Time Register 2 (CTR2)

This register controls the cycle time 2 and duty cycle steps.

Address Offset: 42h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 2 (CTV2)** The Prescaler output clock is divided by the number of (CTR2+ 1). For example, the value of 00h results in a divisor of 1. The value of FFh results in a divisor of 256. After writing data to the register, system will be changed to the 4-CTR mode. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.12.4.5 Cycle Time Register 3 (CTR3)

This register controls the cycle time 3 and duty cycle steps.

Address Offset: 43h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 3 (CTV3)** The Prescaler output clock is divided by the number of (CTR3+ 1). For example, the value of 00h results in a divisor of 1. The value of FFh results in a divisor of 256. After writing data to the register, system will be changed to the 4-CTR mode. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.12.4.6 PWM Duty Cycle Register 0 to 7(DCRi)

This register (DCRi; I=0 to 7) controls the duty cycle of PWMi output signal.

Address Offset: 02h(ch0), 03h(ch1), 04h(ch2), 05h(ch3), 06h(ch4), 07h(ch5), 08h(ch6), 09h(ch7);

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value (DCV)** DCRi register decides the number of clocks for which PWMi is high when INVPi bit is 0 in PWMPOL register. The PWMi Duty Cycle output = (DCRi)/(CTR+1) If the DCRi value > CTR value, PWMi signal is still low. If DCRi value = CTR value, PWMi signal is still high. When Inverse PWMi bit is 1, the value of PWMi is inversed.

7.12.4.7 PWM Polarity Register (PWMPOL)

This register controls the polarity of PWM0 to PWM7.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Inverse PWM Outputs (INVP7-0)** Bit 7 to 0 control the polarity of PWM7 to PWM0 respectively. 0: Non-inverting. 1: Inverting.

7.12.4.8 Prescaler Clock Frequency Select Register (PCFSR)

This register Bit 3~0 is used to select prescaler clock frequency for four channel group 3~0. Each of them includes 1 set prescaler registers. See the following table.

Channel Group	Prescaler Channels
0	C0CPRS
1	C4MCPRS,C4CPRS
2	C6MCPRS,C6CPRS
3	C7MCPRS,C7CPRS

Address Offset: 0Bh

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**Prescaler Clock High Frequency Select for Group 1** The high frequency clock source select of the prescaler of group 1 is defined by this bit. 0b: Select lower frequency (reference to the definition of PCFS3-0) 1b: Select 48 MHz.
4	-	-	**Reserved**
3-0	R/W	0000b	**Prescaler Clock Frequency Select (PCFS3-0)** The clock source of the prescaler of group 0 consists of G6MSEL0 and PCFS0 bit. G6MSEL0 bit is in CLK6MSEL register. PCFS0 bit is in this register. {G6MSEL0, PCFS0}: 00b: Select 32.768 kHz. 01b: Select FreqEC (EC Clock). 10b: Select FreqFND * 6/15 11b: Select FreqFND * 4/15 (FreqEC and FreqPLL are listed in Table 10-2 on page 570) So are group 1, 2 and 3.

7.12.4.9 Prescaler Clock Source Select Group Low (PCSSGL)

This register is used to select prescaler clock source for four channels. Each channel uses 2 bits to select one from four prescaler clock sources.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-6	R/W	00b	**Prescaler Clock Select 3 (PCS3)** The bits select prescaler clock for channel 3. The bits 7-6 are the same as bit 1-0.
5-4	R/W	00b	**Prescaler Clock Select 2 (PCS2)** The bits select prescaler clock for channel 2. The bits 5-4 are the same as bit 1-0.
3-2	R/W	00b	**Prescaler Clock Select 1 (PCS1)** The bits select prescaler clock for channel 1. The bits 3-2 are the same as bit 1-0.

Bit	R/W	Default	Description
1-0	R/W	00b	**Prescaler Clock Select 0 (PCS0)** Default as below： 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR0 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR0 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR0 After writing data to CTR1,CTR2 or CTR3 register 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR1 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR2 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR3

7.12.4.10 Prescaler Clock Source Select Group High (PCSSGH)

This register is used to select prescaler clock source for four channels. Each channel uses 2 bits to select one from four prescaler clock sources.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-6	R/W	01b	**Prescaler Clock Select 7 (PCS7)** The bits select prescaler clock for channel 7. The bits 7-6 are the same as bit 1-0.
5-4	R/W	01b	**Prescaler Clock Select 6 (PCS6)** The bits select prescaler clock for channel 6. The bits 5-4 are the same as bit 1-0.
3-2	R/W	01b	**Prescaler Clock Select 5 (PCS5)** The bits select prescaler clock for channel 5. The bits 3-2 are the same as bit 1-0.
1-0	R/W	01b	**Prescaler Clock Select 4 (PCS4)** The bits select prescaler clock for channel 4. Default as below： 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR0 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR0 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR0 After writing data to CTR1,CTR2 or CTR3 register 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR1 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR2 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR3

7.12.4.11 Prescaler Clock Source Gating Register (PCSGR)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Clock Source Gating (PCSG)** Bits 7-0 are used to gate prescaler clock source for PWM channels 7-0 respectively. 0: no gating clock source 1: gating clock source; PWM channel output is 0 when INVP bit is set to 0 respectively

7.12.4.12 Cycle Time 1 MSB Register (CTR1M)

This register controls the MSB of cycle time 1 and duty cycle steps.

Address Offset: 10h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	3h	**Cycle Time Value 1 MSB(CTV1M)** The Prescaler output clock is divided by the number of ({CTR1M, CTR1} + 1). For example, the value of 00h results in a divisor of 1. The value of 3FFh results in a divisor of 1024. After writing data to the register, system will be changed to the 4-CTR mode. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.12.4.13 Fan 1 Tachometer LSB Reading Register (F1TLRR)

This register reflects the LSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. The tachometer input of Fan 1 corresponds to TACH0A/TACH0B, and it can be switched by controlling the T0CHSEL bit.
Reading F1TLRR and F1TMRR registers should be in pairs to get the correct 16-bit tachometer value.
Reading these two registers via D2EC/I2EC is not guaranteed to get the correct value.
After switching the input TACH0A/TACH0B, these two registers should be read in pairs after the data-valid status (T0DIS or T0DVS bit) is set.

Address Offset: 1Eh

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer LSB Value (CTACHLV)** The value of bit 7-0 denotes LSB Tachometer speed.

7.12.4.14 Fan 1 Tachometer MSB Reading Register (F1TMRR)

This register reflects the MSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. The tachometer input of Fan 1 corresponds to TACH0A/TACH0B, and it can be switched by controlling the T0CHSEL bit.

Address Offset: 1Fh

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer MSB Value (CTACHMV)** The value of bits 7-0 denotes MSB Tachometer speed.

7.12.4.15 Fan 2 Tachometer LSB Reading Register (F2TLRR)

This register reflects the LSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. The tachometer input of Fan 2 corresponds to TACH1A/TACH1B, and it can be switched by controlling the T1CHSEL bit.
Reading F2TLRR and F2TMRR registers should be in pairs to get the correct 16-bit tachometer value.
Reading these two registers via D2EC/I2EC is not guaranteed to get the correct value.
After switching the input TACH1A/TACH1B, these two registers should be read in pairs after the data-valid status (T1DIS or T1DVS bit) is set.

Address Offset: 20h

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer LSB Value (CTACHLV)** The value of bits 7-0 denotes the LSB Tachometer speed based on sampling the PWM clock (default 48Mhz, refer to definition of SCDCR4).

7.12.4.16 Fan 2 Tachometer MSB Reading Register (F2TMRR)

This register reflects the MSB value of the current tachometer of the Fan. The value is represented for each fan in a 16-bit binary digits. The tachometer input of Fan 2 corresponds to TACH1A/TACH1B, and it can be switched by controlling the T1CHSEL bit.

Address Offset: 21h

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer MSB Value (CTACHMV)** The value of bits 7-0 denotes MSB Tachometer speed based on sampling the PWM clock (default 48Mhz, refer to definition of SCDCR4).

7.12.4.17 Zone Interrupt Status Control Register (ZINTSCR)

Address Offset: 22h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**TACH0A/TACH0B Data-valid Interrupt Enable (T0DIE)** 1: Enable interrupt to the CPU when fan 1 tachometer data is valid. 0: Disable interrupt to the CPU when fan 1 tachometer data is valid.
4	R/WC	0b	**TACH0A/TACH0B Data-valid Interrupt Clear (T0DIC)** Write one to clear the Interrupt status, which is caused when fan 1 tachometer data is valid; writing zero is ignored.
3	R	0b	**TACH0A/TACH0B Data-valid Interrupt Status (T0DIS)** 1: Fan 1 tachometer data-valid event occurs. 0: No fan 1 tachometer data-valid event occurs.
2	R/W	0b	**TACH1A/TACH1B Data-valid Interrupt Enable (T1DIE)** 1: Enable interrupt to the CPU when fan 2 tachometer data is valid. 0: Disable interrupt to the CPU when fan 2 tachometer data is valid.
1	R/WC	0b	**TACH1A/TACH1B Data-valid Interrupt Clear (T1DIC)** Write one to clear the Interrupt status, which is caused when fan 2 tachometer data is valid; writing zero is ignored.
0	R	0b	**TACH1A/TACH1B Data-valid Interrupt Status (T1DIS)** 1: Fan 2 tachometer data-valid event occurs. 0: No fan 2 tachometer data-valid event occurs.

7.12.4.18 PWM Clock Control Register (ZTIER)

Address Offset: 23h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-2	-	0b	**Reserved**
1	R/W	0b	**PWM Clock Counter Enable (PCCE)** 1: Enable PWMs clock counter. Set this bit to 1 after all other registers have been set. 0: Disable PWMs clock counter
0	R/W	0b	**PWM Test Mode (PWMTM)** 1: PWM switches to a test mode 0: PWM works on a normal mode

7.12.4.19 Channel 4 Clock Prescaler Register (C4CPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV7-0)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divisor of 2 and the value of FFFFh results in a divisor of 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C4MCPRS defines the high byte.

7.12.4.20 Channel 4 Clock Prescaler MSB Register (C4MCPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/W	00b	**Prescaler Divider Value (PSDV15-8)** Refer to the previous register for the detail.

7.12.4.21 Channel 6 Clock Prescaler Register (C6CPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Bh

	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV7-0)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divisor of 2 and the value of FFFFh results in a divisor of 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C6MCPRS defines the high byte.

7.12.4.22 Channel 6 Clock Prescaler MSB Register (C6MCPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV15-8)** Refer to the previous register for the detail.

7.12.4.23 Channel 7 Clock Prescaler Register (C7CPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV7-0)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divisor of 2 and the value of FFFFh results in a divisor of 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C7MCPRS defines the high byte.

7.12.4.24 Channel 7 Clock Prescaler MSB Register (C7MCPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV15-8)** Refer to the previous register for the detail.

7.12.4.25 PWM Duty Cycle Register 2 MSB (DCR2M)

This register controls the duty cycle MSB of PWM2 output signal.

Address Offset: 30h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00h	**Duty Cycle Value 2 MSB (DCV2M)** DCR2M register decides the number of clocks for which PWM2 is high when INVP2 bit is 0 in PWMPOL register. The PWM2 Duty Cycle output = ({DCR2M, DCR2})/({CTR1M, CTR1}+1) If the {DCR2M, DCR2} value > {CTR1M, CTR1} value, PWM2 signal is still low. If {DCR2M, DCR2} value = {CTR1M, CTR1} value, PWM2 signal is still high. When Inverse PWM2 bit is 1, the value of PWM2 is inversed.

7.12.4.26 PWM Duty Cycle Register 3 MSB (DCR3M)

This register controls the duty cycle MSB of PWM3 output signal.

Address Offset: 31h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00h	**Duty Cycle Value 3 MSB (DCV3M)** DCR3M register decides the number of clocks for which PWM3 is high when INVP3 bit is 0 in PWMPOL register. The PWM3 Duty Cycle output = ({DCR3M, DCR3})/({CTR1M, CTR1}+1) If the {DCR3M, DCR3} value > {CTR1M, CTR1} value, PWM3 signal is still low. If {DCR3M, DCR3} value = {CTR1M, CTR1} value, PWM3 signal is still high. When Inverse PWM3 bit is 1, the value of PWM3 is inversed.

7.12.4.27 Detected Duty Register of Fan 2 Tachometer (DDRF2T)

This register indicates the detected duty of Fan 2 Tachometer.

Address Offset: 3Ch

Bit	R/W	Default	Description
7-0	R	00h	**Detected Duty Cycle Value of Fan 2 Tachometer (DDCVF2T)** The value of the detected duty cycle is calculated as the following based on sampling the PWM clock (default 48Mhz, refer to definition of SCDCR4): { DMSBDCVF2T, DDRF2T }/1024 = x %

7.12.4.28 Detected MSB Duty Register of Fan 2 Tachometer (DMDRF2T)

This register indicates the detected MSB duty of Fan 2 Tachometer.

Address Offset: 3Eh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**

Bit	R/W	Default	Description
1-0	R	00b	**Detected MSB Duty Cycle Value of Fan 2 Tachometer (DMSBDCVF2T)** The value of the detected duty cycle is calculated as the following based on sampling the PWM clock (default 48Mhz, refer to definition of SCDCR4): { DMSBDCVF2T , DDRF2T }/1024 = x %

7.12.4.29 PWM Clock 6MHz Select Register (CLK6MSEL)

This register controls the group clock.

Address Offset: 40h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R	0b	**Cycle Time Register Mode (CTRMODE)** 0: 1 cycle time mode 1: 4 cycle time mode After writing data to CTR1, CTR2, or CTR3, the bit will be set to 1 and system will be changed to the 4-CTR mode.
3-0	R/W	0000b	**Clock Group 6MHz Selection (G6MSEL3-0)** Refer to PCFS3-0 field in PCFSR register.

7.12.4.30 PWM5 Timeout Control Register (PWM5TOCTRL)

This register controls the PWM5 Timeout Period.

Address Offset: 44h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**Fan2 Tachometer Input Debounce Disable** 1b: Disable input debounce. 0b: Enable input debounce.
4	R/W	0b	**Backlight Mode for Color Sensor** 0b: Disable 1b: Enable
3	R/W	0b	**Test Mode for Color Frequency Control Mode** 1: Color Frequency mode switches to a test mode 0: Color Frequency mode works on a normal mode
2-0	R/W	000b	**PWM5 Timeout Period Selection (PWM5TOSEL3-0)** If PWM5 Timeout is enabled, PWM5 output would be held 100% duty when the DCR of PWM5 is not updated during the specified time selected in Timeout Control Register. 000h: Disable 001h: 1 sec 010h: 1.5 sec 011h: 2 sec 100h: 2.5 sec 101h: 3 sec 110h: 3.5 sec 111h: 4 sec

7.12.4.31 Color Frequency LSB Register (CFLRR)

This register reflects the LSB value of the current Frequency of the Color Sensor from Tach2. The value is shown in 16-bit format.
Reading CFLRR and CFMRR registers should be in pairs to get the correct 16-bit frequnecy value.Reading these two registers via D2EC/I2EC is not guaranteed to get the correct value.

Address Offset: 45h

Bit	R/W	Default	Description
7-0	R	-	**Current Color Frequency LSB Value (CCFLV)** The value of bit 7-0 denotes the LSB Color Frquency based on sampling the PWM clock (default 48Mhz, refer to definition of SCDCR4).

7.12.4.32 Color Frequency MSB Register (CFMRR)

This register reflects the MSB value of the current Frequency of the Color Sensor from Tach2. The value is shown in 16-bit format.

Address Offset: 46h

Bit	R/W	Default	Description
7-0	R	-	**Current Color Frequency MSB Value (CCFMV)** The value of bit 7-0 denotes the MSB Color Frquency based on sampling the PWM clock (default 48Mhz, refer to definition of SCDCR4).

7.12.4.33 Color Frequency Interrupt Control Register (CFINTCTRL)

This register controls the interrupt of the color frequency register.

Address Offset: 47h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**Color Frequency Data-valid Interrupt Enable (CFDIE)** 1: Enable interrupt to the CPU when Color Frequency data is valid. 0: Disable interrupt to the CPU when Color Frequency data is valid.
1	R/WC	0b	**Color Frequency Data-valid Interrupt Clear (CFDIC)** Write one to clear the interrupt status, which is caused when fan 2 tachometer data is valid; writing zero is ignored.
0	R	0b	**Color Frequency Data-valid Interrupt Status (CFDIS)** 1: Color Frequency data-valid event occurs. 0: No Color Frequency data-valid event occurs.

7.12.4.34 Tachometer Switch Control Register (TSWCTLR)

Address Offset: 48h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/WC	0b	**TACH0A/TACH0B Data-valid Status (T0DVS)** Write one to clear the status, which is caused when TACH0A/TACH0B data is valid; writing zero is ignored. This bit will be cleared when the input is switched by controlling the T0CHSEL bit. 0: TACH0A/TACH0B data is not valid. 1: TACH0A/TACH0B data is valid.

Bit	R/W	Default	Description
2	R/W	0b	**TACH0A/TACH0B Channel Selection (T0CHSEL)** This bit controls the channel switch of TACH0A and TACH0B. Notice that the related GPIO ports should be set to the function mode. 0b: Fan 1 tachometer input is set to select TACH0A. 1b: Fan 1 tachometer input is set to select TACH0B.
1	R/WC	0b	**TACH1A/TACH1B Data-valid Status (T1DVS)** Write one to clear the status, which is caused when TACH1A/TACH1B data is valid; writing zero is ignored. This bit will be cleared when the input is switched by controlling the T1CHSEL bit. 0: TACH1A/TACH1B data is not valid. 1: TACH1A/TACH1B data is valid.
0	R/W	0b	**TACH1A/TACH1B Channel Selection (T1CHSEL)** This bit controls the channel switch of TACH1A and TACH1B. Notice that the related GPIO ports should be set to the function mode. 0b: Fan 2 tachometer input is set to select TACH1A. 1b: Fan 2 tachometer input is set to select TACH1B.

7.12.4.35 PWM Output Open-Drain Enable Register (PWMODENR)

Address Offset: 49h

Bit	R/W	Default	Description
7	R/W	0b	**PWM7 Output Open-Drain Enable (PWM7ODEN)** This bit controls the output open-drain function of PWM7. Notice that the related GPIO ports should be set to the function mode. 0b: PWM7 output is set to push-pull mode. 1b: PWM7 output is set to open-drain mode.
6	R/W	0b	**PWM6 Output Open-Drain Enable (PWM6ODEN)** This bit controls the output open-drain function of PWM6. Notice that the related GPIO ports should be set to the function mode. 0b: PWM6 output is set to push-pull mode. 1b: PWM6 output is set to open-drain mode.
5	R/W	0b	**PWM5 Output Open-Drain Enable (PWM5ODEN)** This bit controls the output open-drain function of PWM5. Notice that the related GPIO ports should be set to the function mode. 0b: PWM5 output is set to push-pull mode. 1b: PWM5 output is set to open-drain mode.
4	R/W	0b	**PWM4 Output Open-Drain Enable (PWM4ODEN)** This bit controls the output open-drain function of PWM4. Notice that the related GPIO ports should be set to the function mode. 0b: PWM4 output is set to push-pull mode. 1b: PWM4 output is set to open-drain mode.
3	R/W	0b	**PWM3 Output Open-Drain Enable (PWM3ODEN)** This bit controls the output open-drain function of PWM3. Notice that the related GPIO ports should be set to the function mode. 0b: PWM3 output is set to push-pull mode. 1b: PWM3 output is set to open-drain mode.
2	R/W	0b	**PWM2 Output Open-Drain Enable (PWM2ODEN)** This bit controls the output open-drain function of PWM2. Notice that the related GPIO ports should be set to the function mode. 0b: PWM2 output is set to push-pull mode. 1b: PWM2 output is set to open-drain mode.

Bit	R/W	Default	Description
1	R/W	0b	**PWM1 Output Open-Drain Enable (PWM1ODEN)** This bit controls the output open-drain function of PWM1. Notice that the related GPIO ports should be set to the function mode. 0b: PWM1 output is set to push-pull mode. 1b: PWM1 output is set to open-drain mode.
0	R/W	0b	**PWM0 Output Open-Drain Enable (PWM0ODEN)** This bit controls the output open-drain function of PWM0. Notice that the related GPIO ports should be set to the function mode. 0b: PWM0 output is set to push-pull mode. 1b: PWM0 output is set to open-drain mode.

7.12.4.36 Backlight Duty Register for Color Sensor (BDRCS)

This register indicates the detected backlight duty of Color Sensor.

Address Offset: 4Ch

Bit	R/W	Default	Description
7-0	R	00h	**Backlight Duty Cycle Value of Color Sensor (BDCVCS)** The value of the detected duty cycle is calculated as the following based on sampling the PWM clock (default 48Mhz, refer to definition of SCDCR4): { BMSBDCVCS, BDRCS}/1024 = x %

7.12.4.37 Backlight MSB Duty Register for Color Sensor (BMDRCS)

This register indicates the detected backlight MSB duty of Color Sensor.

Address Offset: 4Eh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	00b	**Backlight MSB Duty Cycle Value of Color Sensor (BMSBDCVCS)** The value of the detected duty cycle is calculated as the following based on sampling the PWM clock (default 48Mhz, refer to definition of SCDCR4): { BMSBDCVCS, BDRCS}/1024 = x %

7.12.4.38 Color Frequency Control Mode Register (CFCMR)

This register indicates the control mode of Color Sensor..

Address Offset: 4Fh

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**Disable Color Sensor Detect** 0: Enable Color detect function. 1: Disable Color detect function.
5	R/W	0b	**Disable Fan 2 Tachometer Detect** 0: Enable Fan 2 Tachometer detect function. 1: Disable Fan 2 Tachometer detect function.
4-3	-	-	**Reserved**
2	R/W	0b	**Color Frequency Detected Edge Select** 0: Falling edge is detected. 1: Rising edge is detected.
1	R/W	0b	**Color Frequency PWM TACH Bypass Mode Select** 0: PIN direct bypass 1: Register mirror mode
0	R/W	0b	**Color Frequency PWM TACH Bypass Mode Enalbe** 0: Disable 1: Enable

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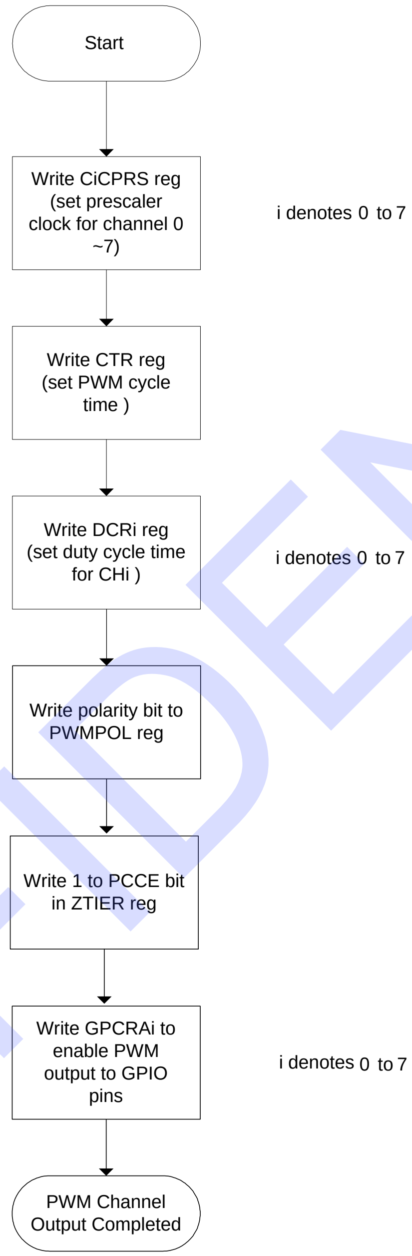
Figure 7-19. Program Flow Chart for PWM Channel Output



7.13 EC Access to the Host Controlled Modules (EC2I Bridge)

7.13.1 Overview

The module enables EC access to PNPCFG and SWUC modules. It can access the host domain modules with host on alternate usage or take control of it and prevent any host from accessing that module.

7.13.2 Features

- Supports lock bit to prevent conflicts in host-controlled module
- Supports Super I/O I-Bus arbitration
- Supports Super I/O access lock violation indication

7.13.3 Functional Description

The EC2I bridge enables the EC to access the host Controlled module registers (e.g., host configuration module(PNPCFG) and SWUC), using the I-Bus which is arbitrated by I-Bus Arbiter to prevent I-Bus grant from fighting between EC and the host side. The bridge provides a lock bit to control the access of the host Controlled modules. When the related lock bit is cleared, the host is allowed to access to the host Controlled modules registers. When the related lock bit is set, the host is not allowed to access to the host Controlled module registers (i.e., write operations are ignored and read operations return the unknown). Whenever the host accesses to the locked register, a violation flag is set on the respective bit in the SIOLV register.

EC should access the host Controlled modules only after preventing host accessing to the module (using lock bits). The I-Bus arbiter arbitrates I-Bus usage between the host and EC. If a LPC transaction has started prior to the beginning of EC transaction, EC waiting for the completion of the LPC transaction. If EC transaction starts prior to LPC transaction, the LPC translation needs to wait for the completion of EC transaction.
EC firmware may access the host Controlled modules only when VSTBY is on and VCC is on and LPCCLK is active.

EC Read Operation from a Host Controlled module register, refer to the followings:
1. Set CSAE bit in IBCTL register.
2. Make sure that both CRIB and CWIB bits in IBCTL register are cleared.
3. Setting its enable bit in IBMAE register for access module, only one module can enable at a time.
4. Assign the offset of the register in the device in IHIOA register.
5. Write 1 to CRIB bit in IBCTL register.
6. Read the CRIB bit in IBCTL until it returns 0.
7. Read the data from IHD register.

EC Write Operation from a Host Controlled module register, refer to the followings:
1. Set CSAE bit in IBCTL register.
2. Make sure that both CRIB and CWIB bits in IBCTL register are cleared.
3. Setting its enable bit in IBMAE register for access module, only one module can enable at a time.
4. Assign the offset of the register in the device in IHIOA register.
5. Write the data to IHD register, which begins a write transaction.
6. Read the CWIB bit in IBCTL until it returns 0, which represents that a write transaction has been finished.
For minimal conflict between host and EC in the use of Host Controlled modules, refer to the followings:

Notice for Read/Write Operation
1. The host is allowed to access the host Controlled module only when the corresponding lock bit is cleared.

7.13.4 EC Interface Registers

The following set of registers is accessible only by the EC. The registers are maintained by VSTBY. The registers are listed below and the base address is 1200h.

Table 7-22. EC View Register Map, EC2I

7 ... 0	Offset
Indirect Host I/O Address Register (IHIOA)	00h
Indirect Host Data Register (IHD)	01h
Lock Super I/O Host Access Register (LSIOHA)	02h
Super I/O Access Lock Violation Register (SIOLV)	03h
EC to I-Bus Modules Access Enable Register (IBMAE)	04h
I-Bus Control Register (IBCTL)	05h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”.

7.13.4.1 Indirect Host I/O Address Register (IHIOA)

This register defines the host I/O address for read or write transactions initiated by EC from/to the host Controlled modules. The I/O address is an offset from the LSB bits of the address of the host controlled module. The accessed module is selected using EC to I-Bus Modules Access Enable Register (IBMAE).

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Indirect Host I/O Offset (IHIOO)** These bits indicate the offsets within the device range are allowed.

7.13.4.2 Indirect Host Data Register (IHD)

This register holds host data for read or write transactions initiated by EC from/to the host Controlled modules.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Indirect Host Data (IHDA)**

7.13.4.3 Lock Super I/O Host Access Register (LSIOHA)

This register controls locking of host access to the host Controlled modules.

Address Offset: 02h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	R/W	0b	**Lock BRAM Host Access (LKRTCHA)** 0: Host access to the BRAM registers is enabled. 1: Host access to the BRAM registers is disabled.
0	R/W	0b	**Lock PNPCFG Registers Host Access (LKCFG)** 0: Host access to the PNPCFG Registers is enabled. 1: Host access to the PNPCFG Registers is disabled.

7.13.4.4 Super I/O Access Lock Violation Register (SIOLV)

This register provides an error indication when a host lock violation occurs on Host Controlled modules access.

Address Offset: 03h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	-	0h	**Reserved**
0	R/WC	0b	**PNPCFG Register Lock Violation (CFGLV)** 0: There is no lock violation when the host accesses PNPCFG registers. 1: when the host accesses PNPCFG register but LKCFG bit in LSIOHA register is set, this bit is set to indicate a violation and can be write-1-clear.

7.13.4.5 EC to I-Bus Modules Access Enable Register (IBMAE)

This register enables EC access to the host Controlled modules. Only one of the bits in this register may be set at a time.

Address Offset: 04h

Bit	R/W	Default	Description
7-3	-	00h	**Reserved**
2	R/W	0b	**Mobile System Wake-Up Control (SWUC) Access Enable (SWUCAE)** 0: EC access to the SWUC Registers is disabled. 1: EC access to the SWUC Registers is enabled.
1	-	-	**Reserved**
0	R/W	0b	**PNPCFG Register EC Access Enable (CFGAE)** 0: EC access to the PNPCFG Registers is disabled. 1: EC access to the PNPCFG Registers is enabled.

7.13.4.6 I-Bus Control Register (IBCTL)

This register allows EC to the I-Bus Bridge operation.

Address Offset: 05h

Bit	R/W	Default	Description
7-4	-	0h	**Reserved**
3	-	-	**Reserved**
2	R	0b	**EC Write to I-Bus (CWIB)** Read: 1: EC write-access is still processing with IHD register. 0: It's completed.
1	R/W	0b	**EC Read from I-Bus (CRIB)** Write: See also CSAE bit definition. Read: 1: EC read-access is still processing. 0: It's completed and IHD register is available.
0	R/W	0b	**EC to I-Bus Access Enabled (CSAE)** 0: EC access to the I-Bus is disabled (default). 1: EC access to the I-Bus is enabled. The module to be accessed is selected in the IBMAE register. If 1 is written to both CSAE and CRIB, this access is a read-action. If 1 is written to CSAE and 0 to CRIB, this access is a write-action. If 0 is written to CSAE, the internal state machine of accessing is stopped.

7.13.5 EC2I Programming Guide

The read/write cycles PNPCFG and SWUC modules via EC2I are only valid when VCC is supplied. It means that such cycles may be executed after every VCC power-on.

Figure 7-20. Program Flow Chart for EC2I Read

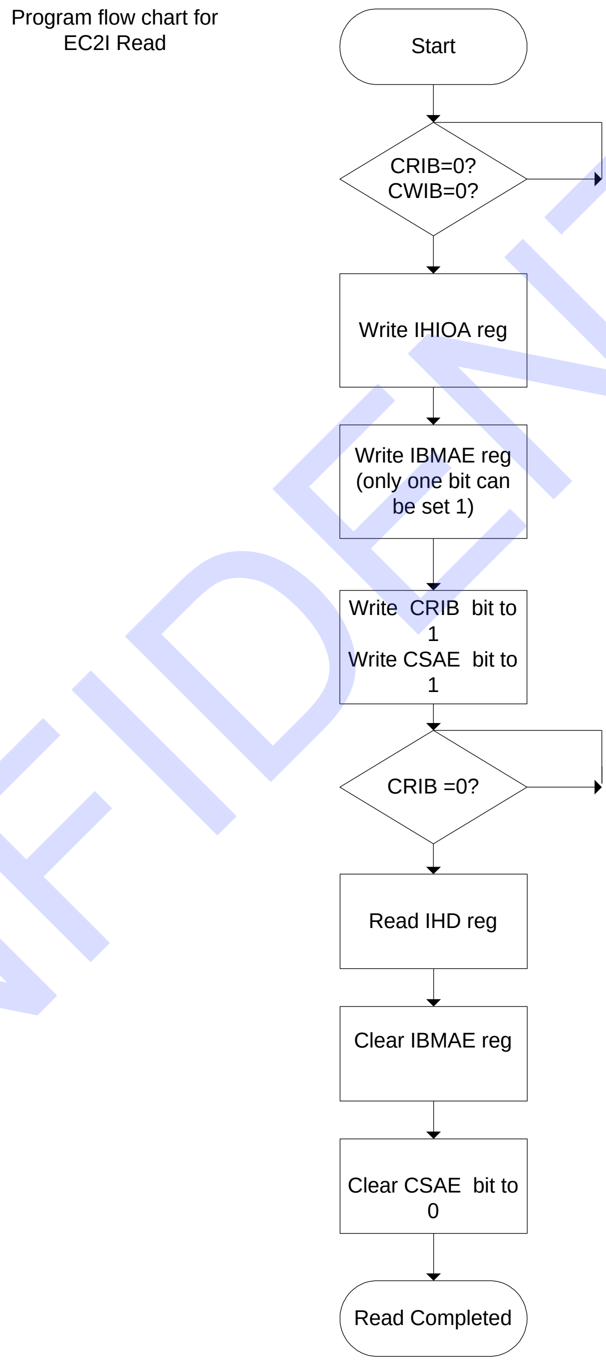
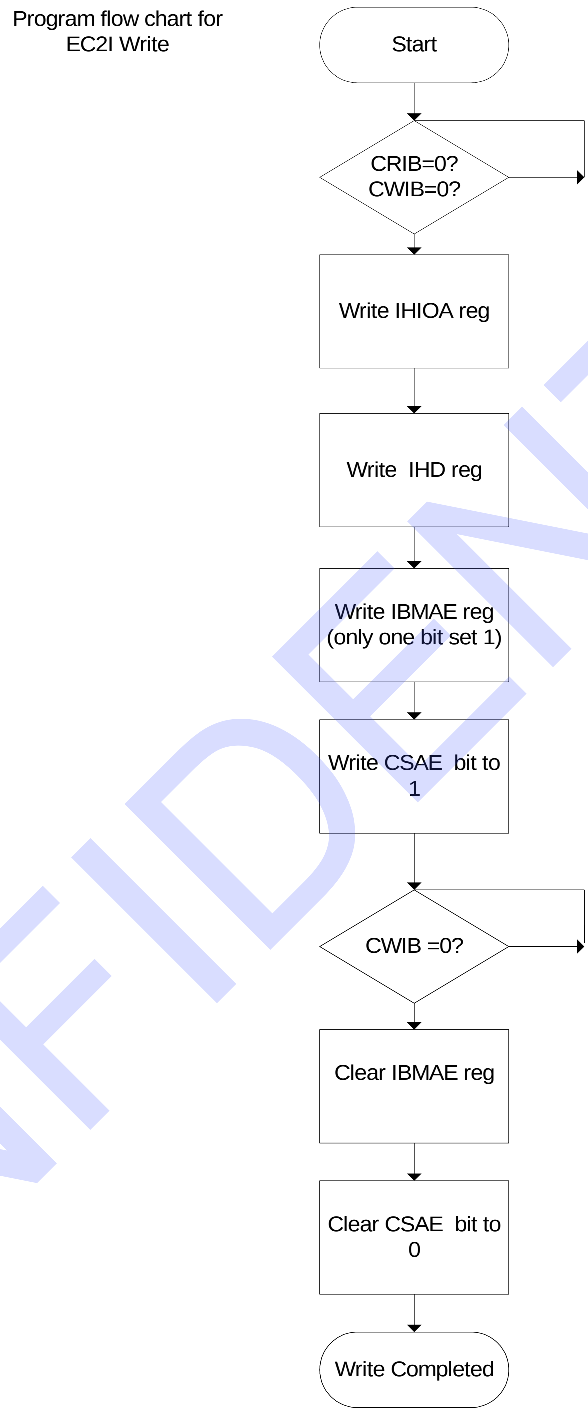


Figure 7-21. Program Flow Chart for EC2I Write



7.14 External Timer and External Watchdog (ETWD)

7.14.1 Overview

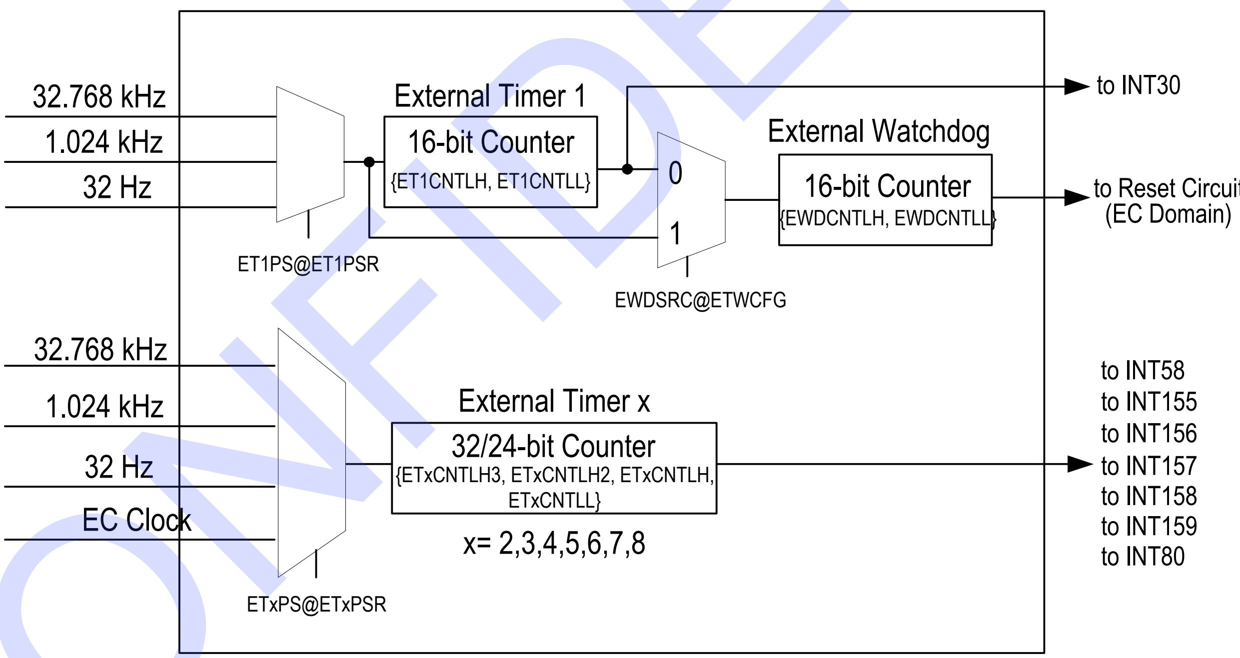
IT81202 implements 8 external timers outside CPU. External timer 1 can function as a watchdog timer (WDT) as well and the other 7 timers are without WDT function. All 8 timers are based on 32.768 k clock and still work when EC is in the Doze/Deep Doze/Sleep mode.

ETWD module cannot count external signal sources from pins. If the firmware wants to count external signal sources from pins, refer to TACH0A/B and TACH1A/B of tachometer inputs of PWM.

7.14.2 Features

- 32.768 kHz, 1.024 kHz and 32 Hz prescaler for External Timer 1
- 32.768 kHz, 1.024 kHz, 32 Hz, and EC clock prescaler for External Timer 2,3,4,5,6,7,8
- 16-bit count-down External Timer 1
- 24-bit count-down External Timer 2,3,5,7
- 32-bit count-down External Timer 4,6,8
- 16-bit count-down External WDT
- Timer 3 and 4, timer 5 and 6, timer 7 and 8 combinational mode

Figure 7-22. ETWD Simplified Diagram



7.14.3 Functional Description

7.14.3.1 External Timer Operation

The External Timer 1 is a 16-bit counter down timer, and the External Timer 2,3,4,5,6,7,8 are 24-bit count-down timers. Their clock sources are based on 32.768 k Clock and can be selected by a prescaler defined at ETxPS field in ETxPSR register.

The count number of External Timer 1 is defined in ET1CNTLH and ET1CNTLL registers, and that of External Timer 2/3/4/5/6/7/8 is defined in ETxCNTLH2, ETxCNTLH, and ETxCNTLL registers. External Timer 1/2 is

stopped after reset and started after writing data to ET1CNTLL/ET2CNTLL register and never stops until reset. External Timer 3/4/5/6/7/8 is stopped after reset and started after setting 1 to ETxEN register and can be disabled by setting 0 to ETxEN register.
It asserts an interrupt to INTC (see Table 7-23) when it counts to zero every time.

The External Timer 1/2 re-starts when
- it counts to zero periodically.
- data is written to ET1CNTLL/ET2CNTLL register.
- 1 is written to ET1RST/ET2RST bit in ETWCTRL register.

The External Timer 3/4/5/6/7/8 re-starts when
- it counts to zero periodically.
- 1 is written to ETxEN@ETxCTRL register.
- 1 is written to ET1RST/ET2RST bit in ETWCTRL register.

External Timer 1/2/3/4/5/6/7/8 asserts periodical interrupt to CPU when it counts to zero. The relationship between 8 timers and CPU interrupt source are listed below.

Table 7-23. ETWD Interrupt Mapping

Timer Channel	INT Number
External Timer 1	INT30
External Timer 2	INT58
External Timer 3	INT155
External Timer 4	INT156
External Timer 5	INT157
External Timer 6	INT158
External Timer 7	INT159
External Timer 8	INT80

7.14.3.2 External WDT Operation

External WDT is a 16-bit counter down timer. Its clock source is either External Timer 1 output or the same clock source of External Timer 1, and it is controlled by EWDSRC bit in ETWCFG register.

The count number is defined in EWDCNTLH and EWDCNTLL registers. External WDT is stopped after reset and started after writing data to EWDCNTLL register and can be stopped by setting EWDSCEN bit and EWDSCMS bit in ETWCTRL register. It asserts an External Watchdog Reset to EC domain when it counts to zero. External WDT requires starting External Timer 1 regardless of EWDSRC field in ETWCFG register. External WDT cannot be started until External Timer 1 is started.

The External WDT re-starts when it is touched by the firmware.
There are two following ways to touch (re-start) External WDT:
- Writing data to EWDCNTLL register (if LEWDCNTL bit in ETWCFG register is not set)
- Writing 5Ch to EWDKEYR register, called key-match

External WDT asserts an External Watchdog Reset to EC domain when
- it counts to zero.
- data except 5Ch is written to EWDKEYR register.

7.14.3.3 Combinational Mode

When the combinational mode, the Counter Observation value of Timer 4,6,8 will in incremental order.

7.14.4 EC Interface Registers

The following set of the registers is accessible only by the EC. They are listed below and the base address is

1F00h.

Table 7-24. EC View Register Map, ETWD

7 — 0	Offset
External Timer 1/WDT Configuration Register (ETWCFG)	01h
External Timer 1 Prescaler Register (ET1PSR)	02h
External Timer 1 Counter High Byte (ET1CNTLHR)	03h
External Timer 1 Counter Low Byte (ET1CNTLLR)	04h
External Timer 2 Prescaler Register (ET2PSR)	0Ah
External Timer 2 Counter High Byte (ET2CNTLHR)	0Bh
External Timer 2 Counter Low Byte (ET2CNTLLR)	0Ch
External Timer 2 Counter High Byte 2 (ET2CNTLH2R)	0Eh
External Timer/WDT Control Register (ETWCTRL)	05h
External WDT Counter High Byte (EWDCNTLHR)	09h
External WDT Counter Low Byte (EWDCNTLLR)	06h
External WDT Key Register (EWDKEYR)	07h
External Timer 3 Control Register (ET3CTRL)	10h
External Timer 3 Prescaler Register (ET3PSR)	11h
External Timer 3 Counter Low Byte (ET3CNTLLR)	14h
External Timer 3 Counter High Byte (ET3CNTLHR)	15h
External Timer 3 Counter High Byte 2 (ET3CNTLH2R)	16h
External Timer 4 Control Register (ET4CTRL)	18h
External Timer 4 Prescaler Register (ET4PSR)	19h
External Timer 4 Counter Low Byte (ET4CNTLLR)	1Ch
External Timer 4 Counter High Byte (ET4CNTLHR)	1Dh
External Timer 4 Counter High Byte 2 (ET4CNTLH2R)	1Eh
External Timer 4 Counter High Byte 3 (ET4CNTLH3R)	1Fh
External Timer 5 Control Register (ET5CTRL)	20h
External Timer 5 Prescaler Register (ET5PSR)	21h
External Timer 5 Counter Low Byte (ET5NTLLR)	24h
External Timer 5 Counter High Byte (ET5CNTLHR)	25h
External Timer 5 Counter High Byte 2 (ET5CNTLH2R)	26h
External Timer 6 Control Register (ET6CTRL)	28h
External Timer 6 Prescaler Register (ET6PSR)	29h
External Timer 6 Counter Low Byte (ET6CNTLLR)	2Ch
External Timer 6 Counter High Byte (ET6CNTLHR)	2Dh
External Timer 6 Counter High Byte 2 (ET6CNTLH2R)	2Eh
External Timer 6 Counter High Byte 3 (ET6CNTLH3R)	2Fh
External Timer 7 Control Register (ET7CTRL)	30h
External Timer 7 Prescaler Register (ET7PSR)	31h
External Timer 7 Counter Low Byte (ET7CNTLLR)	34h
External Timer 7 Counter High Byte (ET7CNTLHR)	35h
External Timer 7 Counter High Byte 2 (ET7CNTLH2R)	36h
External Timer 8 Control Register (ET8CTRL)	38h
External Timer 8 Prescaler Register (ET8PSR)	39h
External Timer 8 Counter Low Byte (ET8CNTLLR)	3Ch
External Timer 8 Counter High Byte (ET8CNTLHR)	3Dh
External Timer 8 Counter High Byte 2 (ET8CNTLH2R)	3Eh
External Timer 8 Counter High Byte 3 (ET8CNTLH3R)	3Fh
External Timer 1 Counter Observation Low Byte (ET1CNTOLR)	40h
External Timer 1 Counter Observation High Byte (ET1CNTOHR)	41h
External Timer 2 Counter Observation Low Byte (ET2CNTOLR)	44h
External Timer 2 Counter Observation High Byte (ET2CNTOHR)	45h
External Timer 2 Counter Observation High Byte 2 (ET2CNTOH2R)	46h

7	0	Offset
External Timer 3 Counter Observation Low Byte (ET3CNTOLR)		48h
External Timer 3 Counter Observation High Byte (ET3CNTOHR)		49h
External Timer 3 Counter Observation High Byte 2 (ET3CNTOH2R)		4Ah
External Timer 4 Counter Observation Low Byte (ET4CNTOLR)		4Ch
External Timer 4 Counter Observation High Byte (ET4CNTOHR)		4Dh
External Timer 4 Counter Observation High Byte 2 (ET4CNTOH2R)		4Eh
External Timer 4 Counter Observation High Byte 3 (ET4CNTOH3R)		4Fh
External Timer 5 Counter Observation Low Byte (ET5CNTOLR)		50h
External Timer 5 Counter Observation High Byte (ET5CNTOHR)		51h
External Timer 5 Counter Observation High Byte 2 (ET5CNTOH2R)		52h
External Timer 6 Counter Observation Low Byte (ET6CNTOLR)		54h
External Timer 6 Counter Observation High Byte (ET6CNTOHR)		55h
External Timer 6 Counter Observation High Byte 2 (ET6CNTOH2R)		56h
External Timer 6 Counter Observation High Byte 3 (ET6CNTOH3R)		57h
External Timer 7 Counter Observation Low Byte (ET7CNTOLR)		58h
External Timer 7 Counter Observation High Byte (ET7CNTOHR)		59h
External Timer 7 Counter Observation High Byte 2 (ET7CNTOH2R)		5Ah
External Timer 8 Counter Observation Low Byte (ET8CNTOLR)		5Ch
External Timer 8 Counter Observation High Byte (ET8CNTOHR)		5Dh
External Timer 8 Counter Observation High Byte 2 (ET8CNTOH2R)		5Eh
External Timer 8 Counter Observation High Byte 3 (ET8CNTOH3R)		5Fh
External WDT Counter Observation Low Byte (EWDCNTOLR)		60h
External WDT Counter Observation High Byte (EWDCNTOHR)		61h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”

7.14.4.1 External Timer 1/WDT Configuration Register (ETWCFG)

Address Offset: 01h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6	-	0b	**Reserved**
5	R/W	0b	**External WDT Key Enabled (EWDKEYEN)** 1: Enable the key match function to touch the WDT. 0: Otherwise.
4	R/W	0b	**External WDT Clock Source (EWDSRC)** 1: Select clock after prescaler of the external timer 1. 0: Select clock from the output of the external timer 1.
3	R/W	0b	**Lock EWDCNTLx Register (LEWDCNTL)** 1: Writing to EWDCNTL is ignored. 0: Writing to EWDCNTL is allowed.
2	R/W	0b	**Lock ET1CNTLx Registers (LET1CNTL)** 1: Writing to ET1CNTLL is ignored. 0: Writing to ET1CNTLL is allowed.
1	R/W	0b	**Lock ET1PS Register (LET1PS)** 1: Writing to ET1PS is ignored. 0: Writing to ET1PS is allowed.
0	R/W	0b	**Lock ETWCFG Register (LETWCFG)** 1: Writing to ETWCFG itself is ignored, and this bit can’t be cleared until reset. 0: Writing to ETWCFG itself is allowed.

7.14.4.2 External Timer 1 Prescaler Register (ET1PSR)

Address Offset: 02h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1-0	R/W	00b	**External Timer 1 Prescaler Select (ET1PS)** These bits control the clock input source to the external timer 1. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: Reserved Note the prescaler will not output clock until data is written to ET1CNTLLR register.

7.14.4.3 External Timer 1 Counter High Byte (ET1CNTLHR)

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 1 Counter High Byte (ET1CNTLH)** Define the count number of high byte of the 16-bit count-down timer.

7.14.4.4 External Timer 1 Counter Low Byte (ET1CNTLLR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 1 Counter Low Byte (ET1CNTLL)** Define the count number of low byte of the 16-bit count-down timer. The external timer 1 starts or re-starts after writing this register.

7.14.4.5 External Timer 2 Prescaler Register (ET2PSR)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R/W	00b	**External Timer 2 Prescaler Select (ET2PS)** These bits control the clock input source to the external timer 2. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: EC Clock Note the prescaler will not output clock until data is written to ET2CNTLLR register.

7.14.4.6 External Timer 2 Counter High Byte (ET2CNTLHR)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 2 Counter High Byte (ET2CNTLH)** Define the count number of high byte of the 24-bit count-down timer.

7.14.4.7 External Timer 2 Counter Low Byte (ET2CNTLLR)

Address Offset: 0Ch

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 2 Counter Low Byte (ET2CNTLL)** Define the count number of low byte of the 24-bit count-down timer. The external timer 2 starts or re-starts after writing this register.

7.14.4.8 External Timer 2 Counter High Byte 2 (ET2CNTLH2R)

Address Offset: 0Eh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 2 Counter High Byte 2 (ET2CNTLH2)** Define the count number of high byte 2 of the 24-bit count-down timer.

7.14.4.9 External Timer/WDT Control Register (ETWCTRL)

Address Offset: 05h

Bit	R/W	Default	Description
7-6	-	00b	**Reserved**
5	R/W	0b	**External WDT Stop Count Enable (EWDSCEN)** 1: External WDT is stopped counting. 0: Otherwise. This bit cannot be set until EWDSCMS bit is set to 1.
4	R/W	0b	**External WDT Stop Count Mode Select (EWDSCMS)** 1: External WDT can be stopped by setting EWDSCEN bit. 0: External WDT cannot be stopped. Writing data to this bit is ignored after writing data to EWDCNTLL register, and this bit cannot be cleared until being reset.
3	R	0b	**External Timer 2 Terminal Count (ET2TC)** 1: Indicates the external timer 2 has counted down to zero, and it is cleared after reading it. 0: Otherwise. Writing to this bit is ignored.
2	W	-	**External Timer 2 Reset (ET2RST)** Writing 1 forces the external timer 2 to re-start. Writing 0 is ignored. Read always returns zero.
1	R	0b	**External Timer 1 Terminal Count (ET1TC)** 1: Indicates the external timer 1 has counted down to zero, and it is cleared after reading it. 0: Otherwise Writing to this bit is ignored.
0	W	-	**External Timer 1 Reset (ET1RST)** Writing 1 forces the external timer 1 to re-start. Writing 0 is ignored. Read always returns zero.

7.14.4.10 External WDT Counter High Byte (EWDCNTLHR)

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	00h	**External WDT Counter High Byte (EWDCNTL)** Define the count number of high byte of the 16-bit count-down WDT.

7.14.4.11 External WDT Counter Low Byte (EWDCNTLLR)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	0Fh	**External WDT Counter Low Byte (EWDCNTLL)** Define the count number of 16-bit count-down WDT.

7.14.4.12 External WDT Key Register (EWDKEYR)

Address Offset: 07h

Bit	R/W	Default	Description
7-0	W	-	**External WDT Key (EWDKEY)** External WDT is re-started (touched) if 5Ch is written to this register. Writing with other values causes an External Watchdog Reset. This function is enabled by EWDKEYEN bit. Read returns unpredictable value.

7.14.4.13 External Timer 3 Control Register (ET3CTRL)

Address Offset: 10h

Bit	R/W	Default	Description
7-4	-	0000b	**Reserved**
3	R/W	0b	**External Timer 3 and Timer 4 Combine Mode (ET3ET4COMB)** In combinational mode, the timer 4 interrupt will be asserted when Timer 3 and Timer 4 all down count to 0. 1: Enable to combine timer 3 and timer 4. 0: Disable combine.
2	R	0b	**External Timer 3 Terminal Count (ET3TC)** 1: Indicates the external timer 3 has counted down to zero, and it is cleared after reading it. 0: Otherwise. Writing to this bit is ignored.
1	W	-	**External Timer 3 Reset (ET3RST)** Writing 1 forces the external timer 3 to re-start. Writing 0 is ignored. Read always returns zero.
0	R/W	0b	**External Timer 3 Enable Register (ET3EN)** 1: Enable timer. 0: Disable timer. When this bit is set from 0 to 1, the timer reloads the ET3CNTLL, ET3CNTLH, ET3CNTLH2 and start to count down.

7.14.4.14 External Timer 3 Prescaler Register (ET3PSR)

Address Offset: 11h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R/W	00b	**External Timer 3 Prescaler Select (ET3PS)** These bits control the clock input source to the external timer 3. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: EC Clock Note the prescaler will not output clock until ET3EN is enabled.

7.14.4.15 External Timer 3 Counter Low Byte (ET3CNTLLR)

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 3 Counter Low Byte (ET3CNTLL)** Define the count number of low byte of the 24-bit count-down timer.

7.14.4.16 External Timer 3 Counter High Byte (ET3CNTLHR)

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 3 Counter High Byte (ET3CNTLH)** Define the count number of high byte of the 24-bit count-down timer.

7.14.4.17 External Timer 3 Counter High Byte 2 (ET3CNTLH2R)

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 3 Counter High Byte 2 (ET3CNTLH2)** Define the count number of high byte 2 of the 24-bit count-down timer.

7.14.4.18 External Timer 4 Control Register (ET4CTRL)

Address Offset: 18h

Bit	R/W	Default	Description
7:3	-	00000b	**Reserved**
2	R	0b	**External Timer 4 Terminal Count (ET4TC)** 1: Indicates the external timer 4 has counted down to zero, and it is cleared after reading it. 0: Otherwise. Writing to this bit is ignored.
1	W	-	**External Timer 4 Reset (ET4RST)** Writing 1 forces the external timer 4 to re-start. Writing 0 is ignored. Read always returns zero.
0	R/W	0b	**External Timer 4 Enable Register (ET4EN)** 1: Enable timer. 0: Disable timer. When this bit is set from 0 to 1, the timer reloads the ET4CNTLL, ET4CNTLH, ET4CNTLH2 and start to count down.

7.14.4.19 External Timer 4 Prescaler Register (ET4PSR)

Address Offset: 19h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R/W	00b	**External Timer 4 Prescaler Select (ET4PS)** These bits control the clock input source to the external timer 4. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: EC Clock Note the prescaler will not output clock until ET4EN is enabled.

7.14.4.20 External Timer 4 Counter Low Byte (ET4CNTLLR)

Address Offset: 1Ch

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 4 Counter Low Byte (ET4CNTLL)** Define the count number of low byte of the 24-bit count-down timer.

7.14.4.21 External Timer 4 Counter High Byte (ET4CNTLHR)

Address Offset: 1Dh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 4 Counter High Byte (ET4CNTLH)** Define the count number of high byte of the 24-bit count-down timer.

7.14.4.22 External Timer 4 Counter High Byte 2 (ET4CNTLH2R)

Address Offset: 1Eh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 4 Counter High Byte 2 (ET4CNTLH2)** Define the count number of high byte 2 of the 24-bit count-down timer.

7.14.4.23 External Timer 4 Counter High Byte 3 (ET4CNTLH3R)

Address Offset: 1Fh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 4 Counter High Byte 3 (ET4CNTLH3)** Define the count number of high byte 3 of the 32-bit count-down timer.

7.14.4.24 External Timer 5 Control Register (ET5CTRL)

Address Offset: 20h

Bit	R/W	Default	Description
7:4	-	00000b	**Reserved**
3	R/W	0b	**External Timer 5 and Timer 6 Combine Mode (ET5ET6COMB)** In combinational mode, the timer 6 interrupt will be asserted when Timer 5 and Timer 6 all down count to 0. 1: Enable to combine timer 5 and timer 6. 0: Disable combine.
2	R	0b	**External Timer 5 Terminal Count (ET5TC)** 1: Indicates the external timer 5 has counted down to zero, and it is cleared after reading it. 0: Otherwise. Writing to this bit is ignored.
1	W	-	**External Timer 5 Reset (ET5RST)** Writing 1 forces the external timer 5 to re-start. Writing 0 is ignored. Read always returns zero.
0	R/W	0b	**External Timer 5 Enable Register (ET5EN)** 1: Enable timer. 0: Disable timer. When this bit is set from 0 to 1, the timer reloads the ET5CNTLL, ET5CNTLH, ET5CNTLH2 and start to count down.

7.14.4.25 External Timer 5 Prescaler Register (ET5PSR)

Address Offset: 21h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R/W	00b	**External Timer 5 Prescaler Select (ET5PS)** These bits control the clock input source to the external timer 5. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: EC Clock Note the prescaler will not output clock until ET5EN is enabled.

7.14.4.26 External Timer 5 Counter Low Byte (ET5CNTLLR)

Address Offset: 24h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 5 Counter Low Byte (ET5CNTLL)** Define the count number of low byte of the 24-bit count-down timer.

7.14.4.27 External Timer 5 Counter High Byte (ET5CNTLHR)

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 3 Counter High Byte (ET5CNTLH)** Define the count number of high byte of the 24-bit count-down timer.

7.14.4.28 External Timer 5 Counter High Byte 2 (ET5CNTLH2R)

Address Offset: 26h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 5 Counter High Byte 2 (ET5CNTLH2)** Define the count number of high byte 2 of the 24-bit count-down timer.

7.14.4.29 External Timer 6 Control Register (ET6CTRL)

Address Offset: 28h

Bit	R/W	Default	Description
7:3	-	00000b	**Reserved**
2	R	0b	**External Timer 6 Terminal Count (ET6TC)** 1: Indicates the external timer 6 has counted down to zero, and it is cleared after reading it. 0: Otherwise. Writing to this bit is ignored.
1	W	-	**External Timer 6 Reset (ET6RST)** Writing 1 forces the external timer 6 to re-start. Writing 0 is ignored. Read always returns zero.
0	R/W	0b	**External Timer 6 Enable Register (ET6EN)** 1: Enable timer. 0: Disable timer. When this bit is set from 0 to 1, the timer reloads the ET6CNTLL, ET6CNTLH, ET6CNTLH2 and start to count down.

7.14.4.30 External Timer 6 Prescaler Register (ET6PSR)

Address Offset: 29h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R/W	00b	**External Timer 6 Prescaler Select (ET6PS)** These bits control the clock input source to the external timer 6. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: EC Clock Note the prescaler will not output clock until ET6EN is enabled.

7.14.4.31 External Timer 6 Counter Low Byte (ET6CNTLLR)

Address Offset: 2Ch

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 6 Counter Low Byte (ET6CNTLL)** Define the count number of low byte of the 24-bit count-down timer.

7.14.4.32 External Timer 6 Counter High Byte (ET6CNTLHR)

Address Offset: 2Dh

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 6 Counter High Byte (ET6CNTLH)** Define the count number of high byte of the 24-bit count-down timer.

7.14.4.33 External Timer 6 Counter High Byte 2 (ET6CNTLH2R)

Address Offset: 2Eh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 6 Counter High Byte 2 (ET6CNTLH2)** Define the count number of high byte 2 of the 24-bit count-down timer.

7.14.4.34 External Timer 6 Counter High Byte 3 (ET6CNTLH3R)

Address Offset: 2Fh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 6 Counter High Byte 3 (ET6CNTLH3)** Define the count number of high byte 3 of the 32-bit count-down timer.

7.14.4.35 External Timer 7 Control Register (ET7CTRL)

Address Offset: 30h

Bit	R/W	Default	Description
7-4	-	0000b	**Reserved**
3	R/W	0b	**External Timer 7 and Timer 8 Combine Mode (ET7ET8COMB)** In combinational mode, the timer 8 interrupt will be asserted when Timer 8 and Timer 7 all down count to 0. 1: Enable to combine timer 7 and timer 8. 0: Disable combine.
2	R	0b	**External Timer 7 Terminal Count (ET7TC)** 1: Indicates the external timer 7 has counted down to zero, and it is cleared after reading it. 0: Otherwise. Writing to this bit is ignored.
1	W	-	**External Timer 7 Reset (ET7RST)** Writing 1 forces the external timer 7 to re-start. Writing 0 is ignored. Read always returns zero.
0	R/W	0b	**External Timer 7 Enable Register (ET7EN)** 1: Enable timer. 0: Disable timer. When this bit is set from 0 to 1, the timer reloads the ET7CNTLL, ET7CNTLH, ET7CNTLH2 and start to count down.

7.14.4.36 External Timer 7 Prescaler Register (ET7PSR)

Address Offset: 31h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**

Bit	R/W	Default	Description
1-0	R/W	00b	**External Timer 7 Prescaler Select (ET7PS)** These bits control the clock input source to the external timer 7. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: EC Clock Note the prescaler will not output clock until ET7EN is enabled.

7.14.4.37 External Timer 7 Counter Low Byte (ET7CNTLLR)

Address Offset: 34h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 7 Counter Low Byte (ET7CNTLL)** Define the count number of low byte of the 24-bit count-down timer.

7.14.4.38 External Timer 7 Counter High Byte (ET7CNTLHR)

Address Offset: 35h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 7 Counter High Byte (ET7CNTLH)** Define the count number of high byte of the 24-bit count-down timer.

7.14.4.39 External Timer 7 Counter High Byte 2 (ET7CNTLH2R)

Address Offset: 36h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 7 Counter High Byte 2 (ET7CNTLH2)** Define the count number of high byte 2 of the 24-bit count-down timer.

7.14.4.40 External Timer 8 Control Register (ET8CTRL)

Address Offset: 38h

Bit	R/W	Default	Description
7:3	-	00000b	**Reserved**
2	R	0b	**External Timer 8 Terminal Count (ET8TC)** 1: Indicates the external timer 8 has counted down to zero, and it is cleared after reading it. 0: Otherwise. Writing to this bit is ignored.
1	W	-	**External Timer 8 Reset (ET8RST)** Writing 1 forces the external timer 8 to re-start. Writing 0 is ignored. Read always returns zero.
0	R/W	0b	**External Timer 8 Enable Register (ET8EN)** 1: Enable timer. 0: Disable timer. When this bit is set from 0 to 1, the timer reloads the ET8CNTLL, ET8CNTLH, ET8CNTLH2 and start to count down.

7.14.4.41 External Timer 8 Prescaler Register (ET8PSR)

Address Offset: 39h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R/W	00b	**External Timer 8 Prescaler Select (ET8PS)** These bits control the clock input source to the external timer 8. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: EC Clock Note the prescaler will not output clock until ET8EN is enabled.

7.14.4.42 External Timer 8 Counter Low Byte (ET8CNTLLR)

Address Offset: 3Ch

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 8 Counter Low Byte (ET8CNTLL)** Define the count number of low byte of the 24-bit count-down timer.

7.14.4.43 External Timer 8 Counter High Byte (ET8CNTLHR)

Address Offset: 3Dh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 8 Counter High Byte (ET8CNTLH)** Define the count number of high byte of the 24-bit count-down timer.

7.14.4.44 External Timer 8 Counter High Byte 2 (ET8CNTLH2R)

Address Offset: 3Eh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 8 Counter High Byte 2 (ET8CNTLH2)** Define the count number of high byte 2 of the 24-bit count-down timer.

7.14.4.45 External Timer 8 Counter High Byte 3 (ET8CNTLH3R)

Address Offset: 3Fh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 8 Counter High Byte 3 (ET8CNTLH3)** Define the count number of high byte 3 of the 32-bit count-down timer.

7.14.4.46 External Timer 1 Counter Observation Low Byte (ET1CNTOLR)

Address Offset: 40h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 1 Counter Observation Low Byte (ET1CNTOL)** Observation of low byte of the 16-bit count-down timer.

7.14.4.47 External Timer 1 Counter Observation High Byte (ET1CNTOHR)

Address Offset: 41h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 1 Counter Observation High Byte (ET1CNTOH)** Observation of high byte of the 16-bit count-down timer.

7.14.4.48 External Timer 2 Counter Observation Low Byte (ET2CNTOLR)

Address Offset: 44h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 2 Counter Observation Low Byte (ET2CNTOL)** Observation of low byte of the 24-bit count-down timer.

7.14.4.49 External Timer 2 Counter Observation High Byte (ET2CNTOHR)

Address Offset: 45h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 2 Counter Observation High Byte (ET2CNTOH)** Observation of high byte of the 24-bit count-down timer.

7.14.4.50 External Timer 2 Counter Observation High Byte 2 (ET2CNTOH2R)

Address Offset: 46h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 2 Counter Observation High Byte 2 (ET2CNTOH2)** Observation of high byte 2 of the 24-bit count-down timer.

7.14.4.51 External Timer 3 Counter Observation Low Byte (ET3CNTOLR)

Address Offset: 48h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 3 Counter Observation Low Byte (ET3CNTOL)** Observation of low byte of the 24-bit count-down timer.

7.14.4.52 External Timer 3 Counter Observation High Byte (ET3CNTOHR)

Address Offset: 49h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 3 Counter Observation High Byte (ET3CNTOH)** Observation of high byte of the 24-bit count-down timer.

7.14.4.53 External Timer 3 Counter Observation High Byte 2 (ET3CNTOH2R)

Address Offset: 4Ah

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 3 Counter Observation High Byte 2 (ET3CNTOH2)** Observation of high byte 2 of the 24-bit count-down timer.

7.14.4.54 External Timer 4 Counter Observation Low Byte (ET4CNTOLR)

Address Offset: 4Ch

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 4 Counter Observation Low Byte (ET4CNTOL)** Observation of low byte of the 24-bit count-down timer.

7.14.4.55 External Timer 4 Counter Observation High Byte (ET4CNTOHR)

Address Offset: 4Dh

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 4 Counter Observation High Byte (ET4CNTOH)** Observation of high byte of the 24-bit count-down timer.

7.14.4.56 External Timer 4 Counter Observation High Byte 2 (ET4CNTOH2R)

Address Offset: 4Eh

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 4 Counter Observation High Byte 2 (ET4CNTOH2)** Observation of high byte 2 of the 24-bit count-down timer.

7.14.4.57 External Timer 4 Counter Observation High Byte 3 (ET4CNTOH3R)

Address Offset: 4Fh

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 4 Counter Observation High Byte 3 (ET4CNTOH3)** Observation of high byte 3 of the 32-bit count-down timer.

7.14.4.58 External Timer 5 Counter Observation Low Byte (ET5CNTOLR)

Address Offset: 50h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 5 Counter Observation Low Byte (ET5CNTOL)** Observation of low byte of the 24-bit count-down timer.

7.14.4.59 External Timer 5 Counter Observation High Byte (ET5CNTOHR)

Address Offset: 51h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 5 Counter Observation High Byte (ET5CNTOH)** Observation of high byte of the 24-bit count-down timer.

7.14.4.60 External Timer 5 Counter Observation High Byte 2 (ET5CNTOH2R)

Address Offset: 52h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 5 Counter Observation High Byte 2 (ET5CNTOH2)** Observation of high byte 2 of the 24-bit count-down timer.

7.14.4.61 External Timer 6 Counter Observation Low Byte (ET6CNTOLR)

Address Offset: 54h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 6 Counter Observation Low Byte (ET6CNTOL)** Observation of low byte of the 24-bit count-down timer.

7.14.4.62 External Timer 6 Counter Observation High Byte (ET6CNTOHR)

Address Offset: 55h

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 6 Counter Observation High Byte (ET6CNTOH)** Observation of high byte of the 24-bit count-down timer.

7.14.4.63 External Timer 6 Counter Observation High Byte 2 (ET6CNTOH2R)

Address Offset: 56h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 6 Counter Observation High Byte 2 (ET6CNTOH2)** Observation of high byte 2 of the 24-bit count-down timer.

7.14.4.64 External Timer 6 Counter Observation High Byte 3 (ET6CNTOH3R)

Address Offset: 57h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 6 Counter Observation High Byte 3 (ET6CNTOH3)** Observation of high byte 3 of the 32-bit count-down timer.

7.14.4.65 External Timer 7 Counter Observation Low Byte (ET7CNTOLR)

Address Offset: 58h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 7 Counter Observation Low Byte (ET7CNTOL)** Observation of low byte of the 24-bit count-down timer.

7.14.4.66 External Timer 7 Counter Observation High Byte (ET7CNTOHR)

Address Offset: 59h

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 7 Counter Observation High Byte (ET7CNTOH)** Observation of high byte of the 24-bit count-down timer.

7.14.4.67 External Timer 7 Counter Observation High Byte 2 (ET7CNTOH2R)

Address Offset: 5Ah

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 7 Counter Observation High Byte 2 (ET7CNTOH2)** Observation of high byte 2 of the 24-bit count-down timer.

7.14.4.68 External Timer 8 Counter Observation Low Byte (ET8CNTOLR)

Address Offset: 5Ch

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 8 Counter Observation Low Byte (ET8CNTOL)** Observation of low byte of the 24-bit count-down timer.

7.14.4.69 External Timer 8 Counter Observation High Byte (ET8CNTOHR)

Address Offset: 5Dh

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 8 Counter Observation High Byte (ET8CNTOH)** Observation of high byte of the 24-bit count-down timer.

7.14.4.70 External Timer 8 Counter Observation High Byte 2 (ET8CNTOH2R)

Address Offset: 5Eh

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 8 Counter Observation High Byte 2 (ET8CNTOH2)** Observation of high byte 2 of the 24-bit count-down timer.

7.14.4.71 External Timer 8 Counter Observation High Byte 3 (ET8CNTOH3R)

Address Offset: 5Fh

Bit	R/W	Default	Description
7-0	R	FFh	**External Timer 8 Counter Observation High Byte 3 (ET8CNTOH3)** Observation of high byte 3 of the 32-bit count-down timer.

7.14.4.72 External WDT Counter Observation Low Byte (EWDCNTOLR)

Address Offset: 60h

Bit	R/W	Default	Description
7-0	R	0Fh	**External WDT Counter Observation Low Byte (EWDCNTOL)** Observation of low byte of the 16-bit count-down WDT.

7.14.4.73 External WDT Counter Observation High Byte (EWDCNTOHR)

Address Offset: 61h

Bit	R/W	Default	Description
7-0	R	00h	**External WDT Counter Observation High Byte (EWDCNTOH)** Observation of high byte of the 16-bit count-down WDT.

7.14.5 ETWD Programming Guide

For byte access observation of External Timer 0 counter
Step 1. Read External Timer 1 Counter Observation Low Byte. (This step is for latching current counter control. Its value is not correct.)
Step 2. Read External Timer 1 Counter Observation Low Byte. (The real value)
Step 3. Read External Timer 1 Counter Observation High Byte. (The real value)

7.15 General Control (GCTRL)

7.15.1 Overview

This module controls EC function that doesn't belong to the specified module.

7.15.2 Features

- By module reset
- Hardwired SHA-1

7.15.3 Functional Description

Wait Next Clock Rising:
When 0 is written to WNCKR register, the CPU will be paused and wait for a low to high transition of the internal 65.536 kHz clock. This may be useful to get a delay.

For a loop that writing 0 to WNCKR register for N times, the delay value will be
((N-1) / 65.536 kHz) to (N / 65.536 kHz)

e.g.
Consecutively writing 0 to WNCKR register for 33 times get 0.5ms delay with –2.3% ~ +0.7% tolerance.
Consecutively writing 0 to WNCKR register for 66 times get 1ms delay with –0.8% ~ +0.7% tolerance.
Consecutively writing 0 to WNCKR register for 132 times get 2ms delay with –0.05% ~ +0.7% tolerance.

SHA-1 Hash Calculation: SHA-1 use 32 * 4 = 128-byte in Scratch SRAM. HASHBADDR1 is the base address of the 128-byte in Scratch SRAM. HASHBADDR1 must be located at 128-byte boundary.

SHA-1 Program Flow:

1. Load 32-bit word data (W[0] ~ W[15],H0~H4,K0~k3) to SRAM.
2. Write HASHBADDR1 @ SHA1HBADDR
3. Write 1 to SHA1SCTRL @ SHA1HASHCTRLR
4. H0 to H4 will be updated.

Table 7-25. SHA-1 Scratch SRAM Usage Map

W[0] is 4-byte data and located at address [HASHBADDR1 + (00 * 4)].
W[1] is 4-byte data and located at address [HASHBADDR1 + (01 * 4)].
W[2] is 4-byte data and located at address [HASHBADDR1 + (02 * 4)].
W[3] is 4-byte data and located at address [HASHBADDR1 + (03 * 4)].
W[4] is 4-byte data and located at address [HASHBADDR1 + (04 * 4)].
W[5] is 4-byte data and located at address [HASHBADDR1 + (05 * 4)].
W[6] is 4-byte data and located at address [HASHBADDR1 + (06 * 4)].
W[7] is 4-byte data and located at address [HASHBADDR1 + (07 * 4)].
W[8] is 4-byte data and located at address [HASHBADDR1 + (08 * 4)].
W[9] is 4-byte data and located at address [HASHBADDR1 + (09 * 4)].
W[10] is 4-byte data and located at address [HASHBADDR1 + (10 * 4)].
W[11] is 4-byte data and located at address [HASHBADDR1 + (11 * 4)].
W[12] is 4-byte data and located at address [HASHBADDR1 + (12 * 4)].
W[13] is 4-byte data and located at address [HASHBADDR1 + (13 * 4)].
W[14] is 4-byte data and located at address [HASHBADDR1 + (14 * 4)].
W[15] is 4-byte data and located at address [HASHBADDR1 + (15 * 4)].
Reserved
Reserved
Reserved
Reserved
Reserved
H0 is 4-byte data and located at address [HASHBADDR1 + (21 * 4)].
H1 is 4-byte data and located at address [HASHBADDR1 + (22 * 4)].
H2 is 4-byte data and located at address [HASHBADDR1 + (23 * 4)].
H3 is 4-byte data and located at address [HASHBADDR1 + (24 * 4)].
H4 is 4-byte data and located at address [HASHBADDR1 + (25 * 4)].
Reserved
Reserved
K0 is 4-byte data and located at address [HASHBADDR1 + (28 * 4)].
K1 is 4-byte data and located at address [HASHBADDR1 + (29 * 4)].
K2 is 4-byte data and located at address [HASHBADDR1 + (30 * 4)].
K3 is 4-byte data and located at address [HASHBADDR1 + (31 * 4)].

7.15.4 EC Interface Registers

The following set of the registers is accessible only by EC. They are listed below and the base address is 2000h.

Table 7-26. EC View Register Map, GCTRL

7 0	Offset
Chip ID Byte 1 (ECHIPID1)	85h
Chip ID Byte 2 (ECHIPID2)	86h
Chip ID Byte 3 (ECHIPID3)	87h
Chip Version (ECHIPVER)	02h
Reserved	03h
Identify Input Register (IDR)	04h
Reserved	05h
Reset Status (RSTS)	06h
Reset Control 1 (RSTC1)	07h
Reset Control 2 (RSTC2)	08h
Reset Control 3 (RSTC3)	09h
Reset Control 4 (RSTC4)	11h
Reset Control DMM (RSTDMMC)	10h
Base Address Select (BADRSEL)	0Ah

7 ... 0	Offset
Wait Next Clock Rising (WNCKR)	0Bh
Special Control 1 (SPCTRL1)	0Dh
Reset Control Host Side (RSTCH)	0Eh
Generate IRQ (GENIRQ)	0Fh
Special Control 2 (SPCTRL2)	12h
Reserved	16h
Port I2EC High-Byte Register (PI2ECH)	14h
Port I2EC Low-Byte Register (PI2ECL)	15h
BRAM Interrupt Address 0 Register (BINTADDR0R)	19h
BRAM Interrupt Address 1 Register (BINTADDR1R)	1Ah
BRAM Interrupt Control Register (BINTCTRLR)	1Bh
Special Control 4 (SPCTRL4)	1Ch
Eflash DMA 4KB Select Register (EDMA4SR)	27h
SHA-1 Hash Control Register (SHA1HASHCTRLR)	2Dh
SHA-1 Hash Base Address Register (SHA1HBADDR)	2Eh
Memory Controller Configuration Register (MCCR)	30h
External ILM/DLM Size Register (EIDSR)	31h
Pin Multi-function Enable Register 1 (PMER1)	32h
Pin Multi-function Enable Register 2 (PMER2)	33h
Pin Multi-function Enable Register 3 (PMER3)	46h
Fix Region Register 0 (FRR0)	34h
Fix Region Register 1 (FRR1)	35h
Fix Region Register 2 (FRR2)	36h
Eflash Protect Lock Register (EPLR)	37h
Sensor Interrupt Switch Select Register 0 (SISSR0)	38h
Sensor Interrupt Switch Select Register 1 (SISSR1)	39h
Sensor Interrupt Switch Select Register 2 (SISSR2)	3Ah
Sensor Interrupt Switch Select Register 3 (SISSR3)	3Bh
Sensor Interrupt Switch Select Register 4 (SISSR4)	3Ch
Sensor Interrupt Switch Select Register 5 (SISSR5)	3Dh
Memory Controller Configuration Register 1 (MCCR1)	3Eh
DLM Size Reduce Control Flag Register 0 (DSRCFR0)	42h
DLM Size Reduce Control Flag Register 1 (DSRCFR1)	43h
Memory Controller Configuration Register 2 (MCCR2)	44h
Memory Controller Configuration Register 3 (MCCR3)	20h
Dummy Register (DMR)	45h
ETWD and UART Control Register (ETWDUARTCR)	4Bh
Wakeup MCU Control Register (WMCR)	4Ch
Mailbox Message Register (MMR)	4Dh
EC Interrupt Request Register (EIRR)	4Eh
DIM Base Address Register 0 (DIMBA0)	3Fh
DIM Base Address Register 1 (DIMBA1)	40h
Interrupt Vector Table Base Address Register (IVTBAR)	41h
Port 80h/81h Status Register (P80H81HSR)	50h
Port 80h Data Register (P80HDR)	51h
Port 81h Data Register (P81HDR)	52h
H2RAM Offset Register (H2ROFSR)	53h
Eflash 1K R/W Protect Control Register0 For Path From EC	55h
Eflash 1K R/W Protect Control Register1 For Path From EC	56h
Eflash 1K R/W Protect Control Register0 For Path From DBGR	57h
Eflash 1K R/W Protect Control Register1 For Path From DBGR	58h
Eflash 1K R/W Protect Control Register0 For Path From Host	59h
Eflash 1K R/W Protect Control Register1 For Path From Host	5Ah

7 — 0	Offset
Hardware ECC Function Control Register (HWECCFCR)	5Bh
Hardware ECC Function Control Register1 (HWECCFCR1)	5Ch
RISCV ILM Configuration Register 0 (RVILMCR0)	5Dh
RISCV ILM Configuration Register 1 (RVILMCR1)	5Eh
RISCV ILM Configuration Register 2 (RVILMCR2)	5Fh
Eflash Write Protect Register 0~15 For Path From Host (EWPR0PFH~EWPR15PFH)	60h~6Fh
Eflash Read Protect Register 0~15 For Path From Host (ERPR0PFH~ERPR15PFH)	70h~7Fh
Eflash Write Protect Register 0~15 For Path From DBGR (EWPR0PFD~EWPR15PFD)	A0h~Afh
Eflash Read Protect Register 0~15 For Path From DBGR (ERPR0PFD~ERPR15PFD)	B0h~Bfh
Eflash Write Protect Register 0~15 For Path From EC (EWPR0PFEC~EWPR15PFEC)	C0h~Cfh
Eflash Read Protect Register 0~15 For Path From EC (ERPR0PFEC~ERPR15PFEC)	D0h~Dfh

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”.

7.15.4.1 Chip ID Byte 1 (ECHIPID1)

The content of this EC side register is the same as that of the CHIPID1 register in the host side.

Address Offset: 85h

Bit	R/W	Default	Description
7-0	R	08h	**Chip ID Byte 1 (ECHIPID1)** This register contains the Chip ID byte 1.

7.15.4.2 Chip ID Byte 2 (ECHIPID2)

The content of this EC side register is the same as that of the CHIPID2 register in the host side.

Address Offset: 86h

Bit	R/W	Default	Description
7-0	R	12h	**Chip ID Byte 2 (ECHIPID2)** This register contains the Chip ID byte 2.

7.15.4.3 Chip ID Byte 3 (ECHIPID3)

The content of this EC side register is the same as that of the CHIPID3 register in the host side.

Address Offset: 87h

Bit	R/W	Default	Description
7-0	R	02h	**Chip ID Byte 3 (ECHIPID3)** This register contains the Chip ID byte 3.

7.15.4.4 Chip Version (ECHIPVER)

This register contains revision ID of this chip.
The content of this EC side register is the same as that of the CHIPVER register in the host side.

Address Offset: 02h

Bit	R/W	Default	Description
7-4	R	-	**Embedded Flash Size** Ah: 0KB 4h: 256KB 8h: 512KB Ch: 1MB
3-0	R	1h	**Chip Version (ECHIPVER)**

7.15.4.5 Identify Input Register (IDR)

Address Offset: 04h

Bit	R/W	Default	Description
7	R	-	**Identify Input 7 (ID7)**
6	R	-	**Identify Input 6 (ID6)**
5	R	-	**Identify Input 5 (ID5)**
4	R	-	**Identify Input 4 (ID4)**
3	R	-	**Identify Input 3 (ID3)**
2	R	-	**Identify Input 2 (ID2)**
1	R	-	**Identify Input 1 (ID1)**
0	R	-	**Identify Input 0 (ID0)**

7.15.4.6 Reset Status (RSTS)

Address Offset: 06h

Bit	R/W	Default	Description
7-6	R/W	10b	**VCC Detector Option (VCCDO)** 00b: The VCC power status is treated as power-off. 01b: The VCC power status is treated as power-on. otherwise: reserved No matter which option is selected, the VCC power status is always recognized as power-off if LPCPD# input is level low. The VCC power status is used as internal “power good” signal to prevent current leakage while VCC is off. The current VCC power status can be read from VCCPO bit in SWCTL1 register in section 6.5.5.1 on page 152. Intentionally toggling this field when VCC is supplied can reset logic VCC domain in EC.
5	R/W	-	**VFSPI Power Good (VFSPIPG)** The written data of this bit is used as an internal "power good" signal to avoid current leakage while VFSPI is off. 0b: The power status of VFSPI is treated as power-on. 1b: The power status of VFSPI is treated as power-off.
4	-	-	**Reserved**

Bit	R/W	Default	Description
3	R/W	1b	**Host Global Reset (HGRST)** 0: The reset source of PNPCFG is RSTPNP bit in RSTCH register and WRST#. 1: The reset source of PNPCFG are RSTPNP bit in RSTCH register, internal VCC status controlled by VCCDO bit in RSTS register, LPCPD#, LPCRST# and WRST#.
2	R/W	1b	**Global Reset (GRST)** This bit controls whether to reset EC domain globally during Internal/External Watchdog Reset. 0: Only reset CPU, and each module can be reset by RSTCn register 1: Reset all the EC domain
1-0	R/WC	-	**Last Reset Source (LRS)** These bits indicate the last reset source. To clear them, write a one to bit 0. If this register field is used, it is required to write 11b to this field once and only one time after reset. 00b, 01b: VSTBY Power-Up Reset or Warm Reset 10b: Internal Watchdog Reset 11b: External Watchdog Reset

7.15.4.7 Reset Control 1 (RSTC1)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).
Refer to VCCDO field in RSTS register to reset logic in VCC domain in EC.

Address Offset: 07h

Bit	R/W	Default	Description
7	W	-	**Reset SMFI (RSMFI)**
6	W	-	**Reset INTC (RINTC)**
5	W	-	**Reset EC2I (REC2I)**
4	W	-	**Reset KBC (RKBC)**
3	W	-	**Reset SWUC (RSWUC)**
2	W	-	**Reset PMC (RPMC)**
1	W	-	**Reset GPIO (RGPIO)**
0	W	-	**Reset PWM (RPWM)**

7.15.4.8 Reset Control 2 (RSTC2)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 08h

Bit	R/W	Default	Description
7	W	-	**Reset ADC (RADC)**
6	-	-	**Reserved**
5	W	-	**Reset WUC (RWUC)**
4	W	-	**Reset KBS (RKBS)**
3	W	-	**Reset SMBus Channel F (RSMBF)**
2	-	-	**Reserved**
1	-	-	**Reserved**
0	W	-	**Reset USBPD (RUSBPD)**

7.15.4.9 Reset Control 3 (RSTC3)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 09h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	W	-	**Reset SMBus Channel D (RSMBD)**
2	W	-	**Reset SMBus Channel C (RSMBC)**
1	W	-	**Reset SMBus Channel B (RSMBB)**
0	W	-	**Reset SMBus Channel A (RSMBA)** To reset the logic of SMBus shared with all channels, write 1111b to bit 3-0 at the same time and writing 0111b is reserved.

7.15.4.10 Reset Control 4 (RSTC4)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 11h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	W	-	**Reset SMBus Channel E (RSMBE)**
5	-	-	**Reserved**
4	W	-	**Reset PECI (RPECI)**
3	-	-	**Reserved**
2	W	-	**Reset UART2 (RUART2)**
1	W	-	**Reset UART1 (RUART1)**
0	W	-	**Reset SSPI (RSSPI)**

7.15.4.11 Reset Control DMM (RSTDMMC)

Determine whether a double-mapping module belongs to the host or EC side.

Address Offset: 10h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**UART1 SIDE (UART1SD)** 1: UART1 belongs to the EC side. For its clock, refer to section 7.7.3.5 Auto Clock Gating (AUTOCG) on page 263. 0: UART1 belongs to the host side and it will be reset during Host Domain Hardware/Software reset. Its clock is off if VCC is off.
2	R/W	0b	**UART2 SIDE (UART2SD)** 1: UART2 belongs to the EC side. For its clock, refers to section 7.7.3.5 Auto Clock Gating (AUTOCG) on page 263. 0: UART2 belongs to the host side and it will be reset during Host Domain Hardware/Software reset. Its clock is off if VCC is off.
1	R/W	1b	**SSPI SIDE (SSPISD)** 1: SSPI belongs to the EC side. For its clock, refer to section 7.7.3.5 Auto Clock Gating (AUTOCG) on page 263. 0: SSPI belongs to the host side and it will be reset during Host Domain Hardware/Software reset. Its clock is off if VCC is off.
0	-	-	**Reserved**

7.15.4.12 Base Address Select (BADRSEL)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Base Address (BADDR1-0)** 00b: The register pair to access PNPCFG is 002Eh and 002Fh. 01b: The register pair to access PNPCFG is 004Eh and 004Fh. 10b: The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR. 11b: Reserved

7.15.4.13 Wait Next Clock Rising (WNCKR)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	W	-	**Wait Next 65K Rising (WN65K)** Writing 00h to this register and the CPU program counter will be paused until the next low to high transition of 65.536 kHz clock. Writing other values is reserved.

7.15.4.14 Special Control 1 (SPCTRL1)

Address Offset: 0Dh

Bit	R/W	Default	Description
7	R/W	0b	**P80L Enable (P80LEN)** This bit will be set if 1 is written and cleared if 1 is written or there is a VCC on->off transition. This bit is supplied by the VSTBY power. Refer to section 7.16.4 P80L on page 458. 1b: Enable P80L function. 0b: Otherwise
6	R/W	0b	**Accept Port 80h Cycle (ACP80)** This bit will be set if 1 is written and cleared if 1 is written or there is a VCC on->off transition. This bit is supplied by the VSTBY power. Refer to section 7.16.4 P80L on page 458. 1b: The host LPC I/O cycle with address 80h will be accepted by EC. If P80LEN is set, enabling this bit to guarantee LPC I/O port 80h data can be latched even though there is a transaction cycle to BRAM. 0b: Otherwise
5-4	-	-	**Reserved**
3	R/W	0b	**Accept Port 81h Cycle (ACP81)** This bit will be set if 1 is written and cleared if 1 is written or there is a VCC on->off transition. This bit is supplied by the VSTBY power. Refer to section 7.16.4 P80L on page 458. 1b: The host LPC I/O cycle with address 81h will be accepted by EC. If P80LEN is set, enabling this bit to guarantee LPC I/O port 81h data can be latched even though there is a transaction cycle to BRAM. 0b: Otherwise
2	-	-	**Reserved**

Bit	R/W	Default	Description
1-0	R/W	00b	**I2EC Control (I2ECCTRL)** 00b: I2EC is disabled. 10b: I2EC is read-only. 11b: I2EC is read-write. 01b: Reserved Refer to section 7.22.4.5 EC Memory Snoop (ECMS) on page 533.

7.15.4.15 Reset Control Host Side (RSTCH)

Address Offset: 0Eh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	W	-	**Reset PNPCFG (RSTPNP)**
1-0	-	-	**Reserved**

7.15.4.16 Generate IRQ (GENIRQ)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	W	-	**Generate IRQ Number (GENIRQNUM)** Writing to this field will generate SERIRQ with a specified number. This field is valid only when it is between 1-12 or 14-15.

7.15.4.17 Special Control 2 (SPCTRL2)

Address Offset: 12h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Port I2EC Enable (PI2ECEN)** 1b: Decode I2EC cycles via address I2EC_XADDR. 0b: Otherwise Refer to section 7.22.4.5 EC Memory Snoop (ECMS) on page 533.

7.15.4.18 Special Control 4 (SPCTRL4)

Address Offset: 1Ch

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/WC	-	**Last Reset Source Is Warm Reset (LRSIWR)** To clear this bit, write a one to it. 0b: Last reset is not generated from Warm reset function. 1b: Last reset source is Warm reset.
1	R/WC	-	**Last Reset Source Is PWRSW Timeout Reset (LRSIPWRSWTR)** If this bit is used, it is required to write 1 to this bit once and only one time after reset. 0b: Last reset is not generated from PWRSW timeout reset function. 1b: Last reset source is PWRSW timeout reset. Write 1: Clear this bit Write 0: No action

Bit	R/W	Default	Description
0	R/WC	-	**Last Reset Source Is Power Good Watch Reset (LRSIPGWR)** If this bit is used, it is required to write 1 to this bit once and only one time after reset. 0b: Last reset is not generated from power good watch reset function. 1b: Last reset source is power good watch reset. Write 1: Clear this bit Write 0: No action

7.15.4.19 Port I2EC High-Byte Register (PI2ECH)

LPC I/O port with address equal to PORT_I2EC[15:0] + 1: I2EC_XADDR_H
LPC I/O port with address equal to PORT_I2EC[15:0] + 2: I2EC_XADDR_L
LPC I/O port with address equal to PORT_I2EC[15:0] + 3: I2EC_XDATA
EC only accepts the LPC I/O cycle with PORT_I2EC address if PI2ECEN bit in SPCTRL2 register is set.

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R/W	03h	**Port I2EC[15:8] (PORT_I2EC[15:8])** High-byte address of I/O port for I2EC purpose. Bit 7-4 (PORT_I2EC[15:12]) are forced to 0000b and can't be written.

7.15.4.20 Port I2EC Low-Byte Register (PI2ECL)

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R/W	80h	**Port I2EC[7:0] (PORT_I2EC[7:0])** Low-byte address of I/O port for I2EC purpose. Bit 1-0 (PORT_I2EC[1:0]) are forced to 00b and can't be written.

7.15.4.21 BRAM Interrupt Address 0 Register (BINTADDR0R)

BINTADDR0R, BINTADDR1R and BINTCTRLR are used for I2BRAM function.

Address Offset: 19h

Bit	R/W	Default	Description
7-0	R/W	00h	**BRAM Interrupt Address 0 (BINTADDR0)** When the host side writes data to BRAM and the address offset equals to the value of BINTADDR0, the interrupt source, INT71, will be issued. In addition, this function will be activated only when BINTA0EN bit is set. Notice that BRAM interrupt address range must be set from 2280h to 22BFh.

7.15.4.22 BRAM Interrupt Address 1 Register (BINTADDR1R)

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**BRAM Interrupt Address 1 (BINTADDR1)** When the host side writes data to BRAM and the address offset equals to the value of BINTADDR1, the interrupt source, INT71, will be issued. In addition, this function will be activated only when BINTA1EN bit is set. Notice that BRAM interrupt address range must be set from 2280h to 22BFh.

7.15.4.23 BRAM Interrupt Control Register (BINTCTRLR)

Address Offset: 1Bh

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/WC	0b	**BRAM Interrupt Address 1 Match Status (BINTA1MSTS)** This bit will be set when the host side writes data to BRAM address offset, BINTADDR1 and it will be write-one-cleared.
4	R/WC	0b	**BRAM Interrupt Address 0 Match Status (BINTA0MSTS)** This bit will be set when host side writes data to BRAM address offset, BINTADDR0 and it will be write-one-cleared.
3-2	-	-	**Reserved**
1	R/W	0b	**BRAM Interrupt Address 1 Enable (BINTA1EN)** 0b: BRAM interrupt address 1 function is disabled. 1b: BRAM interrupt address 1 function is enabled.
0	R/W	0b	**BRAM Interrupt Address 0 Enable (BINTA0EN)** 0b: BRAM interrupt address 0 function is disabled. 1b: BRAM interrupt address 0 function is enabled.

7.15.4.24 Eflash DMA 4KB Select Register (EDMA4SR)

Address Offset: 27h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R/W	0b	**Eflash DMA 4KB select for ILM16~ILM23** These registers select which 4K eflash DMA is in the selected ILM16~ILM23. 000b: 0~4kB 001b: 4kB~8kB 010b: 8kB~12kB 011b: 12kB~16kB 100b: 16kB~20kB 101b: 20kB~24kB 110b: 24kB~28kB 111b: 28kB~32kB

7.15.4.25 SHA-1 Hash Control Register (SHA1HASHCTRLR)

SHA1HASHCTRLR and SHA1HBADDR are used for SHA-1.

Address Offset: 2Dh

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	W	0b	**SHA-1 Start Control (SHA1SCTRL)** Write 01b to this bit to start SHA-1.

7.15.4.26 SHA-1 Hash Base Address Register (SHA1HBADDR)

Address Offset: 2Eh

Bit	R/W	Default	Description
7-0	W	00h	**Hash Base Address 1 Register (HASHBADDR1R)** HASHBADDR1R = (HASHBADDR1 >> 6) & FFEh

7.15.4.27 Memory Controller Configuration Register (MCCR)

Address Offset: 30h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-5	R/W	10b	**EC Memory Snoop Extended Cycle** 00: No cycle extend 01: 1T EC cycle extend 10: 2T EC cycle extend 11: 3T EC cycle extend
4	-	-	**Reserved**
3	R/W	0b	**DLM 12k~16k Size Select** 0: Disable 1: Enable
2	R/W	0b	**DLM 8k~12k Size Select** 0: Disable 1: Enable
1-0	-	-	Reserved

7.15.4.28 External ILM/DLM Size Register (EIDSR)

Address Offset: 31h

Bit	R/W	Default	Description
7-4	R/W	10b	**External Data Local Memory Size** 0: 4k byte 1: 8k byte 2: 16k byte 3: 32k byte 4: 64k byte 5: 128k byte 6: 256k byte 7: 512k byte 8: 1M byte 9: 1k byte 10: 2k byte 11-14: Reserved 15: 0 Byte (Used for unconnected external ILM)
3-0	R/W	101b	**External Instruction Local Memory Size** 0: 4k byte 1: 8k byte 2: 16k byte 3: 32k byte 4: 64k byte 5: 128k byte 6: 256k byte 7: 512k byte 8: 1M byte 9: 1k byte 10: 2k byte 11-14: Reserved 15: 0 Byte (Used for unconnected external ILM)

7.15.4.29 Pin Multi-function Enable Register 1 (PMER1)

Address Offset: 32h

Bit	R/W	Default	Description
7	R/W	0b	**Sensor Fusion Interrupt 5 Pin Multi-function Enable (SMINT5EN)** 0: Disable 1: Enable
6	R/W	0b	**Sensor Fusion Interrupt 4 Pin Multi-function Enable (SMINT4EN)** 0: Disable 1: Enable
5	R/W	0b	**Sensor Fusion Interrupt 3 Pin Multi-function Enable (SMINT3EN)** 0: Disable 1: Enable
4	R/W	0b	**Sensor Fusion Interrupt 2 Pin Multi-function Enable (SMINT2EN)** 0: Disable 1: Enable
3	R/W	0b	**Sensor Fusion Interrupt 1 Pin Multi-function Enable (SMINT1EN)** 0: Disable 1: Enable
2	R/W	0b	**Sensor Fusion Interrupt 0 Pin Multi-function Enable (SMINT0EN)** 0: Disable 1: Enable
1	R/W	0b	**SMB Group 5 Pin Multi-function Enable** 0: Disable 1: Enable
0	R/W	0b	**SMB Group 4 Pin Multi-function Enable** 0: Disable 1: Enable

7.15.4.30 Pin Multi-function Enable Register 2 (PMER2)

Address Offset: 33h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**Jtag Hardware Strap Pin Multi-function Disable** 0: Disable 1: Enable
5	R/W	0b	**Sensor Fusion Interrupt 11 Pin Multi-function Enable (SMINT11EN)** 0: Disable 1: Enable
4	R/W	0b	**Sensor Fusion Interrupt 10 Pin Multi-function Enable (SMINT10EN)** 0: Disable 1: Enable
3	R/W	0b	**Sensor Fusion Interrupt 9 Pin Multi-function Enable (SMINT9EN)** 0: Disable 1: Enable
2	R/W	0b	**Sensor Fusion Interrupt 8 Pin Multi-function Enable (SMINT8EN)** 0: Disable 1: Enable
1	R/W	0b	**Sensor Fusion Interrupt 7 Pin Multi-function Enable (SMINT7EN)** 0: Disable 1: Enable

Bit	R/W	Default	Description
0	R/W	0b	**Sensor Fusion Interrupt 6 Pin Multi-function Enable (SMINT6EN)** 0: Disable 1: Enable

7.15.4.31 Pin Multi-function Enable Register 3 (PMER3)

Address Offset: 46h

Bit	R/W	Default	Description
7	R/W	0b	**SPI Slave Controller for eMMC Boot Mode Pin Enable (SPISCEBMPEN)** 0b: Disable 1b: CLK/DATA0/CMD are located on GPM2/GPM6/ GPM3.
6	R/W	0b	**SMBUS Channel 3 Pin Select (SMB3PSEL)** 0b: SMCLK3 is located on GPH1. SMDAT3 is located on GPH2. 1b: SMCLK3 is located on GPF2. SMDAT3 is located on GPF3. Refer to Table 7-8. GPIO Alternate Function on page 254.
5-0	-	-	**Reserved**

7.15.4.32 Fix Region Register 0 (FRR0)

Address Offset: 34h

Bit	R/W	Default	Description
7-0	R/W	0b	Fix region base address bit 7-0

7.15.4.33 Fix Region Register 1 (FRR1)

Address Offset: 35h

Bit	R/W	Default	Description
7-0	R/W	0b	Fix region base address bit 15-8

7.15.4.34 Fix Region Register 2 (FRR2)

Address Offset: 36h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	1000b	Fix region base address bit 19-16

7.15.4.35 Eflash Protect Lock Register (EPLR)

Address Offset: 37h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	Eflash protect lock register which can only be write 1 and only be cleared by power-on reset.

7.15.4.36 Sensor Interrupt Switch Select Register 0 (SISSR0)

Address Offset: 38h

Bit	R/W	Default	Description
7-4	R/W	0b	**Sensor Fusion Interrupt 1 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11
3-0	R/W	0b	**Sensor Fusion Interrupt 0 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11

7.15.4.37 Sensor Interrupt Switch Select Register 1 (SISSR1)

Address Offset: 39h

Bit	R/W	Default	Description
7-4	R/W	0b	**Sensor Fusion Interrupt 3 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11
3-0	R/W	0b	**Sensor Fusion Interrupt 2 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11

7.15.4.38 Sensor Interrupt Switch Select Register 2 (SISSR2)

Address Offset: 3Ah

Bit	R/W	Default	Description
7-4	R/W	0b	**Sensor Fusion Interrupt 5 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11

Bit	R/W	Default	Description
3-0	R/W	0b	**Sensor Fusion Interrupt 4 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11

7.15.4.39 Sensor Interrupt Switch Select Register 3 (SISSR3)

Address Offset: 3Bh

Bit	R/W	Default	Description
7-4	R/W	0b	**Sensor Fusion Interrupt 7 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11
3-0	R/W	0b	**Sensor Fusion Interrupt 6 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11

7.15.4.40 Sensor Interrupt Switch Select Register 4 (SISSR4)

Address Offset: 3Ch

Bit	R/W	Default	Description
7-4	R/W	0b	**Sensor Fusion Interrupt 9 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11
3-0	R/W	0b	**Sensor Fusion Interrupt 8 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11

7.15.4.41 Sensor Interrupt Switch Select Register 5 (SISSR5)

Address Offset: 3Dh

Bit	R/W	Default	Description
7-4	R/W	0b	**Sensor Fusion Interrupt 11 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11
3-0	R/W	0b	**Sensor Fusion Interrupt 10 Switch Select** 0: Switch to interrupt 0 1: Switch to interrupt 1 2: Switch to interrupt 2 3: Switch to interrupt 3 4: Switch to interrupt 4 5: Switch to interrupt 5 6: Switch to interrupt 6 7: Switch to interrupt 7 8: Switch to interrupt 8 9: Switch to interrupt 9 10: Switch to interrupt 10 11: Switch to interrupt 11

7.15.4.42 Memory Controller Configuration Register 1 (MCCR1)

Address Offset: 3Eh

Bit	R/W	Default	Description
7	R/W	0b	**SPI Fast Read Function Enable** 0: Disable 1: Enable
6	R/W	0b	**DLM 32k~36k Size Select** 0: Disable 1: Enable
5	R/W	0b	**DLM 28k~32k Size Select** 0: Disable 1: Enable
4	R/W	0b	**DLM 24k~28k Size Select** 0: Disable 1: Enable
3	R/W	0b	**DLM 20k~24k Size Select** 0: Disable 1: Enable
2	R/W	0b	**DLM 16k~20k Size Select** 0: Disable 1: Enable

Bit	R/W	Default	Description
1	R/W	0b	**Jtag Host Mode Enable** 0: Disable 1: Enable
0	R/W	0b	**SRAM 8k~12k Access By DBGR Enable** 0: Disable 1: Enable

7.15.4.43 DIM Base Address Register 0 (DIMBA0)

Address Offset: 3Fh

Bit	R/W	Default	Description
7-0	-	-	DIM base address bit 7-0

7.15.4.44 DIM Base Address Register 1 (DIMBA1)

Address Offset: 40h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	-	-	DIM base address bit 11-8

7.15.4.45 Interrupt Vector Table Base Address Register (IVTBAR)

Address Offset: 41h

Bit	R/W	Default	Description
7-0	R/W	0b	Interrupt Vector Table Base Address, in 64k Byte unit

7.15.4.46 DLM Size Reduce Control Flag Register 0 (DSRCFR0)

Address Offset: 42h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	Enable bit of DLM SRAM size reduce from 8K to 6K for some package. DLM SARM can only be reduced from 8K to 6K in some package when this bit and DSRCFR1 bit0 both be set to 1.

7.15.4.47 DLM Size Reduce Control Flag Register 1 (DSRCFR1)

Address Offset: 43h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	Enable bit of DLM SRAM size reduce from 8K to 6K for some package. DLM SRAM can only be reduced from 8K to 6K in some package when this bit and DSRCFR0 bit0 both be set to 1

7.15.4.48 Memory Controller Configuration Register 2 (MCCR2)

Address Offset: 44h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**FSPI and SSPI Pins Switch Function** 0: Disable 1: Enable
5	R/W	0b	**DLM 56k~60k Size Select** 0: Disable 1: Enable
4	R/W	0b	**DLM 52k~56k Size Select** 0: Disable 1: Enable
3	R/W	0b	**DLM 48k~52k Size Select** 0: Disable 1: Enable
2	R/W	0b	**DLM 44k~48k Size Select** 0: Disable 1: Enable
1	R/W	0b	**DLM 40k~44k Size Select** 0: Disable 1: Enable
0	R/W	0b	**DLM 36k~40k Size Select** 0: Disable 1: Enable

7.15.4.49 Memory Controller Configuration Register 3 (MCCR3)

Address Offset: 20h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**SPI slave Pin Function Enable** 0: Disable 1: Enable
5	R/W	0b	**MAF eSPI reset Function Enable** 0: Disable 1: Enable
4	R/W	0b	**SSPI Second in Path Select** 0: Disable 1: Enable
3-0	-	-	**Reserved**

7.15.4.50 Dummy Register (DMR)

Address Offset: 45h

Bit	R/W	Default	Description
7-3	R/W	0b	**Reserved**
2	R/W	0b	**PLTRST# Signal Reseted by espi_rst_n Select Register** 1: PLTRST# can be reset by espi_rst_n. 0: PLTRST# can not be reset by espi_rst_n.
1	R/W	0b	**SSPI MOSI value in SSPI Read Direction** 0: MOSI will output 0 in the SSPI read direction. 1: MOSI will output 1 in the SSPI read direction.
0	R/W	0b	**EC to BRAM Access Enable** 0: Disable access path of EC to BRAM. 1: Enable access path of EC to BRAM but DBGR to BRAM will be disabled.

7.15.4.51 ETWD and UART Control Register (ETWDUARTCR)

Address Offset: 4Bh

Bit	R/W	Default	Description
7-2	R/W	0b	**Reserved**
1	R/W	0b	**UART Rx Start Detect Select** 0: Low level detect 1: Falling edge detect
0	R/W	0b	**ETWD Hardware Reset Enable** 0: Disable ETWD H/W reset. 1: Enable ETWD H/W reset.

7.15.4.52 Wakeup MCU Control Register (WMCR)

Address Offset: 4Ch

Bit	R/W	Default	Description
7-1	R/W	0b	**Reserved**
0	R/W	0b	**Wakeup MCU Control Register** 0: No wakeup MCU when MCU is in power save mode 1: Wakeup MCU when MCU is in power save mode

7.15.4.53 Mailbox Message Register (MMR)

Address Offset: 4Dh

Bit	R/W	Default	Description
7-0	R/W	0b	The register is used for message transaction.

7.15.4.54 EC Interrupt Request Register (EIRR)

Address Offset: 4Eh

Bit	R/W	Default	Description
7-1	R/W	0b	**Reserved**
0	R/WC	0b	**EC Interrupt Request Register** 0: No interrupt event 1: Interrupt EC

7.15.4.55 Port 80h/81h Status Register (P80H81HSR)

Address Offset: 50h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/WC	0b	**Port 80h/81h Receive Status (P80H81HRS)** 0b: No cycle is received. 1b: The LPC I/O cycle with address 80h (or 81h) is received. Write 1 to clear this bit.

7.15.4.56 Port 80h Data Register (P80HDR)

Address Offset: 51h

Bit	R/W	Default	Description
7-0	R	-	**Port 80h Data (P80HD)** Read returns the received data of the LPC I/O cycle with address 80h.

7.15.4.57 Port 81h Data Register (P81HDR)

Address Offset: 52h

Bit	R/W	Default	Description
7-0	R	-	**Port 81h Data (P81HD)** Read returns the received data of the LPC I/O cycle with address 81h.

7.15.4.58 H2RAM Offset Register (H2ROFSR)

Address Offset: 53h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0h	These bits are used to add an offset to the host to RAM cycle address.

7.15.4.59 Eflash 1K R/W Protect Control Register0 For Path From EC

Address Offset: 55h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash 1K Read/Write Protect Region Control Register for Path from EC** Bit0: (Flash Size – 1k) ~ (Flash Size) write protect enable Bit1: (Flash Size – 1k) ~ (Flash Size) read protect enable Bit2: (Flash Size – 2k) ~ (Flash Size – 1k) write protect enable Bit3: (Flash Size – 2k) ~ (Flash Size – 1k) read protect enable Bit4: (Flash Size – 3k) ~ (Flash Size – 2k) write protect enable Bit5: (Flash Size – 3k) ~ (Flash Size – 2k) read protect enable Bit6: (Flash Size – 4k) ~ (Flash Size – 3k) write protect enable Bit7: (Flash Size – 4k) ~ (Flash Size – 3k) read protect enable

7.15.4.60 Eflash 1K R/W Protect Control Register1 For Path From EC

Address Offset: 56h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash 1K Read/Write Protect Region Control Register for Path from EC** Bit0: (Flash Size – 5k) ~ (Flash Size – 4k) write protect enable Bit1: (Flash Size – 5k) ~ (Flash Size – 4k) read protect enable Bit2: (Flash Size – 6k) ~ (Flash Size – 5k) write protect enable Bit3: (Flash Size – 6k) ~ (Flash Size – 5k) read protect enable Bit4: (Flash Size – 7k) ~ (Flash Size – 6k) write protect enable Bit5: (Flash Size – 7k) ~ (Flash Size – 6k) read protect enable Bit6: (Flash Size – 8k) ~ (Flash Size – 7k) write protect enable Bit7: (Flash Size – 8k) ~ (Flash Size – 7k) read protect enable

7.15.4.61 Eflash 1K R/W Protect Control Register0 For Path From DBGR

Address Offset: 57h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash 1K Read/Write Protect Region Control Register for Path from DBGR** Bit0: (Flash Size – 1k) ~ (Flash Size) write protect enable Bit1: (Flash Size – 1k) ~ (Flash Size) read protect enable Bit2: (Flash Size – 2k) ~ (Flash Size – 1k) write protect enable Bit3: (Flash Size – 2k) ~ (Flash Size – 1k) read protect enable Bit4: (Flash Size – 3k) ~ (Flash Size – 2k) write protect enable Bit5: (Flash Size – 3k) ~ (Flash Size – 2k) read protect enable Bit6: (Flash Size – 4k) ~ (Flash Size – 3k) write protect enable Bit7: (Flash Size – 4k) ~ (Flash Size – 3k) read protect enable

7.15.4.62 Eflash 1K R/W Protect Control Register1 For Path From DBGR

Address Offset: 58h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash 1K Read/Write Protect Region Control Register for Path from DBGR** Bit0: (Flash Size – 5k) ~ (Flash Size – 4k) write protect enable Bit1: (Flash Size – 5k) ~ (Flash Size – 4k) read protect enable Bit2: (Flash Size – 6k) ~ (Flash Size – 5k) write protect enable Bit3: (Flash Size – 6k) ~ (Flash Size – 5k) read protect enable Bit4: (Flash Size – 7k) ~ (Flash Size – 6k) write protect enable Bit5: (Flash Size – 7k) ~ (Flash Size – 6k) read protect enable Bit6: (Flash Size – 8k) ~ (Flash Size – 7k) write protect enable Bit7: (Flash Size – 8k) ~ (Flash Size – 7k) read protect enable

7.15.4.63 Eflash 1K R/W Protect Control Register0 For Path From Host

Address Offset: 59h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash 1K Read/Write Protect Region Control Register for Path from Host** Bit0: (Flash Size – 1k) ~ (Flash Size) write protect enable Bit1: (Flash Size – 1k) ~ (Flash Size) read protect enable Bit2: (Flash Size – 2k) ~ (Flash Size – 1k) write protect enable Bit3: (Flash Size – 2k) ~ (Flash Size – 1k) read protect enable Bit4: (Flash Size – 3k) ~ (Flash Size – 2k) write protect enable Bit5: (Flash Size – 3k) ~ (Flash Size – 2k) read protect enable Bit6: (Flash Size – 4k) ~ (Flash Size – 3k) write protect enable Bit7: (Flash Size – 4k) ~ (Flash Size – 3k) read protect enable

7.15.4.64 Eflash 1K R/W Protect Control Register1 For Path From Host

Address Offset: 5Ah

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash 1K Read/Write Protect Region Control Register for Path from Host** Bit0: (Flash Size – 5k) ~ (Flash Size – 4k) write protect enable Bit1: (Flash Size – 5k) ~ (Flash Size – 4k) read protect enable Bit2: (Flash Size – 6k) ~ (Flash Size – 5k) write protect enable Bit3: (Flash Size – 6k) ~ (Flash Size – 5k) read protect enable Bit4: (Flash Size – 7k) ~ (Flash Size – 6k) write protect enable Bit5: (Flash Size – 7k) ~ (Flash Size – 6k) read protect enable Bit6: (Flash Size – 8k) ~ (Flash Size – 7k) write protect enable Bit7: (Flash Size – 8k) ~ (Flash Size – 7k) read protect enable

7.15.4.65 Hardware ECC Function Control Register (HWECCFCR)

Address Offset: 5Bh

Bit	R/W	Default	Description
7-1	R/W	0b	**Reserved**
0	R/W	0b	**Hardware ECC Function Enable** 0: Disable 1: Enable

7.15.4.66 Hardware ECC Function Control Register1 (HWECCFCR1)

Address Offset: 5Ch

Bit	R/W	Default	Description
7-1	R/W	0b	**Reserved**
0	R	0b	**Hardware ECC Function Start**

7.15.4.67 RISCV ILM Configuration Register 0 (RVILMCR0)

Address Offset: 5Dh

Bit	R/W	Default	Description
7	R/W	0b	**RISCV ILM7 Enable** 0: Disable 1: Enable
6	R/W	0b	**RISCV ILM6 Enable** 0: Disable 1: Enable
5	R/W	0b	**RISCV ILM5 Enable** 0: Disable 1: Enable
4	R/W	0b	**RISCV ILM4 Enable** 0: Disable 1: Enable
3	R/W	0b	**RISCV ILM3 Enable** 0: Disable 1: Enable
2	R/W	0b	**RISCV ILM2 Enable** 0: Disable 1: Enable
1	R/W	0b	**RISCV ILM1 Enable** 0: Disable 1: Enable
0	R/W	0b	**RISCV ILM0 Enable** 0: Disable 1: Enable

7.15.4.68 RISCV ILM Configuration Register 1 (RVILMCR1)

Address Offset: 5Eh

Bit	R/W	Default	Description
7	R/W	0b	**RISCV ILM15 Enable** 0: Disable 1: Enable
6	R/W	0b	**RISCV ILM14 Enable** 0: Disable 1: Enable
5	R/W	0b	**RISCV ILM13 Enable** 0: Disable 1: Enable
4	R/W	0b	**RISCV ILM12 Enable** 0: Disable 1: Enable
3	R/W	0b	**RISCV ILM11 Enable** 0: Disable 1: Enable
2	R/W	0b	**RISCV ILM10 Enable** 0: Disable 1: Enable

Bit	R/W	Default	Description
1	R/W	0b	**RISCV ILM9 Enable** 0: Disable 1: Enable
0	R/W	0b	**RISCV ILM8 Enable** 0: Disable 1: Enable

7.15.4.69 RISCV ILM Configuration Register 2 (RVILMCR2)

Address Offset: 5Fh

Bit	R/W	Default	Description
7	R/W	0b	**RISCV ILM23 Enable** 0: Disable 1: Enable
6	R/W	0b	**RISCV ILM22 Enable** 0: Disable 1: Enable
5	R/W	0b	**RISCV ILM21 Enable** 0: Disable 1: Enable
4	R/W	0b	**RISCV ILM20 Enable** 0: Disable 1: Enable
3	R/W	0b	**RISCV ILM19 Enable** 0: Disable 1: Enable
2	R/W	0b	**RISCV ILM18 Enable** 0: Disable 1: Enable
1	R/W	0b	**RISCV ILM17 Enable** 0: Disable 1: Enable
0	R/W	0b	**RISCV ILM16 Enable** 0: Disable 1: Enable

7.15.4.70 Eflash Write Protect Register 0 For Path From Host (EWPR0PFH)

Address Offset: 60h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 0k~2k Bit1: 2k~4k Bit2: 4k~6k Bit3: 6k~8k Bit4: 8k~10k Bit5: 10k~12k Bit6: 12k~14k Bit7: 14k~16k

7.15.4.71 Eflash Write Protect Register 1 For Path From Host (EWPR1PFH)

Address Offset: 61h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 16k~18k Bit1: 18k~20k Bit2: 20k~22k Bit3: 22k~24k Bit4: 24k~26k Bit5: 26k~28k Bit6: 28k~30k Bit7: 30k~32k

7.15.4.72 Eflash Write Protect Register 2 For Path From Host (EWPR2PFH)

Address Offset: 62h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 32k~34k Bit1: 34k~36k Bit2: 36k~38k Bit3: 38k~40k Bit4: 40k~42k Bit5: 42k~44k Bit6: 44k~46k Bit7: 46k~48k

7.15.4.73 Eflash Write Protect Register 3 For Path From Host (EWPR3PFH)

Address Offset: 63h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 48k~50k Bit1: 50k~52k Bit2: 52k~54k Bit3: 54k~56k Bit4: 56k~58k Bit5: 58k~60k Bit6: 60k~62k Bit7: 62k~64k

7.15.4.74 Eflash Write Protect Register 4 For Path From Host (EWPR4PFH)

Address Offset: 64h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 64k~66k Bit1: 66k~68k Bit2: 68k~70k Bit3: 70k~72k Bit4: 72k~74k Bit5: 74k~76k Bit6: 76k~78k Bit7: 78k~80k

7.15.4.75 Eflash Write Protect Register 5 For Path From Host (EWPR5PFH)

Address Offset: 65h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 80k~82k Bit1: 82k~84k Bit2: 84k~86k Bit3: 86k~88k Bit4: 88k~90k Bit5: 90k~92k Bit6: 92k~94k Bit7: 94k~96k

7.15.4.76 Eflash Write Protect Register 6 For Path From Host (EWPR6PFH)

Address Offset: 66h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 96k~98k Bit1: 98k~100k Bit2: 100k~102k Bit3: 102k~104k Bit4: 104k~106k Bit5: 106k~108k Bit6: 108k~110k Bit7: 110k~112k

7.15.4.77 Eflash Write Protect Register 7 For Path From Host (EWPR7PFH)

Address Offset: 67h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 112k~114k Bit1: 114k~116k Bit2: 116k~118k Bit3: 118k~120k Bit4: 120k~122k Bit5: 122k~124k Bit6: 124k~126k Bit7: 126k~128k

7.15.4.78 Eflash Write Protect Register 8 For Path From Host (EWPR8PFH)

Address Offset: 68h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 128k~130k Bit1: 130k~132k Bit2: 132k~134k Bit3: 134k~136k Bit4: 136k~138k Bit5: 138k~140k Bit6: 140k~142k Bit7: 142k~144k

7.15.4.79 Eflash Write Protect Register 9 For Path From Host (EWPR9PFH)

Address Offset: 69h

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 144k~146k Bit1: 146k~148k Bit2: 148k~150k Bit3: 150k~152k Bit4: 152k~154k Bit5: 154k~156k Bit6: 156k~158k Bit7: 158k~160k

7.15.4.80 Eflash Write Protect Register 10 For Path From Host (EWPR10PFH)

Address Offset: 6Ah

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 160k~162k Bit1: 162k~164k Bit2: 164k~166k Bit3: 166k~168k Bit4: 168k~170k Bit5: 170k~172k Bit6: 172k~174k Bit7: 174k~176k

7.15.4.81 Eflash Write Protect Register 11 For Path From Host (EWPR12PFH)

Address Offset: 6Bh

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 176k~178k Bit1: 178k~180k Bit2: 180k~182k Bit3: 182k~184k Bit4: 184k~186k Bit5: 186k~188k Bit6: 188k~190k Bit7: 190k~192k

7.15.4.82 Eflash Write Protect Register 12 For Path From Host (EWPR12PFH)

Address Offset: 6Ch

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 192k~194k Bit1: 194k~196k Bit2: 196k~198k Bit3: 198k~200k Bit4: 200k~202k Bit5: 202k~204k Bit6: 204k~206k Bit7: 206k~208k

7.15.4.83 Eflash Write Protect Register 13 For Path From Host (EWPR13PFH)

Address Offset: 6Dh

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 208k~210k Bit1: 210k~212k Bit2: 212k~214k Bit3: 214k~216k Bit4: 216k~218k Bit5: 218k~220k Bit6: 220k~222k Bit7: 222k~224k

7.15.4.84 Eflash Write Protect Register 14 For Path From Host (EWPR14PFH)

Address Offset: 6Eh

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 224k~226k Bit1: 226k~228k Bit2: 228k~230k Bit3: 230k~232k Bit4: 232k~234k Bit5: 234k~236k Bit6: 236k~238k Bit7: 238k~240k

7.15.4.85 Eflash Write Protect Register 15 For Path From Host (EWPR15PFH)

Address Offset: 6Fh

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from Host** Bit0: 240k~242k Bit1: 242k~244k Bit2: 244k~246k Bit3: 246k~248k Bit4: 248k~250k Bit5: 250k~252k Bit6: 252k~254k Bit7: 254k~256k

7.15.4.86 Eflash Read Protect Register 0~15 For Path From Host (ERPR0PFH~ERPR15PFH)

Address Offset: 70h~7Fh

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Read Protect Region Control Register for Path from Host** The same eflash protet region mapped as EWPR0PFH~EWPR15PFH. These registers are read protect when the size is less than or equal to 256k but will become write protect when it is larger than 256k.

7.15.4.87 Eflash Write Protect Register 0~15 For Path From DBGR (EWPR0PFD~EWPR15PFD)

Address Offset: A0h~AFh

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from DBGR** The same eflash protet region mapped as EWPR0PFH~EWPR15PFH

7.15.4.88 Eflash Read Protect Register 0~15 For Path From DBGR (ERPR0PFD~ERPR15PFD)

Address Offset: B0h~BFh

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Read Protect Region Control Register for Path from DBGR** The same eflash protet region mapped as EWPR0PFH~EWPR15PFH. These registers are read protect when the size is less than or equal to 256k but will become write protect when it is larger than 256k.

7.15.4.89 Eflash Write Protect Register 0~15 For Path From EC (EWPR0PFEC~EWPR15PFEC)

Address Offset: C0h~CFh

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Write Protect Region Control Register for Path from EC** The same eflash protet region mapped as EWPR0PFH~EWPR15PFH

7.15.4.90 Eflash Read Protect Register 0~15 For Path From EC (ERPR0PFEC~ERPR15PFEC)

Address Offset: D0h~DFh

Bit	R/W	Default	Description
7-0	R/W	0b	**Eflash Read Protect Region Control Register for Path from EC** The same eflash protet region mapped as EWPR0PFH~EWPR15PFH. These registers are read protect when the size is less than or equal to 256k but will become write protect when it is larger than 256k.

7.16 Battery-backed SRAM (BRAM)

7.16.1 Overview

This module provides 192 bytes of battery-backed memory area.

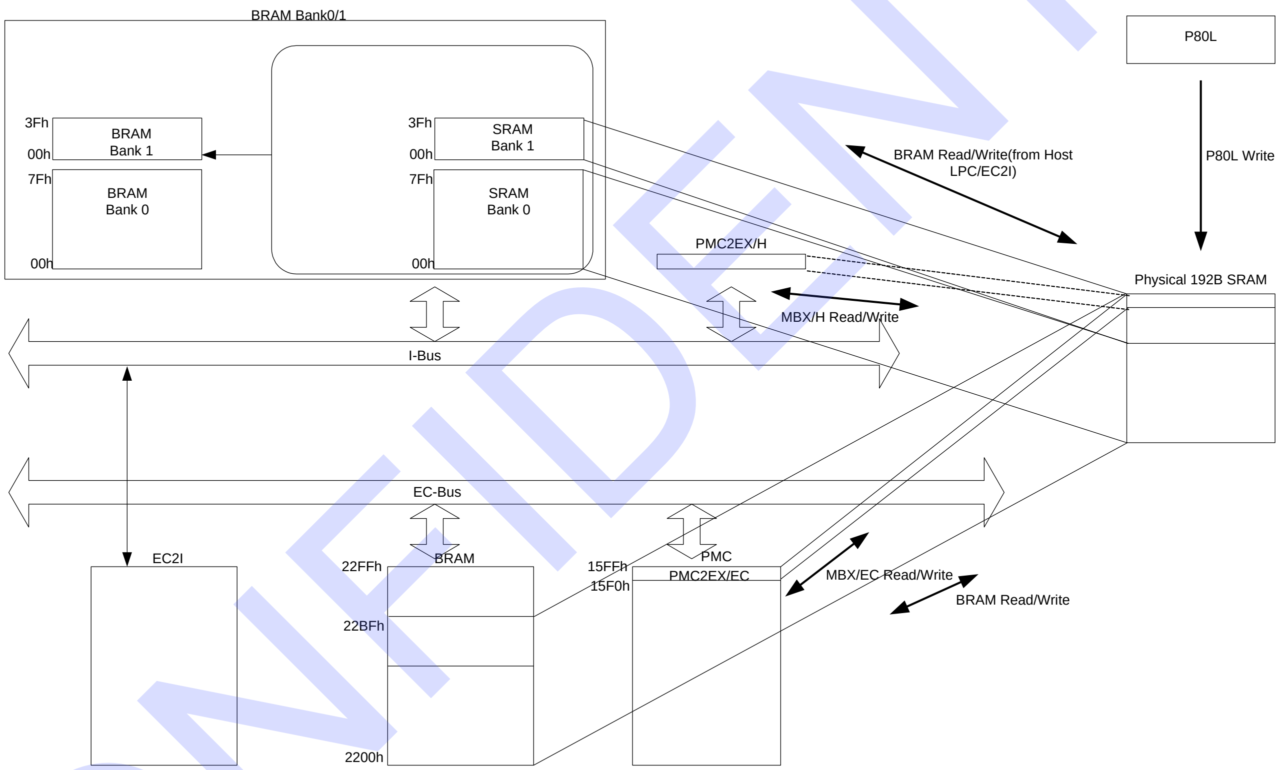
7.16.2 Features

- 192 bytes of battery-backed SRAM mapped into the host and EC side

7.16.3 Functional Description

This module provides 192 bytes of battery-backed SRAM for data-saving function shared with the host side.

Figure 7-23. BRAM Mapping Diagram



7.16.4 P80L

If this function is enabled by P80LEN bit in SPCTRL1 register, LPC I/O port 80h written data will be latched into SRAM of BRAM bank 1.

The data may fail to latch data if there is a transaction cycle to BRAM at the same time unless ACP80 bit in SPCTRL1 register is set, which guarantees written data is latched into SRAM by issuing Long Wait Sync on host LPC bus.

The destination address range in BRAM Bank 1 is determined by P80LB, P80LE register in the host side, which constructs a queue.
P80LB: It indicates the start index of the queue. Readable/Writable.
P80LE: It indicates the end index of the queue. Readable/Writable.
P80LC: It indicates the current index of the queue. Read-only.

These three registers are supplied by VSTBY power and not affected by VCC status.

Whenever written data is latched, P80LC increases one. If it reaches P80LE (queue end), it will wrap back to P80LB (queue begin).

7.16.5 Host Interface Registers

The registers of BRAM can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.

The BRAM resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below. In addition to the I/O Port Base Addresses of channel, there are three I/O Port Base Addresses of channel for accessing BRAM of Bank1.

Table 7-27. Host View Register Map, BRAM

7 0	Offset
BRAM Index Register of Bank 0 (RIRB0)	Legacy 70h
BRAM Data Register of Bank 0 (RDRB0)	Legacy 71h
BRAM Index Register of Bank 1 (RIRB1)	Legacy 272h
BRAM Data Register of Bank 1 (RDRB1)	Legacy 273h

Legacy 70h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 71h represents (I/O Port Base Address 0) + (Offset 1h)
Legacy 272h represents (I/O Port Base Address 1) + (Offset 0h)
Legacy 273h represents (I/O Port Base Address 1) + (Offset 1h)
See also Table 6-7 on page 73.

Table 7-28. Host View Register Map via Index-Data I/O Pair, BRAM Bank 0

7 0	Offset
SRAM Byte n Registers (SBT0)	00h
…	…
SRAM Byte n Registers (SBT127)	7Fh

Table 7-29. Host View Register Map via Index-Data I/O Pair, BRAM Bank 1

7 0	Offset
SRAM Byte n Registers (SBT0)	00h
…	…
SRAM Byte n Registers (SBT63)	3Fh

7.16.6 EC Interface Registers

The registers of the battery-backed SRAM are listed below. The base address is 2200h.

Table 7-30. EC View Register Map, BRAM

7 0	Offset
SRAM Byte n Registers (SBT0)	00h
…	…
SRAM Byte n Registers (SBT191)	BFh

7.16.6.1 SRAM Byte n Registers (SBTn, n= 0-191)

Address Offset: 80h – BFh for byte 0 – byte 191

Bit	R/W	Default	Description
7-0	R/W	-	**SRAM Data (SD)** When data is written to this register, it will be saved in the corresponding memory space. When this register is read, the contents of the corresponding memory space can be read.

7.17 Serial Peripheral Interface (SSPI)

7.17.1 Overview

The SPI device uses 3-wire bi-directional or 4-wire interface for data transmission. The 4-wire device consists four signals, SSCE#, SSCK, SMOSI, and SMISO, for data transmission, and the 3-wire device consists three signals, SSCE#, SSCK, SMISO, for data transmission. The SPI interface consists of two identical channels and they can be connected to either the 3-wire or 4-wire device.

7.17.2 Features

- Supports both Host and EC side
- Supports eight frequency dividers of SSCK (2, 4, 6, 8, 10, 12, 14, 16)
- Supports n-bit transmission (n = 1 ~ 8)
- Supports blocking and non-blocking selection
- Supports Interrupt enable and Interrupt disable in the non-blocking selection.
- Supports 3-wire SPI device and 4-wire SPI device
- Supports four clock modes
- Supports DMA mode and DMA ring buffer
- Supports Command Queue mode

7.17.3 Functional Description

All instructions, addresses, and data are shifted in and out of the device, starting with the most significant bit. The interface supplies the synchronous clock (SSCK) for the serial interface and initiates the data transfer.

The device responds by sending (or receiving) the requested data. The device uses the interface clock to serially shift data out (or in) while the interface shifts the data in (or out).

7.17.3.1 Data Transmissions

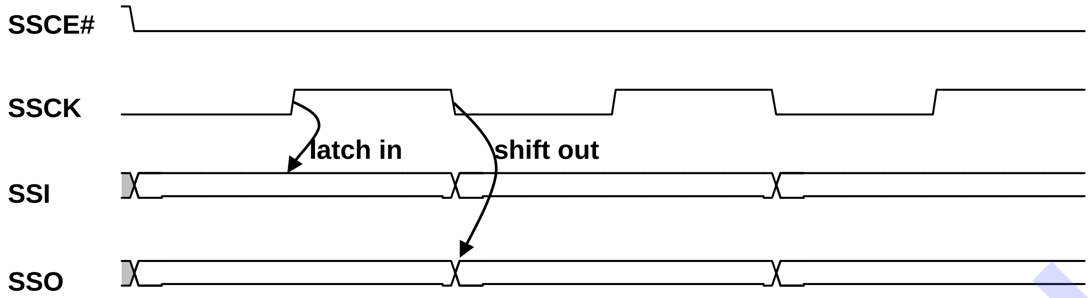
8-bit Transmission
The interface supports 8-cycle SSCK for data transmission. It is available for 1-byte transaction devices. (default)

N-bit Transmission (N = 1 ~ 7)
The interface supports N-cycle SSCK for data transmission. It is available for non-1-byte transaction devices.

7.17.3.2 SPI Mode

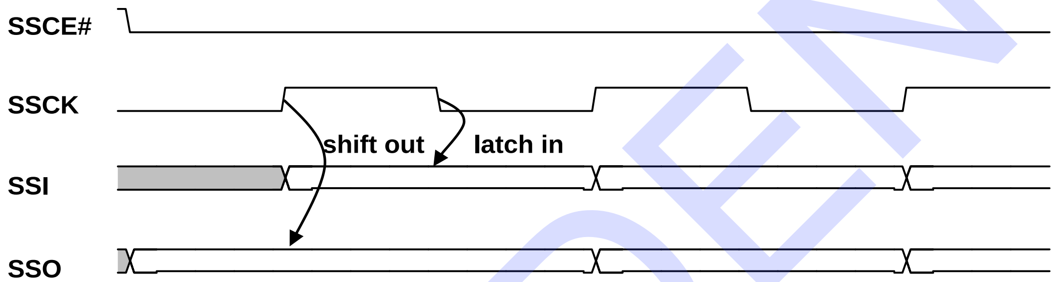
Mode 0
SSCK is low in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge.

Figure 7-24. SPI Mode 0 Waveform



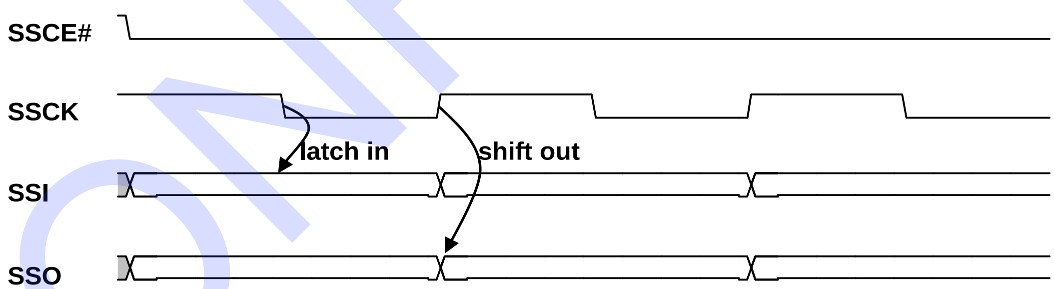
Mode 1
SSCK is low in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge.

Figure 7-25. SPI Mode 1 Waveform



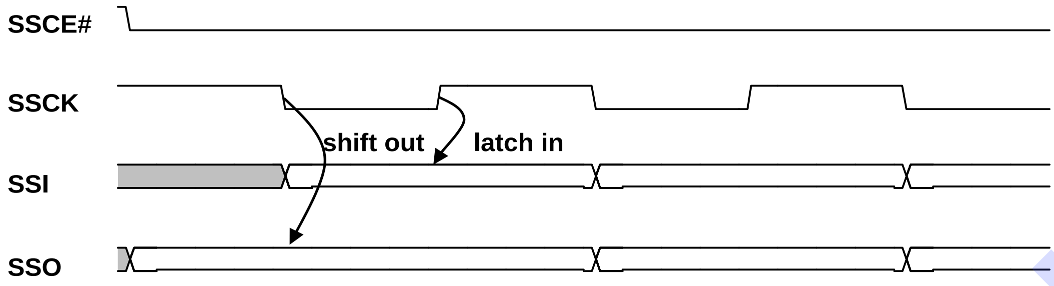
Mode 2
SSCK is high in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge.

Figure 7-26. SPI Mode 2 Waveform



Mode 3
SSCK is high in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge.

Figure 7-27. SPI Mode 3 Waveform



7.17.3.3 Blocking and Non-blocking mode

- Blocking mode:

  After starting the read cycle or write cycle to the SPI module (writing 1 to CH0START or CH1START bit in SPISTS register), the bus will be blocked until this read/write command is finished.

  If the SPI function is controlled by the EC side, EC CPU instruction will be halted until this read/write command is finished.

  If the SPI function is controlled by the host side, the LPC bus will return the long-wait sync pattern until this read/write command is finished.

  It means that the interrupt and the polling are not needed.

- Non-blocking mode

  After starting the read cycle or write cycle to the SSPI module (writing 1 to CH0START or CH1START bit in SPISTS register), the processor receives an interrupt signal or polls bit 2 of SPISTS register to determine if this read/write command will be terminated .

7.17.3.4 Command Queue mode

7.17.3.4.1 Command Definition

The following is the command format for command queue:
Wr_cmd_length: It contains the bytes of SSPI instruction and address for SSPI.
Cmd_end: It indicates this is the last one command in the command lists.
R/W: 1: SSPI read direction; 0: SSPI write direction.
Data_length: The total write data length for SSPI write direction; the total read data length for SSPI read direction.
Auto check status: Enable CMDQ to auto check read status, which must cooperate with check bit mask and check bit value.
SSPI_CS active: It is used to control whether the SSPI chip select signal will keep active or not when CMD is finished.
1: Keep active; 0: Keep inactive.
Dual Mode: When this bit is set to 1, SSPI Bus will be in Dual mode format.
DTR Mode: When this bit is set to 1, SSPI Bus will be in DTR mode format.
Data_address: Allocate the target address of purely transmitted data for SSPI write direction.
Check bit mask: Mask the check bit for read status compared.
Check bit value: The compare value for read status.

Command	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
SPI Write CMD Length	Wr_cmd_length[7:0]							
CMD 1	DTR Mode	Dual Mode	-	-	SSPI_CS Active	Auto Check Status	R/W	Cmd_end
Data Length 1	Data_length[7:0]							
Data Length 2	Data_length[15:8] (Total 60KB SRAM)							
Data Address 1	Data_addr[7:0]							
Data Address 2	Data_addr[15:8]							
Check bit Mask	Check_bit_mask[7:0]							
Check Bit Value	Check_bit_value[7:0]							

7.17.3.4.2 Using Guide

1. Prepare for the CMDQ + SPI instruction (instr + address) to the address of CH0CMDADDR/ CH1CMDADDR (0x05 and 0x06 or 0x12 and 0x13).
2. Prepare to purely write data to the address of correlated data address (Data_addr[15:0]).
 Start the CMDQ.

7.17.4 Host Interface Registers

The registers of SSPI can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.

The SSPI resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below:

Table 7-31. Host View Register Map, SSPI

7 ... 0	Offset
SPI Data Register (SPIDATA)	00h
SPI Control Register 1 (SPICTRL1)	01h
SPI Control Register 2 (SPICTRL2)	02h
SPI Control Register 3 (SPICTRL3)	04h
SPI Start and End Status Register (SPISTS)	03h
Channel 0 Command Address Low Byte Register (CH0CMDADDRLB)	05h
Channel 0 Command Address High Byte Register (CH0CMDADDRHB)	06h
DMA Transfer Count Low Byte Register (DMATCNTLB)	07h
DMA Transfer Count High Byte Register (DMATCNTHB)	08h
SPI Write Command Length Register (SPIWRCMDL)	09h
Channel 0 DMA Ring Depth Low Byte Register (CH0DMARDLB)	0Ah
Channel 0 DMA Ring Depth High Byte Register (CH0DMARDHB)	0Bh
Interrupt Status Register (INTSTS)	0Ch
SPI Control Register 5 (SPICTRL5)	0Dh
Channel 0 Write Memory Address Low Byte Register (CH0WRMEMADDRLB)	0Eh

7 ... 0	Offset
Channel 0 Write Memory Address High Byte Register (CH0WRMEMADDRHB)	0Fh
CMDQ Interval Time Prescale Register (CMDQINVPR)	10h
Channel 0 Wait Time Scale Register for CMDQ(CH0WTSR)	11h
Channel 1 Command Address Low Byte Register (CH1CMDADDRLB)	12h
Channel 1 Command Address High Byte Register (CH1CMDADDRHB)	13h
Channel 1 Write Memory Address Low Byte Register (CH1WRMEMADDRLB)	14h
Channel 1 Write Memory Address High Byte Register (CH1WRMEMADDRHB)	15h
Channel 1 Wait Time Scale Register for CMDQ(CH1WTSR)	16h
Channel 1 DMA Ring Depth Low Byte Register (CH1DMARDLB)	17h
Channel 1 DMA Ring Depth High Byte Register (CH1DMARDHB)	18h
Channel 0 Command Address High Byte 2 Register (CH0CMDADDRHB2)	21h
Channel 0 Write Memory Address High Byte 2 Register (CH0WRMEMADDRHB2)	23h
Channel 1 Command Address High Byte 2 Register (CH1CMDADDRHB2)	25h
Channel 1 Write Memory Address High Byte 2 Register (CH1WRMEMADDRHB2)	27h
Delay Select for SSPI Feedback Clock Register (DSFBCR)	2Dh
SPI Receive Data for Dual/DTR Mode Register (SPIRDATA)	2Eh
SPI Control Register 6 (SPICTRL6)	33h

All registers are double mapped into the host and EC side; however, the SSPI function should be controlled by a side only.

7.17.5 EC Interface Registers

The register map of EC interface is listed below. The base address for SSPI0 is 2600h.

Table 7-32. EC View Register Map, SSPI

7 ... 0	Offset
SPI Data Register (SPIDATA)	00h, 40h
SPI Control Register 1 (SPICTRL1)	01h, 41h
SPI Control Register 2 (SPICTRL2)	02h, 42h
SPI Control Register 3 (SPICTRL3)	04h, 44h
SPI Start and End Status Register (SPISTS)	03h, 43h
Channel 0 Command Address Low Byte Register (CH0CMDADDRLB)	05h, 45h
Channel 0 Command Address High Byte Register (CH0CMDADDRHB)	06h, 46h
DMA Transfer Count Low Byte Register (DMATCNTLB)	07h, 47h
DMA Transfer Count High Byte Register (DMATCNTHB)	08h, 48h
SPI Write Command Length Register (SPIWRCMDL)	09h, 49h
Channel 0 DMA Ring Depth Low Byte Register (CH0DMARDLB)	0Ah, 4Ah
Channel 0 DMA Ring Depth High Byte Register (CH0DMARDHB)	0Bh, 4Bh
Interrupt Status Register (INTSTS)	0Ch, 4Ch
SPI Control Register 5 (SPICTRL5)	0Dh, 4Dh
Channel 0 Write Memory Address Low Byte Register (CH0WRMEMADDRLB)	0Eh, 4Eh
Channel 0 Write Memory Address High Byte Register (CH0WRMEMADDRHB)	0Fh, 4Fh
CMDQ Interval Time Prescale Register (CMDQINVPR)	10h, 50h
Channel 0 Wait Time Scale Register for CMDQ(CH0WTSR)	11h, 51h
Channel 1 Command Address Low Byte Register (CH1CMDADDRLB)	12h, 52h
Channel 1 Command Address High Byte Register (CH1CMDADDRHB)	13h, 53h
Channel 1 Write Memory Address Low Byte Register (CH1WRMEMADDRLB)	14h, 54h
Channel 1 Write Memory Address High Byte Register (CH1WRMEMADDRHB)	15h, 55h
Channel 1 Wait Time Scale Register for CMDQ(CH1WTSR)	16h, 56h
Channel 1 DMA Ring Depth Low Byte Register (CH1DMARDLB)	17h, 57h
Channel 1 DMA Ring Depth High Byte Register (CH1DMARDHB)	18h, 58h
Channel 0 Command Address High Byte 2 Register (CH0CMDADDRHB2)	21h, 62h

7 0	Offset
Channel 0 Write Memory Address High Byte 2 Register (CH0WRMEMADDRHB2)	23h, 63h
Channel 1 Command Address High Byte 2 Register (CH1CMDADDRHB2)	25h, 65h
Channel 1 Write Memory Address High Byte 2 Register (CH1WRMEMADDRHB2)	27h, 67h
Delay Select for SSPI Feedback Clock Register (DSFBCR)	2Dh, 6Dh
SPI Receive Data for Dual/DTR Mode Register (SPIRDATA)	2Eh, 6Eh
SPI Control Register 6 (SPICTRL6)	33h, 73h

Other related register(s):

- General Control 1 Register (GCR1), SPICTRL bit
- General Control 3 Register (GCR3), SSPIPDG bit

7.17.5.1 SPI Data Register (SPIDATA)

The register holds the shift data from the SPI device in the read mode and the data can be shifted out to the SPI device through the interface while in the write mode,

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**SPI Data (DATA)** This register is to receive data from the SPI device or transmit data to the SPI device.

7.17.5.2 SPI Control Register 1 (SPICTRL1)

This register controls the SPI's operation mode.

Address Offset: Host: 01h (Bank 0) / EC: 01h

Bit	R/W	Default	Description
7	R/W	0b	**Chip Select Polarity (CHPOL)** If CSPOLSEL is set to 1, the bit indicates the chip select polarity of device 0. Otherwise, it indicates both the chip select polarity of device 0 and device 1 0: Active low 1: Active high
6-5	R/W	00b	**Bit 6: Clock Polarity (CLPOL)** 0: SSCK is low in the idle mode. 1: SSCK is high in the idle mode. **Bit 5: Clock Phase (CLPHS)** 0: Latch data on the first SSCK edge. 1: Latch data on the second SSCK edge. **Mode 0:** SSCK is low in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge. **Mode 1:** SSCK is low in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge. **Mode 2:** SSCK is high in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge. **Mode 3:** SSCK is high in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge.

Bit	R/W	Default	Description
4-2	R/W	000b	**SSCK Frequency (SCKFREQ)** **000b:** 1/2 clk_sspi **001b:** 1/4 clk_sspi **010b:** 1/6 clk_sspi **011b:** 1/8 clk_sspi **100b:** 1/10 clk_sspi **101b:** 1/12 clk_sspi **110b:** 1/14 clk_sspi **111b:** 1/16 clk_sspi (FreqEC is listed in Table 10-2 on page 570)
1	R/W	0b	**Interrupt Enable (INTREN)** 0: Disable 1: Enable
0	R/W	0b	**Device0 3-Wire Mode (3WIRECH0)** 0: Disable (4-wire) 1: Enable (3-wire)

7.17.5.3 SPI Control Register 2 (SPICTRL2)

This register controls the SPI's operation mode.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/W	0b	**Host Side Bank (HBANK)** The bit is only available in host side. 0: Bank 0 1: bank 1
6	-	-	**Reserved**
5-3	R/W	000b	**Byte Width (BYTEWIDTH)** 000b: 8-bit transmission 001b: 1-bit transmission 010b: 2-bit transmission 011b: 3-bit transmission 100b: 4-bit transmission 101b: 5-bit transmission 110b: 6-bit transmission 111b: 7-bit transmission
2	R/W	0b	**Channel Read/Write Cycle (CHRW)** 0: Write cycle 1: Read cycle
1	R/W	0b	**Block Select (BLKSEL)** 0: Non-blocking selection 1: Blocking selection
0	R/W	0b	**Device1 3-Wire Mode (3WIRECH1)** 0: Disable (4-wire) 1: Enable (3-wire)

7.17.5.4 SPI Start and End Status Register (SPISTS)

This register reports the status of the SPI and controls the start and end signal.

Address Offset: 03h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/WC	0b	**SPI Transmission End (TRANEND)** Write 1 to end the SPI transmission. Read 0b.
4	R/WC	0b	**Channel 0 Start Signal (CH0START)** Write 1 to start the data transmission of device 0. Read 0b.
3	R/WC	0b	**Channel 1 Start Signal (CH1START)** Write 1 to start the data transmission of device 1. Read 0b.
2	R	0b	**Transfer In Progress (TRANIP)** This bit indicates the SPI is in the transmission state. 0: Data transfer is not in progress. 1: Data transfer is in progress.
1	R/WC	0b	**Transfer End Flag (TRANENDIF)** This bit indicates SPI transmission ends. The bit will be 1 when 1 is written to the TRANEND bit. Write 1 to clear this bit and terminate data transmission.
0	-	-	**Reserved**

7.17.5.5 SPI Control Register 3 (SPICTRL3)

This register controls the SPI’s operation mode.

Address Offset: Host: 01h (Bank 1) / EC: 04h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	-	**Auto Mode (AUTOMODE)** 0: One-shot mode. 1: Auto mode enabled
4-3	-	-	**Reserved**
2	R/W	0b	**Chip Select Polarity Select (CSPOLSEL)** 0: The chip select polarity of device 1 and device 0 is the same. 1: The chip select polarity of device 1 and device 0 is different.
1	R/W	0b	**Chip Select Polarity 1 (CHPOL1)** If CSPOLSEL is set to 1, the bit indicates the chip select polarity of device 1. 0: Active low 1: Active high
0	-	-	**Reserved**

7.17.5.6 Channel 0 Command Address Low Byte Register (CH0CMDADDRLB)

This register controls the low byte command address of channel 0.

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/W	0h	**CH0 CMD Address Low Byte (CH0CMDADDRLB)** The 8-bit value decides the low byte of CH0 CMD address.

7.17.5.7 Channel 0 Command Address High Byte Register (CH0CMDADDRHB)

This register controls the high byte command address of channel 0.

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	0h	**CH0 CMD Address High Byte (CH0CMDADDRLB)** The 8-bit value decides the high byte of CH0 CMD address.

7.17.5.8 DMA Transfer Count Low Byte Register (DMATCNTLB)

This register indicates the currentDMA low byte transfer count.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R	0h	**DMA Transfer Count Low Byte (DMATCNTLB)** The value indicates the low byte of the current DMA transfer count.

7.17.5.9 DMA Transfer Count High Byte Register (DMATCNTHB)

This register indicates the DMA high byte transfer count currently.

Address Offset: 08h

Bit	R/W	Default	Description
7-4	R	-	**Reserved**
3-0	R	0h	**DMA Transfer Count High Byte (DMATCNTHB)** The value indicates the high byte of the current DMA transfer count.

7.17.5.10 SPI Write Command Length Register (SPIWRCMDL)

This register indicates the length of the current SPI write command and address for SPI read direction in command queue mode.

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R	0h	**SPI Write Command/Address Length (SPIWRCMDL)** The value indicates the length of SPI write command and address for SPI read direction.

7.17.5.11 Channel 0 DMA Ring Depth Low Byte Register (CH0DMARDLB)

This register controls the low byte ring buffer depth of DMA for channel 0.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	0h	**Channel 0 DMA Ring Depth Low Byte (CH0DMARDLB)** The value decides the low byte of DMA ring buffer depth for channel 0.

7.17.5.12 Channel 0 DMA Ring Depth High Byte Register (CH0DMARDHB)

This register controls the high byte ring buffer depth of DMA for channel 0.

Address Offset: 0Bh

Bit	R/W	Default	Description
7-5	R	-	**Reserved**
4-0	R/W	0h	**Channel 0 DMA Ring Depth High Byte (CH0DMARDHB)** The value decides the high byte of DMA ring buffer depth for channel 0.

7.17.5.13 Interrupt Status Register (INTSTS)

This register indicates the interrupt status of SSPI.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R	-	**Reserved**
6-5	R	0h	**SPI Current Channel Select** 01b: Channel 0 selected 10b: Channel 1 selected
4	R/W	1b	**SPI CMDQ Bus End Interrupt Mask (SPICMDQENDMASK)** 0: Mask disabled In this condition, the user must clear the SPICMDQEND bit to continue the next command queue flow in the auto mode. 1: Mask enabled In this setting, the command queue flow will automatically continue in the auto mode.
3	R	-	**Reserved**
2	R/WC	0b	**SPI Ring Buffer 1 Full Interrupt (SPIRING1FI)** When this bit is 1, it indicates DMA ring buffer 1 is full. Write 1 to clear this bit.
1	R/WC	0b	**SPI Ring Buffer 0 Full Interrupt (SPIRING0FI)** When this bit is 1, it indicates DMA ring buffer 0 is full. Write 1 to clear this bit.
0	R/WC	0b	**SPI CMDQ Bus End (SPICMDQEND)** When this bit is 1, it indicates SPI CMDQ transmission ends. Write 1 to clear this bit. When the SPICMDQENDMASK bit is 1, this bit will be auto-cleared in the auto mode to continue the next CMDQ flow. When SPICMDQENDMASK bit is 0, it must be cleared by writing one in the auto mode to continue the next CMDQ flow.

7.17.5.14 SPI Control Register 5 (SPICTRL5)

This register controls the SPI's operation mode.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-6	R	-	**Reserved**
5	R/W	0b	**Channel 1 Select in the CMDQ mode (CH1SELCMDQ)** 0: Channel 1 is disabled in the CMDQ mode. 1: Channel 1 is selected in the CMDQ mode.
4	R/W	0b	**Channel 0 Select in the CMDQ mode (CH0SELCMDQ)** 0: Channel 0 is disabled in the CMDQ mode. 1: Channel 0 is selected in the CMDQ mode.
3	-	-	**Reserved**
2	R/W	0b	**SSPI MOSI Value in SSPI Read Direction** 0: MOSI will output 0 in the SSPI read direction. 1: MOSI will output 1 in the SSPI read direction.
1	R/W	0b	**SSCK Frequency Div 1 Enable (SCKFREQDIV1)** 1: 1 clk_sspi 0: Refe to SCKFREQ setting.
0	R/W	0b	**Command Queue Mode (CMDQMODE)** 0: The CMDQ mode is disabled. 1: The CMDQ mode enabled.

7.17.5.15 Channel 0 Write Memory Address Low Byte Register (CH0WRMEMADDRLB)

This register controls the low byte write memory address of channel 0.

Address Offset: 0Eh

Bit	R/W	Default	Description
7-0	R/W	0h	**CH0 Write Memory Address Low Byte (CH0WRMEMADDRLB)** The 8-bit value decidess the low byte of CH0 write memory address.

7.17.5.16 Channel 0 Write Memory Address High Byte Register (CH0WRMEMADDRHB)

This register controls the high byte write memory address of channel 0.

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	R/W	0h	**CH0 Write Memory Address High Byte (CH0WRMEMADDRHB)** The 8-bit value decides the high byte of CH0 write memory address.

7.17.5.17 CMDQ Interval Time Prescale Register (CMDQINVPR)

This register programs the clock scale between two CMDQ flows.

Address Offset: 10h

Bit	R/W	Default	Description
7-0	R/W	0h	**CMDQ Interval Time Prescale Register (CMDQINVPR)** The 8-bit value programs the clock scale between two CMDQ flows. 1 prescale clock cycle = M x SSPI clock 01h: 1 x SSPI clock cycles. 02h: 2 x SSPI clock cycles. … FFh: 255 x SSPI clock cycles.

7.17.5.18 Channel 0 Wait Time Scale Register for CMDQ (CH0WTSR)

This register programs the waiting time scale between two CMDQ flows for channel 0.

Address Offset: 11h

Bit	R/W	Default	Description
7-0	R/W	0h	**Channel 0 Wait Time Scale Register for CMDQ (CH0WTSR)** The 8-bit value programs the waiting time scale between two CMDQ flows for channel 0. Waiting time = N x 1 prescale clock cycle.

7.17.5.19 Channel 1 Command Address Low Byte Register (CH1CMDADDRLB)

This register controls the low byte command address of channel 1.

Address Offset: 12h

Bit	R/W	Default	Description
7-0	R/W	0h	**CH1 CMD Address Low Byte (CH1CMDADDRLB)** The 8-bit value decides the low byte of CH1 CMD address.

7.17.5.20 Channel 1 Command Address High Byte Register (CH1CMDADDRHB)

This register controls the high byte command address of channel 1.

Address Offset: 13h

Bit	R/W	Default	Description
7-0	R/W	0h	**CH1 CMD Address High Byte (CH1CMDADDRLB)** The 8-bit value decides the high byte of CH1 CMD address.

7.17.5.21 Channel 1 Write Memory Address Low Byte Register (CH1WRMEMADDRLB)

This register controls the low byte write memory address of channel 1.

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R/W	0h	**CH1 Write Memory Address Low Byte (CH1WRMEMADDRLB)** The 8-bit value decidess the low byte of CH1 write memory address.

7.17.5.22 Channel 1 Write Memory Address High Byte Register (CH1WRMEMADDRHB)

This register controls the high byte write memory address of channel 1.

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R/W	0h	**CH1 Write Memory Address High Byte (CH1WRMEMADDRHB)** The 8-bit value decidess the high byte of CH1 write memory address.

7.17.5.23 Channel 1 Wait Time Scale Register for CMDQ(CH1WTSR)

This register programs the waiting time scale between two CMDQ flows for channel 1.

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R/W	0h	**Channel 1 Wait Time Scale Register for CMDQ (CH1WTSR)** The 8-bit value programs the waiting time scale between two CMDQ flows for channel 1. Waiting time = N x 1 prescale clock cycle.

7.17.5.24 Channel 1 DMA Ring Depth Low Byte Register (CH1DMARDLB)

This register controls the low byte ring buffer depth of DMA for channel 1.

Address Offset: 17h

Bit	R/W	Default	Description
7-0	R/W	0h	**Channel 1 DMA Ring Depth Low Byte (CH1DMARDLB)** The value decides the low byte of DMA ring buffer depth for channel 1.

7.17.5.25 Channel 1 DMA Ring Depth High Byte Register (CH1DMARDHB)

This register controls the high byte ring buffer depth of DMA for channel 1.

Address Offset: 18h

Bit	R/W	Default	Description
7-5	R	-	**Reserved**
4-0	R/W	0h	**Channel 1 DMA Ring Depth High Byte (CH1DMARDHB)** The value decides the high byte of DMA ring buffer depth for channel 1.

7.17.5.26 Channel 0 Command Address High Byte 2 Register (CH0CMDADDRHB2)

This register controls the high byte 2 command address of Channel 0.

Address Offset: 21h

Bit	R/W	Default	Description
7-0	R/W	0h	**CH0 CMD Address High Byte 2 (CH0CMDADDRHB2)** The 8-bit value decides the high byte 2 of CH0 CMD address.

7.17.5.27 Channel 0 Write Memory Address High Byte 2 Register (CH0WRMEMADDRHB2)

This register controls the high byte 2 write memory address of Channel 0.

Address Offset: 23h

Bit	R/W	Default	Description
7-0	R/W	0h	**CH0 Write Memory Address High Byte 2 (CH0WRMEMADDRHB2)** The 8-bit value decides the high byte 2 of CH0 write memory address.

7.17.5.28 Channel 1 Command Address High Byte 2 Register (CH1CMDADDRHB2)

This register controls the high byte 2 command address of Channel 1.

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	0h	**CH1 CMD Address High Byte 2 (CH1CMDADDRHB2)** The 8-bit value decides the high byte 2 of CH1 CMD address.

7.17.5.29 Channel 1 Write Memory Address High Byte 2 Register (CH1WRMEMADDRHB2)

This register controls the high byte 2 write memory address of Channel 1.

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	0h	**CH1 Write Memory Address High Byte 2 (CH1WRMEMADDRHB2)** The 8-bit value decides the high byte 2 of CH1 write memory address.

7.17.5.30 Delay Select for SSPI Feedback Clock Register (DSFBCR)

This register controls the delay time of SSPI feedback clock.

Address Offset: 2Dh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0h	**Delay Times of SSPI Feedback Clock (DTFBC)** The value decides the delay time of the feedback clock. 0000b: no delay 0001b: delay 1 delay-cell time 0010b: delay 2 delay-cell time 0011b: delay 3 delay-cell time 0100b: delay 4 delay-cell time 0101b: delay 5 delay-cell time 0110b: delay 6 delay-cell time 0111b: delay 7 delay-cell time 1000b: delay 8 delay-cell time 1001b: delay 9 delay-cell time 1010b: delay 10 delay-cell time 1011b: delay 11 delay-cell time 1100b: delay 12 delay-cell time 1101b: delay 13 delay-cell time 1110b: delay 14 delay-cell time 1111b: delay 15 delay-cell time

7.17.5.31 SPI Receive Data for Dual/DTR Mode Register (SPIRDATA)

The register holds the shift data from the SPI device for the Dual/DTR mode.

Address Offset: 2Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**SPI Receive Data (RDATA)** Receives data from the SPI device for the Dual/DTR mode.

7.17.5.32 SPI Control Register 6 (SPICTRL6)

This register controls the SPI operation mode.

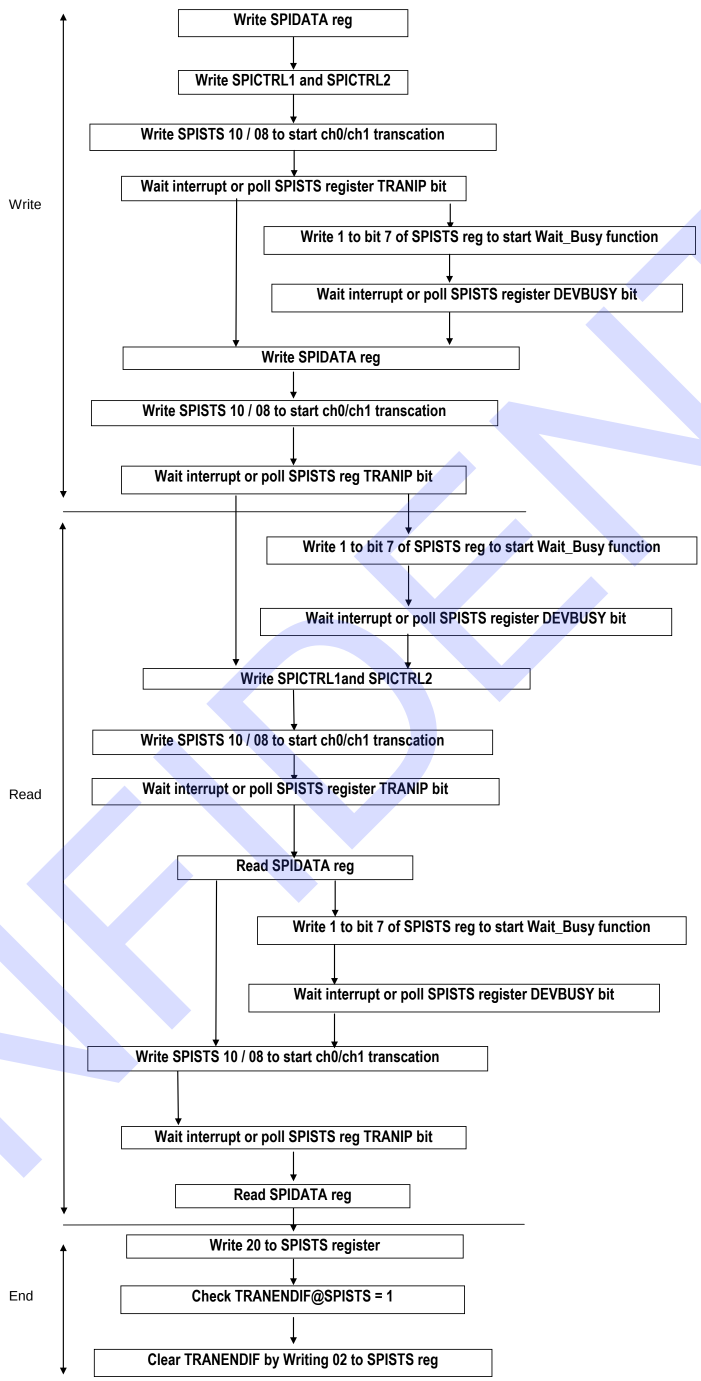
Address Offset: 33h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**One-wire Address Control for CMDQ Dual Mode (OWACCMDQDM)** This bit is used to control one-wire transmission of the address phase for CMDQ Dual mode. 0: The address phase is transmitted by dual wires. 1: The address phase is transmitted by one wire.
1	R/W	0b	**DTR Mode (DTRMODE)** 0: The DTR mode is disabled. 1: The DTR mode is enabled.
0	R/W	0b	**Dual Mode (DUALMODE)** 0: The Dual mode is disabled. 1: The Dual mode is enabled.

7.17.6 Programming Guide

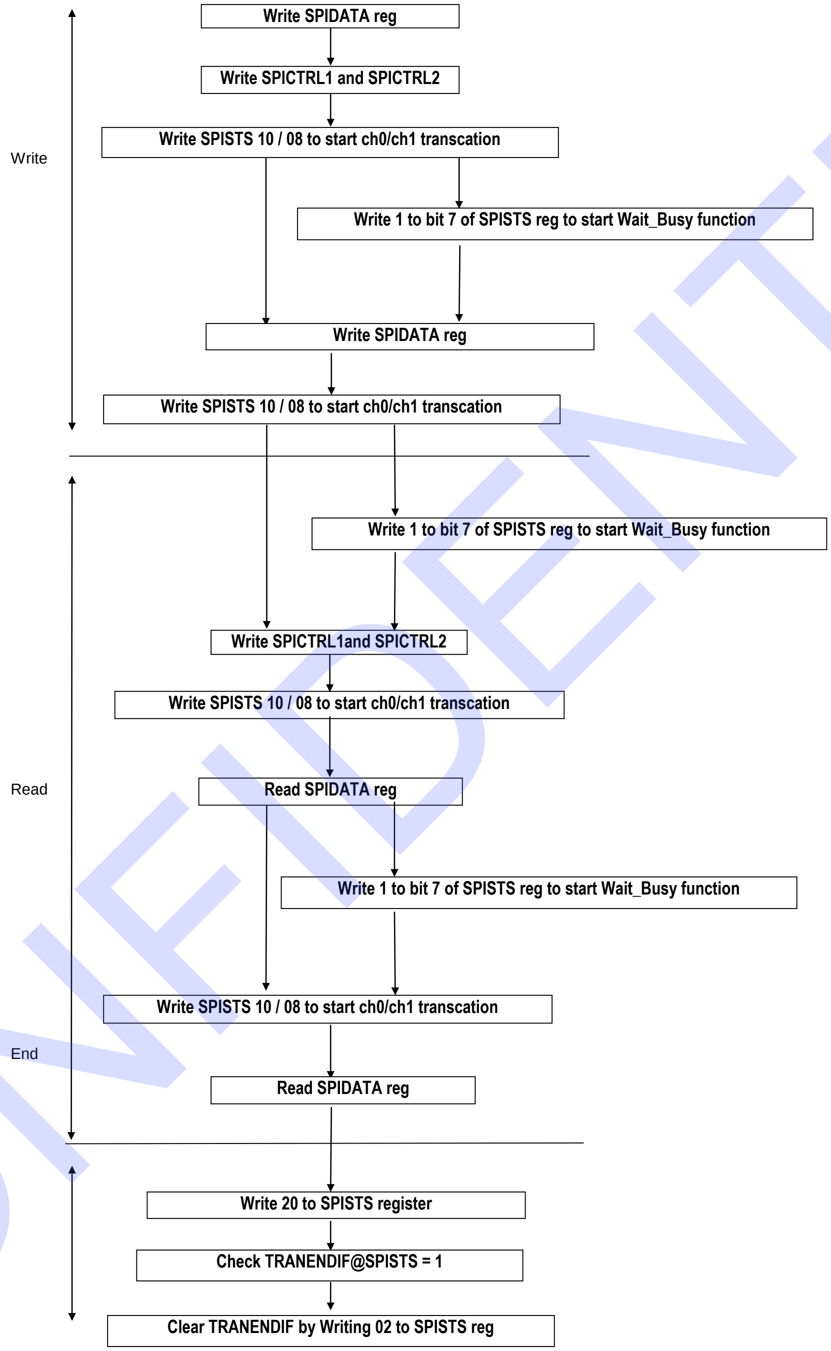
Write the 16-bit data to the SPI device and read the 16-bit data from the SPI device.

Figure 7-28. Program Flow Chart for SSPI Non-blocking



Write 16-bit data to SPI device and read 16-bit data from SPI device.

Figure 7-29. Program Flow Chart for SSPI Blocking



CMDQ mode: Write data to SPI device and read data from SPI device.

1. CPU prepares CMDQ CMD (ex: the Data_addr[15:0] = 0x6200), SPI instruction, address to memory(ex: 0xD100) and write transmit data to another memory(ex: 0x9200).
2. Write CH0 CMD address CH0CMDADDRLB and CH0CMDADDRHB (ex: 0x0100)
3. Write CH0 Write Memory address CH0WRMEMADDRLB and CH0WRMEMADDRHB (ex: 0x5000)
4. Write 0x11 to SPICTRL5 for enabling CH0 CMDQ mode

5. Wait interrupt or polling INTSTS register SPICMDQEND bit
6. Write INTSTS 0x07 to clear interrupt.
7. Check SRAM data (0x8000).

7.18 JTAG Bridge (JTAG)

7.18.1 Overview

The JTAG bridge module connects the JTAG interface and DBGR controller for CPU debug. .

7.18.2 Features

- Supports 5-wire JTAG standard interface.
- Supports JTAG clock up to 48MHz

7.18.3 Register Description

The following table lists all of the Interrupt Controller registers. Each register can be accessed by byte access only. The base address is 0x2DC0.

Table 7-33. EC View Register Map, JTAG Bridge

Register Name	R/W	Address	Default
Control Register	R/W	0x00	81h
Instruction Register	R/W	0x01	00h
Transmit Data Register	R/W	0x03	00h
Receive Data Register	R	0x04	00h
Debug Interrupt Maximum Interval Register	R/W	0x06	90h
BRAM FIFO Status Register	R	0x08	00h

7.18.3.1 Control Register

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	1	**dbgi_n Control** When random dbgi_n is disabled, users can set this bit to control dbgi_n 1: Debug interrupt de-asserted. 0: Debug interrupt asserted.
6	R/W	0	**Random dbgi_n Enable** When this bit is set, the dbgi_n will be asserted automatically.
5-1	-	0	**Reserved**
0	R/W	1	**TRST Control (Active Low)** 1: Trst de-asserted. 0: Trst asserted.

7.18.3.2 Instruction Register

Address Offset: 01h

Bit	R/W	Default	Description
7-4	-	0	**Reserved**
3-0	R/W	0h	**JTAG Instruction setting** The main instruction value and related shift-DR length are as the following: BYPASS: 4'b1111. 64-bit length.

Bit	R/W	Default	Description
			IDCODE: 4'b1001. 32-bit length EXECUTE: 4'b1000. 0-bit length GET_DBG_EVENT: 4'b0111. 5-bit length FAST_ACCESS_MEM: 4'b0110. 33-bit length ACCESS_MISC_REG: 4'b0101. 38-bit length ACCESS_MEM_B: 4'b1011. 42-bit length ACCESS_MEM_H: 4'b1010. 49-bit length ACCESS_MEM_W: 4'b0100. 64-bit length ACCSS_DTR: 4'b0011. 34-bit length ACCSS_EDM_SR: 4'b0010. 41-bit length ACCSS_DIM: 4'b0001. 34-bit length BSCAN: 4'b1110.

7.18.3.3 Transmit Data Register

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Register** Set the transmit data according to different instructions.

7.18.3.4 Receice Data Register

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Register** The register receives data from CPU TDO signal.

7.18.3.5 Debug Interrupt Maximum Interval Register

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	90h	**Debug Interrupt Maximum Interval** When random dbgi_n is enabled, the value is set for interrupt maximum interval.

7.18.3.6 BRAM FIFO Status Register

Address Offset: 08h

Bit	R/W	Default	Description
7	R	0b	**FIFO Data Available** 0: FIFO is empty. 1: Data is available.
6	R	-	**FIFO Full** 0: FIFO is not full. 1: FIFO is full.
5-0	R	-	**FIFO Data Count** Theses bits indicate the number of data left in FIFO.

7.19 Serial Port (UART)

7.19.1 Overview

UART1 can be accessed by software in the host or EC side; however, the UART1 function should be controlled by a side only.
So is UART2.

The UART1/UART2 module is 16550 compatible. This module performs the serial to parallel conversion for the received data, and parallel to serial conversion for the transmitted data.

7.19.2 Features

- Programmable FIFO or character mode
- The 16-byte FIFO buffer is on the transmitter and receiver in the FIFO mode
- Add or delete standard asynchronous communication bits (start, stop and parity) to or from serial data.
- The programmable baud rate generator allows the division of input clock by 1 to 2^16-1 and generates the internal 16X clock.
- Modem control function (CTS#, RTS#, DTR#, DSR#, RI#, DCD#)
- Fully programmable serial-interface characteristics: 5, 6, 7 or 8-bit character
- Even, odd, forced 0/1 or no parity bit generation and detection
- 1, 1½, or 2 stop bits generation
- Baud rate up to 115.2K
- Baud rate up to 230.4K/460.8K if high speed mode enabled
- False start bit detection
- Receiver/Transmitter can be enabled separately.

7.19.3 Functional Description

UART contains a programmable baud rate generator that is capable of dividing the input clock by a number from 1 to 65535. The data rate of each serial port can also be programmed from 115.2K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts. Besides, if the High Speed Baud Rate Select (HHS) or EC High Speed Select (ECHS) is activated, the highest baud rate can be up to 230.4K and 460.8K, which are determined by the divisor of the baud rate generator.

7.19.4 Host Interface Registers

The registers of UART1/UART2 can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.
The UART resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below:

Table 7-34. Host/EC View Register Map, UART

			Index
Receiver Buffer Register (RBR)	if DLAB=0	R	00h
Interrupt Enable Register (IER)	if DLAB=0	R/W	01h
Interrupt Identification Register (IIR)		R	02h
Line Control Register (LCR)		R/W	03h
Modem Control Register (MCR)		R/W	04h
Divisor Latch LSB Register (DLL)	if DLAB=1	R/W	00h
Divisor Latch MSB Register (DLM)	if DLAB=1	R/W	01h
Line Status Register (LSR)		R/W	05h
Modem Status Register (MSR)		R/W	06h
Scratch Pad Register (SCR)		R/W	07h
Transmitter Holding Register (THR)		W	00h
FIFO Control Register (FCR)		W	02h
EC Serial Port Mode Register (ECSPMR)	EC View	R/W	08h
Clock Source Select Register (CSSR)	EC View	R/W	09h

All registers are double mapped into the host and EC side except that ECSPMR and SPPR are only for EC side; however, the UART function should be controlled by a side only.

7.19.5 EC Interface Registers

The register map of EC interface is the the same as Host interface registers. The base address for UART1 is 2700h and the base address for UART2 is 2800h.

Other related register(s):

- General Control 1 Register (GCR1), U1CTRL bit
- General Control 1 Register (GCR1), U2CTRL bit
- General Control 3 Register (GCR3), UART1PDG bit
- General Control 3 Register (GCR3), UART2PDG bit

7.19.5.1 Receiver Buffer Register (RBR)

This register receives and holds the entering data. It contains a non-accessible shift register that converts the incoming serial data stream to a parallel 8-bit word.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R	00h	**Receiver Buffer Register (URBR)** This register receives and holds the entering data.

7.19.5.2 Transmitter Holding Register (THR)

This register holds and transmits the data via a non-accessible shift register. It converts the outgoing parallel data to a serial stream before transmission.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	W	-	**Transmitter Holding Register (THR)** This register holds and transmits the data via a non-accessible shift register.

7.19.5.3 Interrupt Enable Register (IER)

IER is used to enable (or disable) four active high interrupts that activate the interrupt outputs with its lower four

bits, bit 0-bit 3.

Address Offset: 01h

Bit	R/W	Default	Description
7-4	R	0h	**Reserved** These bits are always “0”.
3	R/W	-	**Enable Modem Status Interrupt (EMSI)** Set this bit high to enable the modem status interrupt when one of the modem status registers changes its bit state.
2	R/W	-	**Enable Receiver Line Status Interrupt (ERLSI)** Set this bit high to enable the receiver line status interrupt, which is caused when overrun, parity, framing or break occurs.
1	R/W	-	**Enable Transmitter Holding Register Empty Interrupt (ETHREI)** Set this bit high to enable the transmitter holding register empty interrupt.
0	R/W	-	**Enable Received Data Available Interrupt (ERDVI)** Set this bit high to enable the received data available interrupt (and time-out interrupt in the FIFO mode).

7.19.5.4 Interrupt Identification Register (IIR)

Address Offset: 02h

Bit	R/W	Default	Description
7-6	R	00b	**Interrupt Identification Register Bit 7, Bit 6 (IIR7, IIR6)** These bits are set when FCR[0] is equal to 1.
5-4	R	00b	**Reserved** Always logic 0.
3	R	0b	**Interrupt Identification Register Bit 3 (IIR3)** In the non-FIFO mode, this bit is logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out Interrupt is pending.
2-1	R	00b	**Interrupt Identification Register Bit 2, Bit 1 (IIR2, IIR1)** These bits are used to identify the highest priority pending interrupt.
0	R	1b	**Interrupt Identification Register Bit 0 (IIR0)** This bit is used to indicate a pending interrupt in either a hard-wired prioritized or a polled environment with a logic 0 state. When the condition takes place, IIR contents may be used as a pointer to the appropriate interrupt service routine.

Table 7-35. Interrupt Control Functions

IIR				Interrupt Set and Reset Functions			
Bit3	**Bit2**	**Bit1**	**Bit0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	-	None	None	-
0	1	1	0	1st	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	2nd	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or FIFO drops below the Trigger Level

IIR				Interrupt Set and Reset Functions			
Bit3	Bit2	Bit1	Bit0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
1	1	0	0	2nd	Character Timeout Identification	There is at least one character in the FIFO but no character has been input to the FIFO or read from it for the last four Char times.	Reading the Receiver Buffer Register
0	0	1	0	3rd	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if the source of interrupt is THRE) or Writing into the THR
0	0	0	0	4th	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

7.19.5.5 FIFO Control Register (FCR)

This register is used to enable, and clear the FIFO, and set the RCVR FIFO trigger level.

Address Offset: 02h

Bit	R/W	Default	Description
7-6	W	00b	**FIFO Control Register Bit 7, Bit 6 (FCR7,FCR6)** These bits set the trigger level for the RCVR FIFO interrupt. **FCR7 FCR6 RCVR FIFO Trigger Level** 0 0 1 byte 0 1 4 bytes 1 0 8 bytes 1 1 14 bytes
5-4	W	00b	**Reserved**
3	W	0b	**Reserved** This bit does not affect the serial channel operation. RXRDY and TXRDY functions are not available on this controller.
2	W	0b	**XMIT FIFO Reset (XFRST)** This self-clearing bit clears all contents of XMIT FIFO and resets its related counter to 0.
1	W	0b	**RCVR FIFO Reset (RFRST)** Set this self-clearing bit to logic “1” to clear all contents of RCVR FIFO and resets its related counter to 0 (except the shift register).
0	W	0b	**FIFO Enable (FEN)** XMIT and RCVR FIFOs are enabled when this bit is set high. XMIT and RCVR FIFOs will be disabled and cleared when this bit is cleared to low. This bit has to be a logic “1” if the other bits of the FCR are written or they will not be properly programmed. When this register is changed to the non-FIFO mode, all contents will be cleared.

7.19.5.6 Divisor Latch LSB (DLL)

There are two 8-bit Divisor Latches (DLL and DLM), which store the divisor in a 16-bit binary format. They are loaded during initialization to generate a desired Baud Rate.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Divisor Latch LSB (DLL)** This register stores the low byte of the divisor.

7.19.5.7 Divisor Latch MSB (DLM)

There are two 8-bit Divisor Latches (DLL and DLM), which store the divisor in a 16-bit binary format. They are loaded during initialization to generate a desired Baud Rate.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Divisor Latch LSB (DLM)** This register stores the high byte of the divisor.

Table 7-36. Baud Rate Using 1.8432MHz Clock

Desired Baud Rate	Divisor Used	Percent Error Difference[1]	High Speed Bit[2]
50	2304	-	X
75	1536	-	X
110	1047	0.1247	X
134.5	857	0.0409	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.5916	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	-	X
57600	2	-	X
115200	1	-	X
230400	32770	-	1
460800	32769	-	1

Note1: The percent error difference, which is between the desired and the actual value, for all baud rates is 0.0986% except where the baud rates are indicated otherwise.
Note2: The high speed bit indicates whether the HHS bit or ECHS bit is set to high or not.

7.19.5.8 Scratch Pad Register (SCR)

There are two 8-bit Divisor Latches (DLL and DLM), which store the divisor in a 16-bit binary format. They are loaded during initialization to generate a desired Baud Rate.

Address Offset: 07h

Bit	R/W	Default	Description

7-0	R/W	-	**Scratch Pad Register (SCR)** This 8-bit register does not control the operation of UART in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general-purpose data.

7.19.5.9 Line Control Register (LCR)

LCR controls the format of the data character and provides the information of the serial line.

Address Offset: 03h

Bit	R/W	Default	Description
7	R/W	-	**Divisor Latch Access Bit (DLAB)** This bit has to be set high to access the Divisor Latches of the baud rate generator during read or write operation and set low to access the Data Register (RBR and THR) or the Interrupt Enable Register.
6	R/W	-	**Break Control (BREAK)** This bit forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, and this state will remain until a low level resets this bit, enabling the serial port to alert the terminal in a communication system.
5	R/W	-	**Stick Parity Bit (SP)** When this bit and Parity Enable (PEN) bit are high at the same time, the parity bit is transmitted and then detected by the receiver. On the contrary, the parity bit is detected by Even Parity Select (EPS) bit to force the parity to a known state and to check the parity bit in a known state.
4	R/W	-	**Even Parity Select (EPS)** When the parity is enabled (Parity Enable=1), EPS=0 selects odd parity, and EPS=1 selects even parity.
3	R/W	-	**Parity Enable (PEN)** A parity bit, between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when this bit is high.
2	R/W	-	**Stop Bit Select (STB)** Specify the number of stop bits in each serial character, which is summarized below: **STB Word Length No. of Stop Bit** 0 - 1 bit 1 5 1.5 bits 1 6 2 bits 1 7 2 bits 1 8 2 bits **Note:** The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.
1-0	R/W	-	**Word Length Select Bit 1, Bit 0 (WLS1, WLS0)** Specify the number of bits in each serial character, which is encoded below: **WLS1 WLS0 Word Length** 0 0 5 bits 0 1 6 bits 1 0 7 bits 1 1 8 bits

7.19.5.10 Modem Control Register (MCR)

Address Offset: 04h

Bit	R/W	Default	Description
7-6	R	00b	**Reserved** Bit 7-5 are always low.

Bit	R/W	Default	Description
5	R/W	0b	**Hardware flow control** This bit enables the hardware flow control.
4	R/W	0b	**Loop** This bit provides a loopback feature for the diagnostic test of the serial channel when it is set high. Serial Output (SOUT) is set to the Marking State. Shift Register output Loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected, and the four are forced to inactive high. The transmitted data are immediately received, allowing the processor to verify the data paths of transmitting and receiving of the serial channel.
3	R/W	0b	**OUT2** The Output 2 bit enables the serial port interrupt output by a logic 1.
2	-	0b	**OUT1** This bit does not have an output pin and can only be read or written by the processor.
1	R/W	0b	**Request To Send (RTS)** This bit controls the Request to Send (RTS#), which is in an inverse logic state with it.
0	R/W	0b	**Data Terminal Ready (DTR)** This bit controls the Data Terminal Ready (DTR#), which is in an inverse logic state with it.

7.19.5.11 Line Status Register (LSR)

Address Offset: 05h

Bit	R/W	Default	Description
7	R/W	0b	**Error In RCVR FIFO (ERF)** In the 16550 mode, this bit is always 0. In the FIFO mode, it is set high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads LSR if there are no subsequent errors in the FIFO.
6	R	1b	**Transmitter Empty (TEMT)** This read-only bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty; otherwise, this bit is “0”. It has the same function in the FIFO mode.
5	R	1b	**Transmitter Holding Register Empty (THRE)** This read-only bit indicates that the THR is empty, and is ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty, and is cleared when at least one byte is written to XMIT FIFO.
4	R/W	0b	**Break Interrupt (BI)** This bit indicates that the last received character is a break character. The break interrupt status bit will be asserted only when the last received character, parity bits and stop bits are all break bits. When any of these error conditions is detected (LSR[1] to LSR[4]), a Receiver Line Status interrupt (priority 1) will be produced in IIR with IER[2] previously enabled.
3	RC	0b	**Framing Error (FE)** When this bit is a logic 1, it indicates that the stop bit in the received character is not valid. It is reset low when the CPU reads the contents of LSR.

Bit	R/W	Default	Description
2	RC	0b	**Parity Error (PE)** This bit Indicates the parity error (PE) with a logic "1", representing that the received data character does not have the correct even or odd parity as bit 3 of LCR (Parity Enable) is set to "1". It will be reset to "0" whenever LSR is read by CPU.
1	RC	0b	**Overrun Error (OE)** Overrun Error (OE) bit is set as a logic "1" after RBR has been overwritten by the next character before it is read by CPU. In the FIFO mode, OE occurs when FIFO is full and the next character has been completely received by the Shift Register. It will be reset when CPU reads LSR.
0	R/W	0b	**Data Ready (DR)** A logic "1" indicates a character has been received by RBR. A logic "0" indicates all data in the RBR or RCVR FIFO have been read.

7.19.5.12 Modem Status Register (MSR)

This 8-bit register provides the current state of the control lines from modems or peripheral devices. In addition to this current state information, bit 7-4 can provide the change information when a modem control input changes the state. It will be reset to low when the processor reads MSR.

Address Offset: 06h

Bit	R/W	Default	Description
7	R	0b	**Data Carrier Detect (DCD#)** This bit indicates the complement status of Data Carrier Detect input. If bit 4 of MCR is 1, this bit is equivalent to OUT2 of MCR.
6	R	0b	**Ring Indicator (RI#)** This bit indicates the complement to the RI# input. If bit 4 of MCR is 1, this bit is equivalent to OUT1 in MCR.
5	R	0b	**Data Set Ready (DSR#)** This bit indicates the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the loop mode (bit 5 of MCR is 1), this bit is equivalent to DTR# in the MCR.
4	R	0b	**Clear to Send (CTS#)** This bit indicates the complement of CTS# input. If the serial channel is in the loop mode (bit 4 of MCR is 1), this bit is equivalent to RTS# in MCR.
3	R/W	0b	**Delta Data Carrier Detect (DDCD)** This bit indicates that the DCD# input state has been changed since the last time it is read by the processor.
2	R/W	0b	**Trailing Edge of Ring Indicator (TERI)** This bit indicates that RI input state to the serial channel has been changed from a low to high state since the last time it is read by the processor. The change of logic 1 doesn't activate TERI.
1	R/W	0b	**Delta Data Set Ready (DDSR)** A logic "1" indicates that DSR# input state to the serial channel has been changed since the last time it is read by the processor.
0	R/W	0b	**Delta Clear to Send (DCTS)** This bit indicates the CTS# input state to the serial channel has been changed since the last time it is read by the processor.

7.19.5.13 EC Serial Port Mode Register (ECSPMR)

Address Offset: 08h

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7-2	-	00h	**Reserved** Bit 7-2 are always low.
1	R/W	0b	**EC High Speed Select (ECHS)** This bit indicates that the supported baud rate of UART1/UART2 can be up to 230.4K and 460.8K, which are determined by the divisor of the baud rate generator. (From EC Side) 0: Not selected 1: Selected
0	-	0b	**Reserved** This bit is always low.

7.19.5.14 Clock Source Select Register (CSSR)

Address Offset: 09h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved** Bit 7-5 are always low.
1-0	R/W	01h	**Clock Source Select (CSS)** The two bits indicate that the clock source of UART is 16MHz, 24MHz or 32MHz. This setting must match the CLK_UART_DIV_SEL and this will determine the generation of baud rate 230.4K and 460.8K. (From EC Side) 00: Frequency of clk_uart is equal to 16MHz 01: Frequency of clk_uart is equal to 24MHz 10: Frequency of clk_uart is equal to 32MHz 11: Frequency of clk_uart is equal to 32MHz

7.19.6 Programming Guide

Each serial channel is programmed by control registers whose contents define the character length, number of stop bits, parity, baud and modem interface. Although the control registers can be written in any order, IER should be the last because it controls whether the interrupt is enabled. After the port is programmed, these registers can still be updated whenever the port is not transferring data.

Before using the UART, the SPPR must be set properly. The relationship between PLL frequency and the UART clock source is listed as below.

clk_pll / (CLK_UART_DIV_SEL+1) = clk_uart
clk_uart / UART_SRC_DIV = 1.8432MHz

For example, if PLLFREQ is set to 0111b, ie clk_pll is 96MHz, the recommended value of CLK_UART_DIV_SEL is 03h, so that clk_uart is 24MHz. Then the UART_SRC_DIV can be set to 0dh to generate a clock of 1.846MHz which is close to 1.8432MHz.

7.19.6.1 Programming Sequence

UART module in Intelligent Peripheral Controller is compatible with standard 16550. The following is the programming sequence for standard 16550 compatible component register.

For access RBR/THR:
1. Set bit 7 of the LCR register to “0”.
2. Access RBR/THR.

For Access IER:
1. Set bit 7 of the LCR register to “0”.

2. Access IER.

For Access DLL/DLM:
1. Set bit 7 of the LCR register to “1”.
2. Access DLL/DLM.

7.19.7 Software Reset

This method allows returning to a completely known state without a system reset. It consists of writing the required data to LCR, DLL, DLM and MCR. LSR and RBR has to be read before enabling interrupts in order to clear any residual data or status bits that may be invalid for the subsequent operations.

If UART function is controlled by the EC side, it can be done by writing 1 to the corresponding bit in RSTC4 register, too.

7.19.8 Clock Input Operation

The input frequency of the Serial Channel is FreqEC/5, not exactly 1.8432 MHz.
FreqEC is listed in Table 10-2 on page 570.

7.19.9 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

When bit 0 of FCR and bit 0 of IER are set to 1, RCVR FIFO and receiver interrupts are enabled. RCVR interrupt occurs under the following conditions:

A. The received data available interrupt and the IIR receive data available indication will be issued only if the FIFO has reached its programmed trigger level. They will be cleared as soon as the FIFO drops below its trigger level.

B. The receiver line status interrupt has higher priority than the received data available interrupt.

C. The time-out timer will be reset after receiving a new character or after the processor reads RCVR FIFO whenever a time-out interrupt occurs.

RCVR FIFO time-out Interrupt: By enabling RCVR FIFO and receiver interrupts, the RCVR FIFO time-out interrupt will occur under the following conditions:

A. It will occur only if there is at least one character in FIFO whenever the period between the most recent received serial character and the most recent processor read from the FIFO is longer than the period of four consecutive character-time.
B. The time-out timer will be reset after receiving a new character or after the processor reads RCVR FIFO whenever any time-out interrupts occur. The timer will be reset when the processor reads one character from RCVR FIFO.

(2) XMIT Interrupt

By setting bit 0 of FCR and bit 1 of IER to high, the XMIT FIFO and transmitter interrupts are enabled, and the XMIT interrupt will occur as follows:

A. The transmitter interrupt will occur when XMIT FIFO is empty, and it will be reset if THR is written or IIR is read.
B. The transmitter FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following conditions occurs:
THRE=1 and there are not at least two bytes in the transmitter FIFO at the same time since the last THRE=1.
The transmitter interrupt will be issued immediately after the bit 0 of FCR is changed. Once it is enabled, the

THRE indication is delayed for 1 character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts are in the same priority order as the received data available interrupt. The XMIT FIFO empty is in the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation (Bit 0 of FCR is 1, and bit 0, 1, 2, 3 of IER or all are 0.)
Either one or both XMIT and RCVR can be in this operation mode in which the program will check RCVR and XMIT status via the LSR as described below:

LSR[7]: RCVR FIFO error indication.
LSR[6]: XMIT FIFO and Shift register empty.
LSR[5]: The XMIT FIFO empty indication.
LSR[4] – LSR[1]: Specify that errors have occurs, and the character error status is handled in the same way as in the interrupt mode. IIR is not affected since IER(2)=0.
LSR[0]: This bit is high whenever RCVR FIFO contains at least one byte. There is no trigger level reached or time-out condition indicated in the FIFO Polled Mode.

7.19.10 High Speed Baud Rate Activation

When the high speed baud rate select bit is set to 1 from host side (High Speed Baud Rate Select ; HHS) or EC side (EC High Speed Select ; ECHS), the highest baud rate of UART1/UART2 can be up to 230.4K or 460.8K, which are determined by the divisor of the baud rate generator.

If HHS or ECHS is set to 1 and the divisor is 32770, the baud rate is 230.4K.
If HHS or ECHS is set to 1 and the divisor is 32769, the baud rate is 460.8K.

7.20 USBPD Controller

7.20.1 Overview

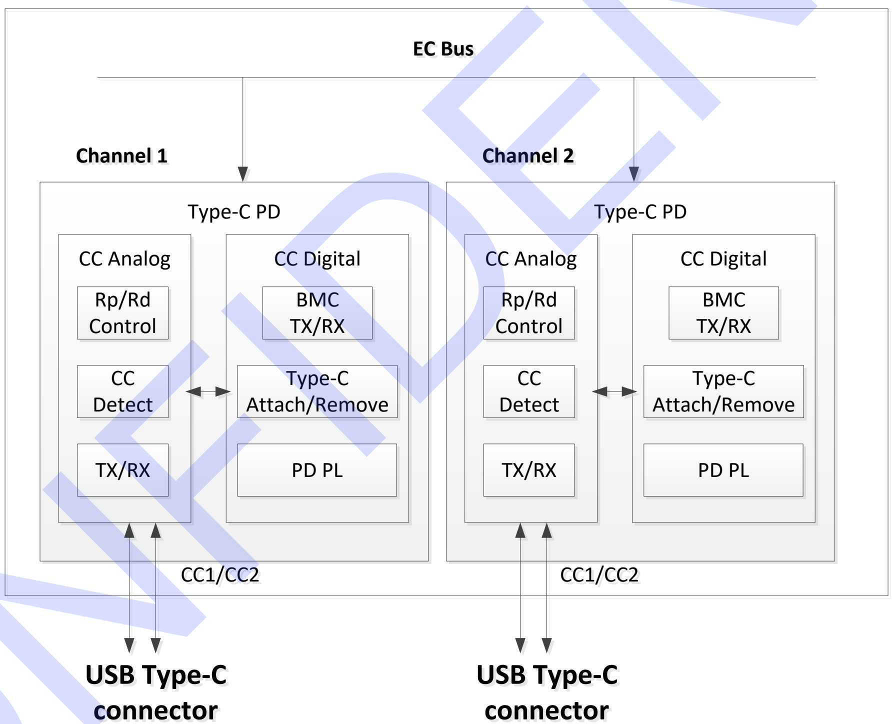
This module supports the USBPD Type-C Power Delivery handshaking and USBPD Type-C assert/remove detection.

7.20.2 Features

- UFP (5.1K resistor to GND)/DFP (USB Default/1.5A/3.0A)/DRP support
- BMC decode/encode
- USB Type-C assert/remove detection (Sink/Source/Audio/Debug mode)
- Detection for USB Type-C assert direction
- Hardware engine for CRC32 check and generation

7.20.3 Block Diagram

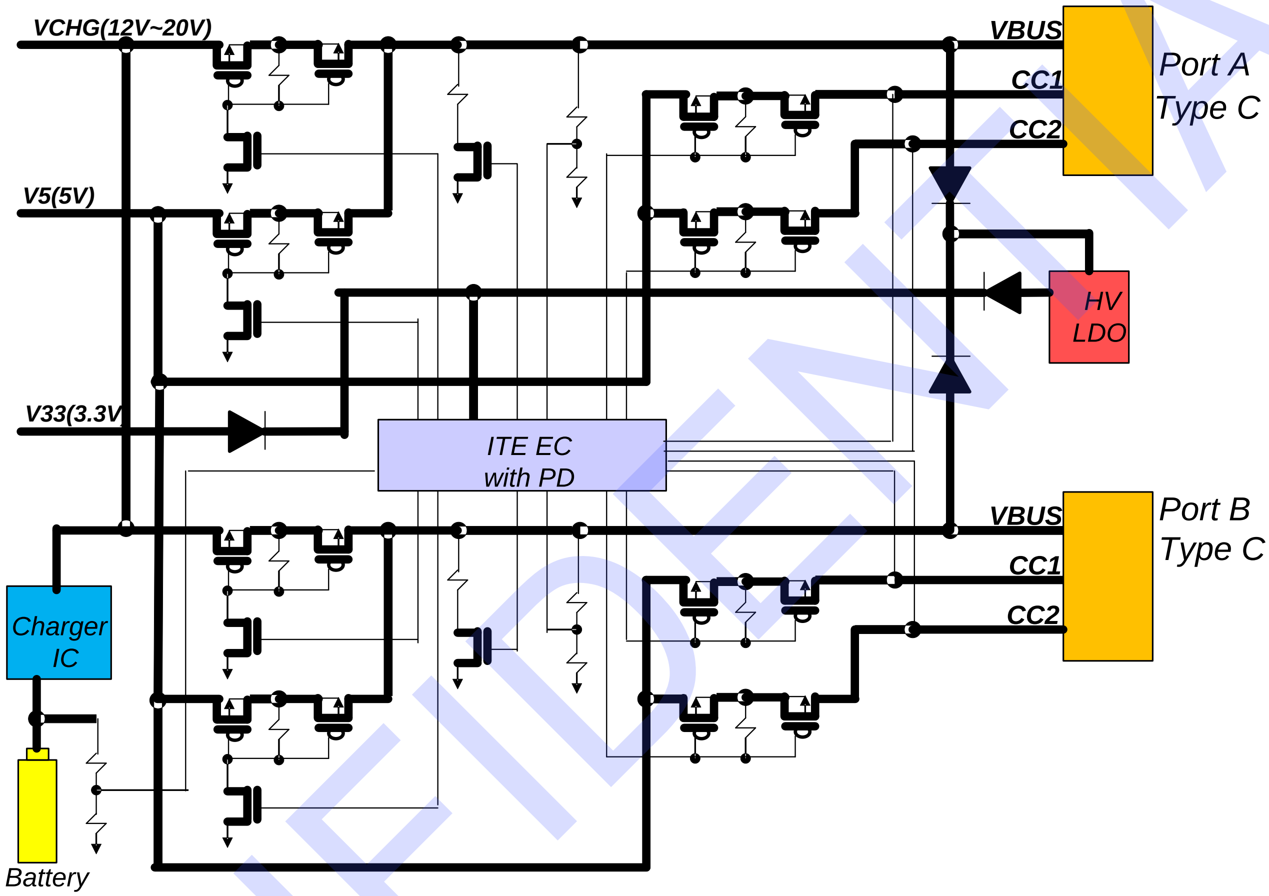
Figure 7-30. USBPD Controller Block Diagram



7.20.4 System Architecture

A two-port Type-C system architecture is demonstrated here. To increase/decrease one port, users just need to copy/remove a group of circuits.

Figure 7-31. USBPD System Architecture Diagram



7.20.5 EC Interface Registers

The register map of EC interface is listed below.
The base address for USBPD Port1 is 3700h and for USBPD Port2 is 3800h.

Table 7-37. List of USBPD Controller Register

Register Name	R/W	Address	Default
PD General Control Register (PDGCR)	R/W[Note1]	0x00	0Ch
PD Control Setting Register 0 (PDCSR0)	R/W	0x01	ABh
PD Mode Selection Register (PDMSR)	R/W	0x02	FFh
PD Control Setting Register 1 (PDCSR1)	R/W	0x03	01h
CC General Configuration Register (CCGCR)	R/W[Note1]	0x04	C1h
CC Channel Setting Register (CCCSR)	R/W[Note1]	0x05	88h
CC Pad Setting Register (CCPSR)	R/W[Note1]	0x06	22h

SRC Voltage Compare Result Register (SRCVCRR)	R	0x08	33h
SNK Voltage Compare Result Register (SNKVCRR)	R	0x09	00h
CC Compare Control Register 0 (CCCCR0)	R/W Note1	0x0A	03h
CC Compare Control Register 1 (CCCCR1)	R/W Note1	0x0B	01h
PD Fast Role Swap Control Register (PDFRSCR)	R/W Note1	0x0C	50h
Timescale of Fast Role Swap Register 0 (TFRSR0)	R/W	0x0D	40h
Timescale of Fast Role Swap Register 1 (TFRSR1)	R/W	0x0E	FFh
Timescale of Fast Role Swap Register 2 (TFRSR2)	R/W	0x0F	B4h
Timescale of Tx GoodCRC (TTXGCRC)	R/W	0x10	15h
Timescale of Rx GoodCRC (TRXGCRC)	R/W Note1	0x11	10h
Interrupt for Fast Role Swap (IFRS)	R/WC Note1	0x12	00h
Mask of Interrupt for Fast Role Swap (MIFRS)	R/W Note1	0x13	A2h
Interrupt for Tx & Rx (ITR)	R/WC Note1	0x14	00h
Mask of Interrupt for Tx & Rx (MITR)	R/W Note1	0x15	77h
Timescale of Frame Gap Register (TFGR)	R/W	0x16	40h
Message Packet Setting Register 0 (MPSR0)	R/W	0x17	00h
Message Transmission Control Register (MTCR)	W Note1	0x18	00h
Message Transmission Setting Register 0 (MTSR0)	R/W Note1	0x19	00h
Message Header Setting Register 0 (MHSR0)	R/W	0x1A	00h
Message Header Setting Register 1 (MHSR1)	R/W	0x1B	00h
Message ID Status Register 0 (MIDSR0)	R Note1	0x1C	00h
Message ID Status Register 1 (MIDSR1)	R Note1	0x1D	00h
Message ID Status Register 2 (MIDSR2)	R Note1	0x1E	00h
Message ID Status Register 3 (MIDSR3)	R Note1	0x1F	00h
Transmitted Header Register 0 (THR0)	R	0x20	00h
Transmitted Header Register 1 (THR1)	R	0x21	00h
Transmit Data Object 0 Register 0 (TDO0R0)	R/W	0x22	00h
Transmit Data Object 0 Register 1 (TDO0R1)	R/W	0x23	00h
Transmit Data Object 0 Register 2 (TDO0R2)	R/W	0x24	00h
Transmit Data Object 0 Register 3 (TDO0R3)	R/W	0x25	00h
Transmit Data Object 1 Register 0 (TDO1R0)	R/W	0x26	00h
Transmit Data Object 1 Register 1 (TDO1R1)	R/W	0x27	00h
Transmit Data Object 1 Register 2 (TDO1R2)	R/W	0x28	00h
Transmit Data Object 1 Register 3 (TDO1R3)	R/W	0x29	00h
Transmit Data Object 2 Register 0 (TDO2R0)	R/W	0x2A	00h
Transmit Data Object 2 Register 1 (TDO2R1)	R/W	0x2B	00h
Transmit Data Object 2 Register 2 (TDO2R2)	R/W	0x2C	00h
Transmit Data Object 2 Register 3 (TDO2R3)	R/W	0x2D	00h
Transmit Data Object 3 Register 0 (TDO3R0)	R/W	0x2E	00h

Transmit Data Object 3 Register 1 (TDO3R1)	R/W	0x2F	00h
Transmit Data Object 3 Register 2 (TDO3R2)	R/W	0x30	00h
Transmit Data Object 3 Register 3 (TDO3R3)	R/W	0x31	00h
Transmit Data Object 4 Register 0 (TDO4R0)	R/W	0x32	00h
Transmit Data Object 4 Register 1 (TDO4R1)	R/W	0x33	00h
Transmit Data Object 4 Register 2 (TDO4R2)	R/W	0x34	00h
Transmit Data Object 4 Register 3 (TDO4R3)	R/W	0x35	00h
Transmit Data Object 5 Register 0 (TDO5R0)	R/W	0x36	00h
Transmit Data Object 5 Register 1 (TDO5R1)	R/W	0x37	00h
Transmit Data Object 5 Register 2 (TDO5R2)	R/W	0x38	00h
Transmit Data Object 5 Register 3 (TDO5R3)	R/W	0x39	00h
Transmit Data Object 6 Register 0 (TDO6R0)	R/W	0x3A	00h
Transmit Data Object 6 Register 1 (TDO6R1)	R/W	0x3B	00h
Transmit Data Object 6 Register 2 (TDO6R2)	R/W	0x3C	00h
Transmit Data Object 6 Register 3 (TDO6R3)	R/W	0x3D	00h
Receive Header Register 0 (RHR0)	R	0x42	00h
Receive Header Register 1 (RHR1)	R	0x43	00h
Receive Data Object 0 Register 0 (RDO0R0)	R	0x44	00h
Receive Data Object 0 Register 1 (RDO0R1)	R	0x45	00h
Receive Data Object 0 Register 2 (RDO0R2)	R	0x46	00h
Receive Data Object 0 Register 3 (RDO0R3)	R	0x47	00h
Receive Data Object 1 Register 0 (RDO1R0)	R	0x48	00h
Receive Data Object 1 Register 1 (RDO1R1)	R	0x49	00h
Receive Data Object 1 Register 2 (RDO1R2)	R	0x4A	00h
Receive Data Object 1 Register 3 (RDO1R3)	R	0x4B	00h
Receive Data Object 2 Register 0 (RDO2R0)	R	0x4C	00h
Receive Data Object 2 Register 1 (RDO2R1)	R	0x4D	00h
Receive Data Object 2 Register 2 (RDO2R2)	R	0x4E	00h
Receive Data Object 2 Register 3 (RDO2R3)	R	0x4F	00h
Receive Data Object 3 Register 0 (RDO3R0)	R	0x50	00h
Receive Data Object 3 Register 1 (RDO3R1)	R	0x51	00h
Receive Data Object 3 Register 2 (RDO3R2)	R	0x52	00h
Receive Data Object 3 Register 3 (RDO3R3)	R	0x53	00h
Receive Data Object 4 Register 0 (RDO4R0)	R	0x54	00h
Receive Data Object 4 Register 1 (RDO4R1)	R	0x55	00h
Receive Data Object 4 Register 2 (RDO4R2)	R	0x56	00h
Receive Data Object 4 Register 3 (RDO4R3)	R	0x57	00h
Receive Data Object 5 Register 0 (RDO5R0)	R	0x58	00h

Receive Data Object 5 Register 1 (RDO5R1)	R	0x59	00h
Receive Data Object 5 Register 2 (RDO5R2)	R	0x5A	00h
Receive Data Object 5 Register 3 (RDO5R3)	R	0x5B	00h
Receive Data Object 6 Register 0 (RDO6R0)	R	0x5C	00h
Receive Data Object 6 Register 1 (RDO6R1)	R	0x5D	00h
Receive Data Object 6 Register 2 (RDO6R2)	R	0x5E	00h
Receive Data Object 6 Register 3 (RDO6R3)	R	0x5F	00h
BMC Decoder Register 0 (BMCDR0)	R/W	0x61	08h
Interrupt for PD Controller TX Busy (IPDCTXB)	R[Note1]	0x62	10h
Mask of Interrupt for PD Controller TX Busy (MIPDCTXB)	R/W[Note1]	0x63	81h
BMC Decoder Register 1 (BMCDR1)	R/W	0x64	00h
CC Test Mode Enable Register (CCTMER)	R/W[Note1]	0x66	00h
Type-C Detect Control Register (TCDCR)	R/W[Note1]	0x67	00h
PD GPIO Control Register (PDGPCR)	R/W[Note1]	0x6C	00h
PD GPIO Enable Register (PDGPER)	R/W[Note1]	0x6D	00h
CC Parameter Setting Register 0 (CCPSR0)	R/W[Note1]	0x70	00h
CC Parameter Setting Register 1 (CCPSR1)	R/W[Note1]	0x71	00h
CC Parameter Setting Register 2 (CCPSR2)	R/W[Note1]	0x72	00h
CC Parameter Setting Register 3 (CCPSR3)	R/W[Note1]	0x73	00h
CC Parameter Setting Register 4 (CCPSR4)	R/W[Note1]	0x74	00h
CC Parameter Setting Register 5 (CCPSR5)	R/W[Note1]	0x75	00h

Note 1: Not all bits have the same property, look in the regiseter to see the detail.
For the summary of the abbreviations used for the register types, see “Register Abbreviations and Access Rules”.

7.20.5.1 PD General Control Register (PDGCR)

Address Offset: 00h

Bit	R/W	Default	Description
7	W	0h	**Soft Reset** Write 1’b1 to this bit to generate a software reset signal for all PD function.
6	W	0h	**Protocol State Clear** Write 1’b1 to this bit to generate a software reset signal for PL and PHY function.
5	W	0h	**TX Message Discard** Write 1’b1 to this bit to control USBPD discard message.
4	R	0h	**BIST DATA Mode Status** According to the PD specification, it is necessary to enter the BIST mode until “Hard Reset/Plug-Out” when a “Bist_Data” message is recived. 1’b0: Not in BIST mode 1’b1: In BIST mode

Bit	R/W	Default	Description
3	R/W	1h	**Auto BIST Response** When the BIST mode is entered and this bit set to 1, the PD controller will not inform CPU when any message except Hard_Reset is received and automatically respond GoodCRC. 1'b0: CPU will be informed and the Rx buffer needs to be cleared. 1'b1: CPU will not be informed and the PD controller will automaticallymatically respond all messages.
2	R/W	1h	**TX Message Enable/Lock** Message TX Enable. 1'b0: Disable the function that CPU uses USBPD to TX. 1'b1: Enable the function that CPU uses USBPD to TX.
1	R/W	0h	**Sniffer Mode** In the sniffer mode, the USBPD PE and PL function is disabled, and will not automatically generate GoodCRC message while PHY is receiving message. 1'b0: Disable 1'b1: Enable
0	R/W	0h	**USBPD PHY Enable** When USBPD PHY is disabled, the RX FSM in PHY will not receive any message. 1'b0: Disable USBPD PHY. 1'b1: Enable USBPD PHY.

7.20.5.2 PD Control Setting Register 0 (PDCSR0)

Address Offset: 01h

Bit	R/W	Default	Description
7-6	R/W	2h	**Retry Count Select** 2'b00: No retry 2'b01: 1 retry 2'b10: 2 retry 2'b11: 3 retry
5	R/W	1h	**Disable Message ID Check** This bit is used for the protocol layer to adjust the decoder for "Normal PD Message". Use this bit to set the decoder for whether to check the ID counter if a normal PD message is received. **Note:** When message ID checking is disabled, all messages including the retry message will be reported. 1'b0: Check 1'b1: Don't care
4	R/W	0h	**Device Role Setting for SOP' and SOP''** This bit is used to generate GoodCRC and PD message's header. 1'b0: Sink/Source 1'b1: Cable
3	R/W	1h	**Check Soft Reset's ID Counter** This bit is used for the protocol layer to adjust the decoder for "Soft Reset". Use this bit to set decoder check/not check ID counter if a Soft Reset message is received. 1'b0: Don't care 1'b1: Check

Bit	R/W	Default	Description
2	R/W	0h	**Ping Ignore** PL Tx Interrupt by Ping Message Enable/Disable. 1'b0: PL will stop the tx message flow (tx discard) while rx a ping message. 1'b1: PL will not cancel the message to tx while rx a ping message.
1	R/W	1h	**SOP',SOP'' Ignore** PL Tx Interrupt by "not SOP" Message Enable/Disable. 1'b0: PL will stop the tx message flow (tx discard) while rx a "not SOP" message. 1'b1: PL will not cancel the message to tx while rx a "not SOP" message
0	R/W	1h	**Check GoodCRC ID Enable** This bit is used for the protocol layer to adjust the decoder for "GoodCRC". Setting this bit for the decorder to check/not to check the ID counter if a "GoodCRC" message is received. 1'b0: Don't care. 1'b1: Check.

7.20.5.3 PD Mode Selection Register (PDMSR)

Address Offset: 02h

Bit	R/W	Default	Description
7	R/W	1h	**Auto Generating Transmit Message Header** The transmit message header will be generated automatically in PL function. Set this bit to 1'b0 to disable this function, after which the transmit header for PHY will be the content in Tx_HDR_REG (0x1A~0x1B). 1'b0: The transmit message header is from Tx_HDR_REG (0x1A~0x1B). 1'b1: Enable automatically generating transmit message header.
6	R/W	1h	**Auto Fast Role Swap Request/Detect Disable** If this bit is set to 1, Fast Role Swap Request/Detect function will be automaticaly disabled when Rx a soft/hard reset message. 1'b0: Disable 1'b1: Enable
5	R/W	1h	**Auto Fast Role Swap Request (Source Role)** If this bit is set to 1, the usbpd controller will automatically pull CC pin to GND if external power lose is detected. 1'b0: Disable 1'b1: Enable
4	R/W	1h	**Auto Message Length** If this bit is set to 1, the usbpd controller will reference Header's Info to adjust message's length to transmit. 1'b0: Disable 1'b1: Enable
3	R/W	1h	**Auto TX Discard Increase ID** If this bit is set to 1, the usbpd controller will automatically increase the message ID counter when message transmission is discarded. 1'b0: Disable 1'b1: Enable

Bit	R/W	Default	Description
2	R/W -	1h	**Auto ID Counter Clear** If this bit is set to 1, the usbpd controller will automatically clear the meesage ID counter when transmitting or recieving the soft reset message. 1'b0: Disable 1'b1: Enable
1	R/W	1h	**Auto RX GoodCRC** If this bit is set to 1, the usbpd controller will check GoodCRC response in time after transmitting a PD message. If no GoodCRC response is received, it will retry by setting (0x01[7:6]). 1'b0: Disable 1'b1: Enable
0	R/W	1h	**Auto TX GoodCRC** If this bit is set to 1, the usbpd controller will automatically respond GoodCRC after reciving a legal USBPD message. 1'b0: Disable 1'b1: Enable

7.20.5.4 PD Control Setting Register 1 (PDCSR1)

Address Offset: 03h

Bit	R/W	Default	Description
7	R/W	0h	**Order Set Match Setting** 1'b0: The message is interpreted as valid if there are more than or equal to 3/4 SOP matched. 1'b1: The message is interpreted as valid if there are 4/4 SOP matched.
6	R/W	0h	**Cable Reset RX Enable** Use this bit to set the decoder to make it capable of decoding "Cable Reset". 1'b0: Disable 1'b1: Enable
5	R/W	0h	**Hard Reset RX Enable** Use this bit to set the decoder to make it capable of decoding "Hard Reset". 1'b0: Disable 1'b1: Enable
4	R/W	0h	**SOP'' Debug RX Enable** Use this bit to set the decoder to make it capable of decoding "SOP" Debug". 1'b0: Disable 1'b1: Enable
3	R/W	0h	**SOP' Debug RX Enable** Use this bit to set the decoder to make it capable of decoding "SOP' Debug". 1'b0: Disable 1'b1: Enable
2	R/W	0h	**SOP'' RX Enable** Use this bit to set the decoder to make it capable of decoding "SOP" Type": 1'b0: Disable 1'b1: Enable

Bit	R/W	Default	Description
1	R/W	0h	**SOP' RX Enable** Use this bit to set the decoder to make it capable of decoding "SOP' Type". 1'b0: Disable 1'b1: Enable
0	R/W	1h	**SOP RX Enable** Use this bit to set the decoder to make it capable of decoding "SOP Type" 1'b0: Disable 1'b1: Enable

7.20.5.5 CC General Configuration Register (CCGCR)

Address Offset: 04h

Bit	R/W	Default	Description
7	R/W	1h	**Power Down CC1 & CC2 (pd_all_cc_reg)** 1'b0: Enable CC1 & CC2 1'b1: Disable CC1 & CC2
6	R/W	1h	**Disable CC1 & CC2 Voltage Detector** 1'b0: Enable 1'b1: Disable
5-4	-	-	**Reserved**
3-1	R/W	0h	**CC Output Current (when R_p selected)** 3'b110: Connect Default Rp (80uA) 3'b100: Connect 1.5A Rp (180uA) 3'b010: Connect 3.0A Rp (330uA) 3'b111: Reserved
0	R/W	1h	**CC1/CC2 Selection** 1'b0: CC2 1'b1: CC1

7.20.5.6 CC Channel Setting Register (CCCSR)

Address Offset: 05h

Bit	R/W	Default	Description
7	R/W	1h	**Dis-connect CC2 with UP/RD/DET/Tx/Rx** 1'b0: Connect 1'b1: Dis-connect
6	R/W	0h	**Dis-connect CC2 with 5.1K Resistor to GND** 1'b0: Connect with 5.1K 1'b1: Dis-connect with 5.1K
5	R/W	0h	**CC2 R_p/R_d Selection** 1'b0: Select R_d (Sink) 1'b1: Select R_p (Source)
4	-	-	**Reserved**
3	R/W	1h	**Dis-connect CC1 with UP/RD/DET/Tx/Rx** 1'b0: Connect 1'b1: Dis-connect
2	R/W	0h	**Dis-connect CC1 with 5.1K Resistor to GND** 1'b0: Connect with 5.1K 1'b1: Dis-connect with 5.1K

Bit	R/W	Default	Description
1	R/W	0h	**CC1 R_p/R_d Selection** 1’b0: Select R_d (Sink) 1’b1: Select R_p (Source)
0	-	-	**Reserved**

7.20.5.7 CC Pad Setting Register (CCPSR)

Address Offset: 06h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0h	**Dis-connect 5.1K Resistor to CC2 in DB** 1’b0: Connect with 5.1K 1’b1: Dis-connect with 5.1K
5	R/W	1h	**Dis-connect 5V Tolerant with CC2** When CC2 is going to source VCONN, this bit must be set to 1’b0. 1’b0: Enable 1’b1: Disable
4-3	-	-	**Reserved**
2	R/W	0h	**Dis-connect 5.1K Resistor to CC1 in DB** 1’b0: Connect with 5.1K 1’b1: Dis-connect with 5.1K
1	R/W	1h	**Dis-connect 5V Tolerant with CC1** When CC1 is going to source VCONN, this bit must be set to 1’b0. 1’b0: Enable 1’b1: Disable
0	-	-	**Reserved**

7.20.5.8 SRC Voltage Compare Result Register (SRCVCRR)

Address Offset: 08h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0h	**CC2 High Voltage Compare Result in Source Mode** This bit will be set to 1’b1 on the following conditions: 1. CC2 > 1.6 V in Source default USB (0.9A) mode 2. CC2 > 1.6 V in Source 1.5A mode 3. CC2 > 2.6 V in Source 3.0A mode Otherwise, it will be set to 1’b0.
4	R/W	0h	**CC2 Low Voltage Compare Result in Source Mode** This bit will be set to1’b1 on the following conditions: 1. CC2 > 0.2V in Source default USB (0.9A) mode 2. CC2 > 0.4V in Source 1.5A mode 3. CC2 > 0.8V in Source 3.0A mode Otherwise, it will be set to 1’b0.
3-2	-	-	**Reserved**

Bit	R/W	Default	Description
1	R/W	0h	**CC1 High Voltage Compare Result in Source Mode** This bit will be set to 1'b1 on the following conditions: 1. CC1 > 1.6 V in Source default USB (0.9A) mode 2. CC1 > 1.6 V in Source 1.5A mode 3. CC1 > 2.6 V in Source 3.0A mode Otherwise, this bit will be set to 1'b0
0	R/W	0h	**CC1 Low Voltage Compare Result in Source Mode** This bit will be set to1'b1 on the following conditions: 1. CC1 > 0.2V in Source default USB (0.9A) mode 2. CC1 > 0.4V in Source 1.5A mode 3. CC1 > 0.8V in Source 3.0A mode Otherwise, this bit will be set to 1'b0

7.20.5.9 SNK Voltage Compare Result Register (SNKVCRR)

Address Offset: 09h

Bit	R/W	Default	Description
7	R/W	0h	**CC2 Fast Role Swap Voltage Compare Result in Sink Mode** This bit will be set to 1'b1 when CC2 > 0.5V in Sink mode.
6	R/W	0h	**CC2 High Voltage Compare Result in Sink Mode** This bit will be set to 1'b1 when CC2 > 1.23V in Sink mode. Otherwise, this bit will be set to 1'b0.
5	R/W	0h	**CC2 Middle Voltage Compare Result in Sink Mode** This bit will be set to 1'b1 when CC2 > 0.66V in Sink mode. Otherwise, this bit will be set to 1'b0.
4	R/W	0h	**CC2 Low Voltage Compare Result in Sink Mode** This bit will be set to 1'b1 when CC2 > 0.2V in Sink mode. Otherwise, this bit will be set to 1'b0.
3	R/W	0h	**CC1 Fast Role Swap Voltage Compare Result in Sink Mode** This bit will be set to 1'b1 when CC1 > 0.5V in Sink mode.
2	R/W	0h	**CC1 High Voltage Compare Result in Sink Mode** This bit will be set to 1'b1 when CC1 > 1.23V in Sink mode. Otherwise, this bit will be set to 1'b0.
1	R/W	0h	**CC1 Middle Voltage Compare Result in Sink Mode** This bit will be set to 1'b1 when CC1 > 0.66V in Sink mode. Otherwise, this bit will be set to 1'b0.
0	R/W	0h	**CC1 Low Voltage Compare Result in Sink Mode** This bit will be set to 1'b1 when CC1 > 0.2V in Sink mode. Otherwise, this bit will be set to 1'b0.

7.20.5.10 CC Compare Control Register 0 (CCCCR0)

Address Offset: 0Ah

Bit	R/W	Default	Description
7	R/W	0h	**Comparator Choose CC2 as Source Input** 1'b0: Dis-Connect 1'b1: Connect
6	R/W	0h	**Comparator Choose CC1 as Source Input** 1'b0: Dis-Connect 1'b1: Connect

Bit	R/W	Default	Description
5-4	R/W	0h	**CC Voltage Compare Threshold Select** DFP: 2'b00: (0.2/0.4/0.8V) 2'b01: (1.6/1.6/2.6V) UFP: 2'b00: 0.2V 2'b01: 0.66V 2'b10: 1.23V 2'b11: Threshold 0.52V
3	R/W	0h	**CC Connect Pin Scan Select** If "auto connect pin select" function is disabled, use this bit to select CC1/CC2 as comparator's source when TypeC's connection is in the attached state. 1'b0: CC2 1'b1: CC1
2	-	-	**Reserved**
1	R/W	1h	**Auto CC Connect Pin Select** When this bit is set to 1 and "Fast Role Swap detect" function is enabled, the connect cc pin to scan will be auto selected. 1'b0: Manual (0x0A[3]) 1'b1: Auto
0	R/W	1h	**Auto CC Voltage Scan** Use this bit to auto scan CC1 voltage and CC2 voltage. 1'b0: Manual (0x0A[7:4]) 1'b1: Auto

7.20.5.11 CC Compare Control Register 1 (CCCCR1)

Address Offset: 0Bh

Bit	R/W	Default	Description
7	R	-	**CC DET Result Temporarily** This bit indicates the CC voltage pin's compared result from the comparator.
6-1	-	-	**Reserved**
0	R/W	1h	**Fast Role Swap Detect Voltage Setting** Use this bit to set the voltage threshold for Fast Role Swap. 1'b0: 0.2V 1'b1: 0.5V

7.20.5.12 PD Fast Role Swap Control Register (PDFRSCR)

Address Offset: 0Ch

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	5h	**External Power Detect Source Select** 3'd0: From Comparator 0 3'd1: From Comparator 1 3'd2: From Comparator 2 3'd3: From Comparator 3 3'd4: From Comparator 4 3'd5: From Comparator 5

Bit	R/W	Default	Description
3	R/W	0h	**Fast Role Swap Detect Mode Setting** 1’b0: Wait R_p re-appear 1’b1: Don’t care R_p re-appear or not
2	R/W	0h	**Do Fast Role Swap Request** When 0x0C[1] is 1,write 1 to request Fast Role Swap (connect 5Ω resister to GND)
1	R/W	0h	**Fast Role Swap Request Enable** (External Power Detect, Auto Request, Manual Request function) 1’b0: Disable 1’b1: Enable
0	R/W	0h	**Fast Role Swap Detect Enable** 1’b0: Disable 1’b1: Enable

7.20.5.13 Timescale of Fast Role Swap Register 0 (TFRSR0)

Address Offset: 0Dh

Bit	R/W	Default	Description
7-0	R/W	40h	**Fast Role Swap Detect Timescale0** Minimum time of CC <0.5V Time: 8’d0: 0us 8’d1: 0.667us 8’d2: 1.334us … 8’d255: 170us

7.20.5.14 Timescale of Fast Role Swap Register 1 (TFRSR1)

Address Offset: 0Eh

Bit	R/W	Default	Description
7-0	R/W	FFh	**Fast Role Swap Detect Timescale1** Maximum time of R_p re-appear Time: 8’d0: 0us 8’d1: 0.667us 8’d2: 1.334us … 8’d255: 170us

7.20.5.15 Timescale of Fast Role Swap Register 2 (TFRSR2)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	R/W	B4h	**Fast Role Swap Request Timescale** Time of 5Ω Resister to GND. Time: 8'd0: 0us 8'd1: 0.667us 8'd2: 1.334us … 8'd255: 170us

7.20.5.16 Timescale of Tx GoodCRC (TTXGCRC)

Address Offset: 10h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4-0	R/W	15h	**Tx GoodCRC TimeOut Timescale** PD Spec: 195us Time: 5'd0: 0us 5'd1: 8us … 5'd31:248: us

7.20.5.17 Timescale of Rx GoodCRC (TRXGCRC)

Address Offset: 11h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4-0	R/W	10h	**Rx GoodCRC TimeOut Timescale** PD Spec: 900~1100us Time: 5'd0: 0us 5'd1: 64us 5'd2: 128us . 5'd31: 1984us

7.20.5.18 Interrupt for Fast Role Swap (IFRS)

Address Offset: 12h

Bit	R/W	Default	Description
7	-	-	**Interrupt for All Fast Role Swap** Interrupt of 0x12 [5:4],0x12[1]
6	-	-	**Reserved**

Bit	R/W	Default	Description
5	R/WC	0h	**Interrupt for External Power Loss** Detect external power loss (source role) 1'b0: None 1'b1: Power loss detected
4	R/WC	0h	**Interrupt for Fast Role Swap Detected (Sink Role)** 1'b0: None 1'b1: Fast Role Swap request detected
3-2	-	-	**Reserved**
1	R/WC	0h	**Interrupt for CC BUSY** CC Bus Status Detect. 1'b0: Idle 1'b1: Busy
0	R/WC	0h	**CRC Rx Timeout** Tx timeout by GoodCRC response not received. 1'b0: None 1'b1: Timeout

7.20.5.19 Mask of Interrupt for Fast Role Swap (MIFRS)

Address Offset: 13h

Bit	R/W	Default	Description
7	R/W	1h	**Mask for All Fast Role Swap** 1'b0: Un-mask 1'b1: Mask
6	-	-	**Reserved**
5	R/W	1h	**Mask for External Power Loss** 1'b0: Un-mask 1'b1: Mask
4	R/W	1h	**Mask for Fast Role Swap Detected(Sink Role)** 1'b0: Un-mask 1'b1: Mask
3-2	-	-	**Reserved**
1	R/W	1h	**Mask for CC BUSY** 1'b0: Un-mask 1'b1: Mask
0	-	-	**Reserved**

7.20.5.20 Interrupt for Tx & Rx (ITR)

Address Offset: 14h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/WC	0h	**Interrupt for Cable Reset Detected**
5	R/WC	0h	**Interrupt for Hard Reset Detected**
4	R/WC	0h	**Interrupt for Message Received**
3	R	0h	**Transmit Error Status** 1'b0: Transmission ok 1'b1: Transmission error (GoodCRC message not received)
2	R/WC	0h	**Interrupt for Cable Reset Transmitted Done**

Bit	R/W	Default	Description
1	R/WC	0h	**Interrupt for Hard Reset Transmitted Done**
0	R/WC	0h	**Interrupt for Message Transmitted Done**

7.20.5.21 Mask of Interrupt for Tx & Rx (MITR)

Address Offset: 15h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	1h	**Mask for Cable Reset Detected** 1’b0: Un-mask 1’b1: Mask
5	R/W	1h	**Mask for Hard Reset Detected** 1’b0: Un-mask 1’b1: Mask
4	R/W	1h	**Mask for Message Received** 1’b0: Un-mask 1’b1: Mask
3	-	-	**Reserved**
2	R/W	1h	**Mask for Cable Reset Transmitted Done** 1’b0: Un-mask 1’b1: Mask
1	R/W	1h	**Mask for Hard Reset Transmitted Done** 1’b0: Un-mask 1’b1: Mask
0	R/W	1h	**Mask for Message Transmitted Done** 1’b0: Un-mask 1’b1: Mask

7.20.5.22 Timescale of Frame Gap Register (TFGR)

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R/W	40h	**Frame Gap Timescale** PD Spec: 25us (Bit step: 0.5us)

7.20.5.23 Message Packet Setting Register 0 (MPSR0)

Address Offset: 17h

Bit	R/W	Default	Description
7-6	R/W	0h	**PD GoodCRC Header Version** PD Spec: 2’b01
5-4	R/W	0h	**Message Length: Last DWord’s Half Byte Number**
3-0	R/W	0h	**Message Length: DWord’s Number**

7.20.5.24 Message Transmission Control Register (MTCR)

Address Offset: 18h

Bit	R/W	Default	Description
7	R/WC	0h	**Message Transmit Discard Flag** Transmission discarded by other message 1'b0: None 1'b1: TX fails
6	R/WC	0h	**Message Transmit No Response Flag** No GoodCRC response and retry times arrive. 1'b0: None 1'b1: TX fails
5	R/WC	0h	**Message Transmit Error cause by not enable Flag** TX Function not enabled. 1'b0: None 1'b1: TX fails
4	R	0h	**CC Bus Busy** 1'b0: IDLE 1'b1: Busy
3	W	0h	**Send Cable Reset Signaling** Write '1' to this bit will make the controller to issue the Cable Reset signal.
2	W	0h	**Send Hard Reset Signaling** Write '1' to this bit will make the controller to issue the Hard Reset signal.
1	R/W	0h	**Send BIST Mode2 Pattern** Setting this bit to '1' will make the controller to send the BIST Mode2 signal.
0	W	0h	**Transmit Message Start Bit** Write '1' to this bit will transmit a message.

7.20.5.25 Message Transmission Setting Register 0 (MTSR0)

Address Offset: 19h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	0h	**SOP Type of Receive Message** 3'b00: SOP 3'b001: SOP' 3'b010: SOP'' 3'b011: Debug_SOP' 3'b100: Debug_SOP'' 3'b101: Hard reset 3'b110: Cable reset
3	-	-	**Reserved**
2-0	R/W	0h	**Tx SOP type** 2'b000: SOP 2'b001: SOP' 2'b010: SOP'' 2'b011: Debug_SOP' 2'b100: Debug_SOP''

7.20.5.26 Message Header Setting Register 0 (MHSR0)

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Header Low (tx_header [7:0])**

7.20.5.27 Message Header Setting Register 1 (MHSR1)

Address Offset: 1Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Header High (tx_header [7:0])**

7.20.5.28 Message ID Status Register 0 (MIDSR0)

Address Offset: 1Ch

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/WC	0h	**SOP’ Receiver Message ID Counter/Debug SOP” ID Reset** READ: It shows the current SOP’ message id of the receiver side. Write Clear: Write ‘1’ to this bit to clear the tx message id counter and rx message id counter. Bit4: Reset the Debug_SOP” message id counter
3	WC	0h	**Debug SOP’ ID Reset** Write Clear: write this bit one to clear tx message id counter and rx message id counter. Bit3: Reset Debug_SOP’ message id counter
2-0	R/WC	0h	**SOP Receiver Message ID Counter/ SOP* ID Reset** READ: It shows the current SOP message id of the receiver side. Write Clear: write this bit one to clear tx message id counter and rx message id counter. Bit0: Reset SOP message id counter Bit0: Reset SOP’ message id counter Bit0: Reset SOP” message id counter

7.20.5.29 Message ID Status Register 1 (MIDSR1)

Address Offset: 1Dh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R	0h	**SOP’’ Receiver Message ID Counter** It shows the current SOP’’ message id of the receiver side.

7.20.5.30 Message ID Status Register 2 (MIDSR2)

Address Offset: 1Eh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**

Bit	R/W	Default	Description
2-0	R	0h	**Debug SOP' Receiver Message ID Counter** It shows the current Debug SOP' message id of the receiver side.

7.20.5.31 Message ID Status Register 3 (MIDSR3)

Address Offset: 1Fh

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	0h	**Transmit Message ID Counter** It shows the current message id of the transmit side.
3	-	-	**Reserved**
2-0	R	0h	**Debug SOP'' Receiver Message ID Counter** It shows the current Debug SOP'' message id of the receiver side.

7.20.5.32 Transmitted Header Register 0 (THR0)

Address Offset: 20h

Bit	R/W	Default	Description
7-0	R	00h	**Transmit Header Low (tx_header [7:0])** It shows the message header that finally transmmits.

7.20.5.33 Transmitted Header Register 1 (THR1)

Address Offset: 21h

Bit	R/W	Default	Description
7-0	R	00h	**Transmit Header High (tx_header [7:0])** It shows the message header that finally transmmits.

7.20.5.34 Transmit Data Object 0 Register 0 (TDO0R0)

Address Offset: 22h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 0 (tx_data0[7:0])**

7.20.5.35 Transmit Data Object 0 Register 1 (TDO0R1)

Address Offset: 23h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 0 (tx_data0[15:8])**

7.20.5.36 Transmit Data Object 0 Register 2 (TDO0R2)

Address Offset: 24h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 0 (tx_data0[23:16])**

7.20.5.37 Transmit Data Object 0 Register 3 (TDO0R3)

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 0 (tx_data0[32:24])**

7.20.5.38 Transmit Data Object 1 Register 0 (TDO1R0)

Address Offset: 26h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 1 (Tx_data1[7:0])**

7.20.5.39 Transmit Data Object 1 Register 1 (TDO1R1)

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 1 (Tx_data1[15:8])**

7.20.5.40 Transmit Data Object 1 Register 2 (TDO1R2)

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 1 (Tx_data1[23:16])**

7.20.5.41 Transmit Data Object 1 Register 3 (TDO1R3)

Address Offset: 29h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 1 (Tx_data1[31:24])**

7.20.5.42 Transmit Data Object 2 Register 0 (TDO2R0)

Address Offset: 2Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 2 (Tx_data2[7:0])**

7.20.5.43 Transmit Data Object 2 Register 1 (TDO2R1)

Address Offset: 2Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 2 (Tx_data2[15:8])**

7.20.5.44 Transmit Data Object 2 Register 2 (TDO2R2)

Address Offset: 2Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 2 (Tx_data2[23:16])**

7.20.5.45 Transmit Data Object 2 Register 3 (TDO2R3)

Address Offset: 2Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 2 (Tx_data2[31:24])**

7.20.5.46 Transmit Data Object 3 Register 0 (TDO3R0)

Address Offset: 2Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 3 (Tx_data3[7:0])**

7.20.5.47 Transmit Data Object 3 Register 1 (TDO3R1)

Address Offset: 2Fh

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 3 (Tx_data3[15:8])**

7.20.5.48 Transmit Data Object 3 Register 2 (TDO3R2)

Address Offset: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 3 (Tx_data3[23:16])**

7.20.5.49 Transmit Data Object 3 Register 3 (TDO3R3)

Address Offset: 31h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 3 (Tx_data3[31:24])**

7.20.5.50 Transmit Data Object 4 Register 0 (TDO4R0)

Address Offset: 32h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 4 (Tx_data4[7:0])**

7.20.5.51 Transmit Data Object 4 Register 1 (TDO4R1)

Address Offset: 33h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 4 (Tx_data4[15:8])**

7.20.5.52 Transmit Data Object 4 Register 2 (TDO4R2)

Address Offset: 34h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 4 (Tx_data4[23:16])**

7.20.5.53 Transmit Data Object 4 Register 3 (TDO4R3)

Address Offset: 35h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 4 (Tx_data4[31:24])**

7.20.5.54 Transmit Data Object 5 Register 0 (TDO5R0)

Address Offset: 36h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 5 (Tx_data5[7:0])**

7.20.5.55 Transmit Data Object 5 Register 1 (TDO5R1)

Address Offset: 37h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 5 (Tx_data5[15:8])**

7.20.5.56 Transmit Data Object 5 Register 2 (TDO5R2)

Address Offset: 38h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 5 (Tx_data5[23:16])**

7.20.5.57 Transmit Data Object 5 Register 3 (TDO5R3)

Address Offset: 39h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 5 (Tx_data5[31:24])**

7.20.5.58 Transmit Data Object 6 Register 0 (TDO6R0)

Address Offset: 3Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 6 (Tx_data6[7:0])**

7.20.5.59 Transmit Data Object 6 Register 1 (TDO6R1)

Address Offset: 3Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 6 (Tx_data6[15:8])**

7.20.5.60 Transmit Data Object 6 Register 2 (TDO6R2)

Address Offset: 3Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 6 (Tx_data6[23:16])**

7.20.5.61 Transmit Data Object 6 Register 3 (TDO6R3)

Address Offset: 3Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Object 6 (Tx_data6[31:24])**

7.20.5.62 Receive Header Register 0 (RHR0)

Address Offset: 42h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Message Header Low (rx_header [7:0])**

7.20.5.63 Receive Header Register 1 (RHR1)

Address Offset: 43h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Message Header High (rx_header [15:8])**

7.20.5.64 Receive Data Object 0 Register 0 (RDO0R0)

Address Offset: 44h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 0 (Rx_data0[7:0])**

7.20.5.65 Receive Data Object 0 Register 1 (RDO0R1)

Address Offset: 45h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 0 (Rx_data0[15:8])**

7.20.5.66 Receive Data Object 0 Register 2 (RDO0R2)

Address Offset: 46h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 0 (Rx_data0[23:16])**

7.20.5.67 Receive Data Object 0 Register 3 (RDO0R3)

Address Offset: 47h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 0 (Rx_data0[31:24])**

7.20.5.68 Receive Data Object 1 Register 0 (RDO1R0)

Address Offset: 48h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 1 (Rx_data1[7:0])**

7.20.5.69 Receive Data Object 1 Register 1 (RDO1R1)

Address Offset: 49h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 1 (Rx_data1[15:8])**

7.20.5.70 Receive Data Object 1 Register 2 (RDO1R2)

Address Offset: 4Ah

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 1 (Rx_data1[23:16])**

7.20.5.71 Receive Data Object 1 Register 3 (RDO1R3)

Address Offset: 4Bh

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 1 (Rx_data1[31:24])**

7.20.5.72 Receive Data Object 2 Register 0 (RDO2R0)

Address Offset: 4Ch

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 2 (Rx_data2[7:0])**

7.20.5.73 Receive Data Object 2 Register 1 (RDO2R1)

Address Offset: 4Dh

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 2 (Rx_data2[15:8])**

7.20.5.74 Receive Data Object 2 Register 2 (RDO2R2)

Address Offset: 4Eh

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 2 (Rx_data2[23:16])**

7.20.5.75 Receive Data Object 2 Register 3 (RDO2R3)

Address Offset: 4Fh

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 2 (Rx_data2[31:24])**

7.20.5.76 Receive Data Object 3 Register 0 (RDO3R0)

Address Offset: 50h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 3 (Rx_data3[7:0])**

7.20.5.77 Receive Data Object 3 Register 1 (RDO3R1)

Address Offset: 51h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 3 (Rx_data3[15:8])**

7.20.5.78 Receive Data Object 3 Register 2 (RDO3R2)

Address Offset: 52h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 3 (Rx_data3[23:16])**

7.20.5.79 Receive Data Object 3 Register 3 (RDO3R3)

Address Offset: 53h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 3 (Rx_data3[31:24])**

7.20.5.80 Receive Data Object 4 Register 0 (RDO4R0)

Address Offset: 54h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 4 (Rx_data4[7:0])**

7.20.5.81 Receive Data Object 4 Register 1 (RDO4R1)

Address Offset: 55h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 4 (Rx_data4[15:8])**

7.20.5.82 Receive Data Object 4 Register 2 (RDO4R2)

Address Offset: 56h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 4 (Rx_data4[23:16])**

7.20.5.83 Receive Data Object 4 Register 3 (RDO4R3)

Address Offset: 57h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 4 (Rx_data4[31:24])**

7.20.5.84 Receive Data Object 5 Register 0 (RDO5R0)

Address Offset: 58h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 5 (Rx_data5[7:0])**

7.20.5.85 Receive Data Object 5 Register 1 (RDO5R1)

Address Offset: 59h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 5 (Rx_data5[15:8])**

7.20.5.86 Receive Data Object 5 Register 2 (RDO5R2)

Address Offset: 5Ah

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 5 (Rx_data5[23:16])**

7.20.5.87 Receive Data Object 5 Register 3 (RDO5R3)

Address Offset: 5Bh

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 5 (Rx_data5[31:24])**

7.20.5.88 Receive Data Object 6 Register 0 (RDO6R0)

Address Offset: 5Ch

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 6 (Rx_data6[7:0])**

7.20.5.89 Receive Data Object 6 Register 1 (RDO6R1)

Address Offset: 5Dh

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 6 (Rx_data6[15:8])**

7.20.5.90 Receive Data Object 6 Register 2 (RDO6R2)

Address Offset: 5Eh

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 6 (Rx_data6[23:16])**

7.20.5.91 Receive Data Object 6 Register 3 (RDO6R3)

Address Offset: 5Fh

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Object 6 (Rx_data6[31:24])**

7.20.5.92 BMC Decoder Register 0 (BMCDR0)

Address Offset: 61h

Bit	R/W	Default	Description
7	R/W	0h	**BMC Decoder Dynamic Calibrate Enable** Use this bit to enable the BMC bit rate dynamic calibration. 1’b0: Disable 1’b1: Enable

Bit	R/W	Default	Description
6-0	R/W	08h	**BMC Rx Threshold** Use these bits to select the BMC receiver threshold according to the power role. 7'b100_0000: Ultra sourcing power 7'b010_0000: Sourcing power 7'b000_1000: Power neutral 7'b000_0010: Sinking power 7'b000_0001: Ultra sinking power Others: Reserved

7.20.5.93 Interrupt for PD Controller TX Busy (IPDCTXB)

Address Offset: 62h

Bit	R/W	Default	Description
7	R	0h	**Interrupt of Fast Role Swap Detect for Sleep Wakeup (Sink Role)** 1'b0: None 1'b1: Fast Role Swap Request detected
6-5	-	-	**Reserved**
4	R/W	1h	**USBPD Controller Transmmit Busy Interrupt Enable** 1'b0: Disable 1'b1: Enable
3	-	-	**Reserved**
2	R	0h	**USBPD TX Hard/Cable Reset** 1'b0: None 1'b1: Busy
1	R	0h	**USBPD TX Normal Message** 1'b0: None 1'b1: Busy
0	R	0h	**Interrupt of USBPD Controller Transmmit Busy** 1'b0: None 1'b1: Controller TX busy

7.20.5.94 Mask of Interrupt for PD Controller TX Busy (MIPDCTXB)

Address Offset: 63h

Bit	R/W	Default	Description
7	R/W	1h	**Mask for Fast Role Swap Detect for Sleep Wakeup** 1'b0: Enable 1'b1: Mask and Disable
6-1	-	-	**Reserved**
0	R/W	1h	**Mask for USBPD Controller Transmmit Busy** 1'b0: Enable 1'b1: Mask and Disable

7.20.5.95 BMC Decoder Register 1 (BMCDR1)

Address Offset: 64h

Bit	R/W	Default	Description
7-6	R/W	0x00	**Rx De-glitch Level** BMC Signal Deglitch time select: 2'b00: bypass mode 2'b01: 250ns 2'b10: 500ns 2'b11: 750ns
5-3	R/W	0x00	**BMC Sample Point Select (Back Half Bit)**
2-0	R/W	0x00	**BMC Sample Point Select (Front Half Bit)**

7.20.5.96 CC Test Mode Enable Register (CCTMER)

Address Offset: 66h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-4	R/W	0h	**CC Test Mode 3 Select (BIST)**
3	-	-	**Reserved**
2	R/W	0h	**CC Test Mode 2 Select**
1	R/W	0h	**CC Test Mode 2 Enable**
0	R/W	0h	**CC Test Mode 1 Enable**

7.20.5.97 Type-C Detect Control Register (TCDCR)

Address Offset: 67h

Bit	R/W	Default	Description
7	R/W	0h	**Plug-out Detect Type Select (Be Source Role)** 1'b0: Detect sink device removed 1'b1: Detect audio/debug device removed
6	R/W	0h	**Plug-in/out Select** 1'b0: Detect Type-C plug-in 1'b1: Detect Type-C plug-out (Be Source Role only)
5	R/W	1h	**Mask of PD3.0 SinkTXOK** 1'b0: Un-mask 1'b1: Mask
4	R/WC	0h	**PD3.0 SinkTXOK Interrupt (CC arrives 3V)**
3	R/W	1h	**Mask of PD3.0 SinkTXNG** 1'b0: Un-mask 1'b1: Mask
2	R/WC	0h	**PD3.0 SinkTXNG Interrupt (CC leaves 3V)**
1	R/W	1h	**Mask and Disable for Plug-in/out Detect** 1'b0: Enable 1'b1: Mask and Disable
0	R/WC	0h	**Interrupt of Type-C Device Plug-in/out**

7.20.5.98 PD GPIO Control Register (PDGPCR)

Address Offset: 6Ch

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	0h	**GPH3 (port1)/GPH4 (port2) Control** 1'b0: GPIO output low 1'b1: GPIO output high
0	R/WC	0h	**Fast Role Swap Detect Status for GPIO (Sink Role)** This status is a subsidiary of usbpd+0x12[4]. It is necessary to use usbpd+0x12[4] first to take effect. 1'b0: None 1'b1: Fast Role Swap request detected

7.20.5.99 PD GPIO Enable Register (PDGPER)

Address Offset: 6Dh

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0h	**GPH3(port1)/GPH4(port2) Enable** Enable this bit to let GPH3 (port1) or GPH4 (port2) be controlled by USBPD. 1'b0: Disable 1'b1: Enable
3-2	-	-	**Reserved**
1	R/W	0h	**GPIO Out Inverse Select** While GPIO being controlled by FRS is disabled (Bit0 is disabled.): 1'b0: Not inverse (If the control register (usbpd+0x6C[1]) is 1, GPIO will be output high.) 1'b1: Inverse (If the control register (usbpd+0x6C[1]) is 1, GPIO will be output low.) While GPIO being controlledby FRS is enabled (Bit0 is enabled): 1'b0: Not inverse (One of FRS or the control register is 1,GPIO will be output high.) 1'b1: Inverse (One of FRS or the control register is 1,GPIO will be output low.)
0	R/W	0h	**GPIO Controlled by FRS Status (usbpd+0x6C[0])** 1'b0: Disable (GPIO only controlled by 0x6C[1]) 1'b1: Enable (GPIO controlled by 0x6C[1] and 0x6C[0])

7.20.5.100 CC Parameter Setting Register 0 (CCPSR0)

Address Offset: 70h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	0h	**Tx RC Filters Tuning**

7.20.5.101 CC Parameter Setting Register 1 (CCPSR1)

Address Offset: 71h

Bit	R/W	Default	Description

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4-0	R/W	00h	**CC IP Current Tuning** Rp(Ip) 330uA/180uA/80uA Tuning

7.20.5.102 CC Parameter Setting Register 2 (CCPSR2)

Address Offset: 72h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0h	**CC RD Resistor Tuning** Rd 5.1K Tuning

7.20.5.103 CC Parameter Setting Register 3 (CCPSR3)

Address Offset: 73h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
1-0	R/W	0h	**CC Tx Pre-driving Rise Time/Delay Tuning** The value of offset plus 0x3700 is for port A&B&C rise time tuning. The value of offset plus 0x3800 is for port B delay tuning. The value of offset plus 0x3B00 is for port C delay tuning.

7.20.5.104 CC Parameter Setting Register 4 (CCPSR4)

Address Offset: 74h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	0h	**CC Tx Pre-driving Fall Time/Delay Tuning** The value of offset plus 0x3700 is for port A&B&C fall time tuning. The value of offset plus 0x3800 is for port A delay tuning. The value of offset plus 0x3B00 is for is reserved.

7.20.5.105 CC Parameter Setting Register 5 (CCPSR5)

Address Offset: 75h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R/W	0h	**CC Tx Swing Tuning** PD Tx Swing 1.125V Tuning.

7.21 SPI Slave Controller (SPISC)

7.21.1 Overview

The SPI slave controller can handle large amounts of data bytes for various applications.

7.21.2 Features

- Supports SPI bus rate up to 24MHz if less than 256 bytes data
- Supports SPI dual mode
- Supports full-duplex mode
- Indepentdent FIFO for Tx/Rx channel, each with two 128-byte FIFOs

7.21.3 EC Interface Registers

The following table lists all of the SPI Slave Controller registers. The base address is **0x3A00**.

Table 7-38. EC View Register Map, SPISC

7 … 0	Offset
SPI Slave General Control Register (SPISGCR)	00h
Tx/Rx FIFO Access Register (TxRxFAR)	01h
Tx FIFO Control Register (TxFCR)	02h
SPI Slave General Control Register2 (SPISGCR2)	03h
Interrupt Mask Register (IMR)	04h
Interrupt Status Register (ISR)	05h
Tx FIFO Status Register (TxFSR)	06h
Rx FIFO Status Register (RxFSR)	07h
CPU Write Tx FIFO Data Byte0 Register (CPUWTxFDB0R)	08h
FIFO Control (FCR) / CPU Write Tx FIFO Data Byte1 Register (CPUWTxFDB1R)	09h
CPU Write Tx FIFO Data Byte2 Register (CPUWTxFDB2R)	0Ah
SPI Slave Response Data (SPISRDR) / CPU Write Tx FIFO Data Byte3 Register (CPUWTxFDB3R)	0Bh
Rx FIFO Readout Data Byte0 (RxFRDRB0)	0Ch
Rx FIFO Readout Data Byte1 (RxFRDRB1)	0Dh
Rx FIFO Readout Data Byte2 (RxFRDRB2)	0Eh
Rx FIFO Readout Data Byte3 (RxFRDRB3)	0Fh
Rx FIFO Count Monitor Byte0 (RxFCMB0)	14h
Rx FIFO Count Monitor Byte1 (RxFCMB1)	15h
Tx FIFO Count Monitor Byte0 (TxFCMB0)	16h
Tx FIFO Count Monitor Byte1 (TxFCMB1)	17h
FIFO Target Count Byte0 Register (FTCB0R)	18h
FIFO Target Count Byte1 Register (FTCB1R)	19h
Target Count Capture Byte0 (TCCB0)	1Ah
Target Count Capture Byte1 (TCCB1)	1Bh
Hardware Parsing Register1	1Ch
Hardware Parsing Register2	1Eh
eMMC Boot Mode Register (eMMCBMR)	21h
UART1 Pin Mux Register (UART1PMR)	23h
Capture Byte0 (CB0)	24h
Capture Byte1 (CB1)	25h
Rx Valid Length Interrupt Status Mask Register (RxVLISMR)	26h
Rx Valid Length Interrupt Status Register (RxVLISR)	27h

7.21.3.1 SPI Slave General Control Register (SPISGCR)

Address Offset: 00h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**Hardware Mode** 0: This mode is for software-based parsing flow. 1: This mode is for hardware-based parsing flow.
1	R/W	0b	**Dual Mode** 0: Single mode. 1: Dual mode is valid only when hardware mode is set, and only for SPI Slave Tx data (host read) direction.
0	R/W	0b	**SPI Slave Controller Enable (SPISCEN)** 0: The SPI slave controller is disabled. 1: The SPI slave controller is enabled.

7.21.3.2 Tx/Rx FIFO Access Register (TxRxFAR)

Address Offset: 01h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**CPU Rx FIFO2 Access (CPURxF2A)** When this bit is set, software can access the Rx FIFO2 and read out data from **{RxFRDRB3, RxFRDRB2, RxFRDRB1, RxFRDRB0}**.
3	R/W	0b	**CPU Rx FIFO1 Access (CPURxF1A)** When this bit is set, software can access the Rx FIFO1 and read out data from **{RxFRDRB3, RxFRDRB2, RxFRDRB1, RxFRDRB0}**.
2	-	-	**Reserved**
1	R/W	0b	**CPU Tx FIFO Access (CPUTFA)** When this bit is set, software can access Tx FIFO, and write data in Tx FIFO.
0	-	-	**Reserved**

7.21.3.3 Tx FIFO Control Register (TxFCR)

Address Offset: 02h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	W	0b	**Tx FIFO Count Monitor Reset (TxFCMR)** Set this bit to reset **{TxFCMB1, TxFCMB0}**.
1	W	0b	**Tx FIFO Reset (TxFR)** Set this bit to reset Tx FIFO.
0	W	0b	**Tx FIFO Switch (TxFS)** After writing data to Tx FIFO is finished, this bit will be to indicate the SPI slave controller.

7.21.3.4 SPI Slave General Control Register2 (SPISGCR2)

Address Offset: 03h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	1	**Rx FIFO End Access Count Reset (RxFEACR)** When this bit is set once **CPURxF1A** or **CPURxF2A** goes from 1 to 0, **RxFCMB0 and RxFCMB1** will reset to 0.
5	R/W	1	**Software Mode Rx FIFO Count Reset Enable (SMRxFCRE)** When this bit is set, **RxFCMB0 and RxFCMB1** will reset to 0 after reaching **{FTCB1R, FTCB0R}.**
4	R/W	1	**Rx FIFO2 Overwrite Control (RxF2OC)** When this bit is set Rx FIFO2 will not be overwrited once it's full (128 byte received).
3	R/W	1	**Rx FIFO1 Overwrite Control (RxF1OC)** When this bit is set Rx FIFO1 will not be overwrited once it's full (128 byte received).
2	R/W	1	**Rx FIFO Count Reset2 (RxFCR2)** When this bit is set and **RxFAR**=0, **RxFCMB0 and RxFCMB1** will reset after a dummy byte CS_N goes high.
1	R/W	0	**Rx FIFO Count Reset1 (RxFCR1)** When this bit is set, **RxFCMB0 and RxFCMB1** will reset after each CS_N goes high.
0	R/W	0	**Rx FIFO Auto Reset (RxFAR)** When this bit is set, Rx FIFO1/FIFO2, **RxFCMB0** and **RxFCMB1** will reset after each CS_N goes high.

7.21.3.5 Interrupt Mask Register (IMR)

Address Offset: 04h

Bit	R/W	Default	Description
7	R/W	1b	**Rx FIFO Full Interrupt Mask** 0: Rx FIFO full interrupt enabled. 1: Rx FIFO full interrupt masked.
6	R/W	1b	**Tx FIFO Empty Interrupt Mask** 0: Tx FIFO empty interrupt enabled. 1: Tx FIFO empty interrupt masked.
5	R/W	1b	**Rx Byte Reach Interrupt Mask** 0: Rx byte reach interrupt enabled. 1: Rx byte reach interrupt masked.
4	R/W	1b	**SPI Bus Busy Interrupt Mask** 0: SPI bus busy interrupt enabled. 1: SPI bus busy interrupt masked.
3	R/W	1b	**Command In Interrupt Mask** 0: Command in interrupt enabled. 1: Command in interrupt masked.
2	R/W	1b	**SPI End Detection Interrupt Mask** 0: SPI end detection interrupt enabled. 1: SPI end detection interrupt masked.
1	R/W	1b	**Tx Byte Reach Interrupt Mask** 0: Tx byte reach interrupt enabled.

Bit	R/W	Default	Description
			1: Tx byte reach interrupt masked.
0	R/W	1b	**Tx Empty Interrupt Mask** 0: Tx empty interrupt enabled. 1: Tx empty interrupt masked.

7.21.3.6 Interrupt Status Register (ISR)

Address Offset: 05h

Bit	R/W	Default	Description
7	R/WC	0b	**Rx FIFO Full Interrupt** When this bit is set, it indicates one of the Rx FIFO1 or Rx FIFO2 is full. Write one to clear this status.
6	R/WC	0b	**Tx FIFO Empty Interrupt** When this bit is set, it indicates one of the Tx FIFO1 or Tx FIFO2 is not full. Write one to clear this status.
5	R/WC	0b	**Rx Byte Reach Interrupt** When this bit is set, it indicates the Rx byte count is reached **{FTCB1R, FTCB0R}**. Write one to clear this status.
4	R	0b	**SPI Bus Busy Interrupt** When this bit is set, it indicates the SPI bus is busy.
3	R/WC	0b	**Command In Interrupt** When this bit is set, it indicates a command data is stored into Rx FIFO. Write one to clear this status. **Note:** Only valid in hardware mode
2	R/WC	0b	**SPI End Detection Interrupt** When this bit is set, it indicates the SPI bus end is detected. Write one to clear this status.
1	R/WC	0b	**Tx Byte Reach Interrupt** When this bit is set, it indicates the Tx byte count is reached **{FTCB1R, FTCB0R}**. Write one to clear this status.
0	R/WC	1b	**Tx Empty Interrupt** When this bit is set, it indicates Tx buffer **(SPISRDR)** is empty. Write data to **SPISRDR** to clear this status.

7.21.3.7 Tx FIFO Status Register (TxFSR)

Address Offset: 06h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4-3	R	0h	**Tx FIFO FSM (TxFFSM)** 2’d0: Tx FIFO initial state, no data in either Tx FIFO1 or Tx FIFO2 2’d1: The SPI slave controller will read data from Tx FIFO1. 2’d2: The SPI slave controller will read data from Tx FIFO2. 2’d3: Reserved
2	R	1b	**Tx FIFO2 Not Full Status (TxF2NFS)** 0: Tx FIFO2 is full. 1: Tx FIFO2 is not full
1	R	1b	**Tx FIFO1 Not Full Status (TxF1NFS)** 0: Tx FIFO1 is full.

Bit	R/W	Default	Description
			1: Tx FIFO1 is not full
0	R	1b	**Tx FIFO Available Status** 0: Tx FIFO is not available, which means **TxF1NFS=0** and **TxF2NFS=0**. 1: Tx FIFO is available, which means **TxF1NFS=1** or **TxF2NFS=1**.

7.21.3.8 Rx FIFO Status Register (RxFSR)

Address Offset: 07h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4-3	R	0h	**Rx FIFO FSM (RxFFSM)** 2'd0: The SPI slave controller writes data into Rx FIFO1. 2'd1: The SPI slave controller writes data into Rx FIFO2. 2'd2: After **CPURxF1A** is set, software wins over the ownership from hardware and then can read data from Rx FIFO1. 2'd3: After **CPURxF2A** is set, software wins over the ownership from hardware and then can read data from Rx FIFO2.
2	R	0b	**Rx FIFO2 Full Status (RxF2FS)** 0: Rx FIFO2 is not full. 1: Rx FIFO2 is full.
1	R	0b	**Rx FIFO1 Full Status (RxF1FS)** 0: Rx FIFO1 is not full. 1: Rx FIFO1 is full.
0	R	0b	**Rx FIFO Available Status** 0: Rx FIFO is not available, which means **RxF1FS=0** and **RxF2FS=0**. 1: Rx FIFO is available, which means **RxF1FS=1** or **RxF2FS=1**.

7.21.3.9 CPU Write Tx FIFO Data Byte0 Register (CPUWTxFDB0R)

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00h	**CPU Write Tx FIFO Data Byte0 (CPUWTFDB0)** When **CPUTFA** is active, this register represents **CPUWTFDB0**.

7.21.3.10 FIFO Control (FCR) / CPU Write Tx FIFO Data Byte1 Register (CPUWTxFDB1R)

Address Offset: 09h

Bit	R/W	Default	Description
7-4	R/W	0h	**Reserved**
3	R, W	0b	**Initial SPI Slave Read Tx FIFO (ISPISRTxF) or Tx FIFO Data Byte1 (CPUWTFDB1)** When **CPUTFA** is active, this register represents **CPUWTFDB1** bit[11]. However, when **CPUTFA** is not active, this bit represents **Initial SPI Slave Read Tx FIFO**.
2	R/W, W	0b	**SPI Slave Read Tx FIFO (SPISRTxF) or Tx FIFO Data Byte1 (CPUWTFDB1)** When **CPUTFA** is active, this register represents **CPUWTFDB1** bit[10]. However, when **CPUTFA** is not active, this bit represents **SPISRTxF**.

Bit	R/W	Default	Description
1	R/W, W	0b	**Rx FIFO Reset (RxFR) or CPU Write Tx FIFO Data Byte1 (CPUWTFDB1)** When **CPUTFA** is active, this register represents **CPUWTFDB1** bit[9]. However, when **CPUTFA** is not active, this bit represents **RxFR**.
0	R/W, W	0b	**Rx FIFO Count Monitor Reset (RxFCMR) or CPU Write Tx FIFO Data Byte1 (CPUWTFDB1)** When **CPUTFA** is active, this register represents **CPUWTFDB1** bit[8]. However, when **CPUTFA** is not active, this bit represents **RxFCMR**.

7.21.3.11 CPU Write Tx FIFO Data Byte2 Register (CPUWTxFDB2R)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	W	0h	**CPU Write Tx FIFO Data Byte2 (CPUWTFDB2)** When **CPUTFA** is active, this register represents **CPUWTFDB2**.

7.21.3.12 SPI Slave Response Data (SPISRDR) / CPU Write Tx FIFO Data Byte3 Register (CPUWTxFDB3R)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	W	00h	**SPI Slave Response Data (SPISRD) or CPU Write Tx FIFO Data Byte3 (CPUWTFDB3)** When **CPUTFA** is active, this register represents **CPUWTFDB3**. However, when **CPUTFA** is not active, this bit represents **SPISRD**.

7.21.3.13 Rx FIFO Readout Data Byte0 (RxFRDRB0)

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	R	00h	**Rx FIFO Data Out Byte0** This register indicates the SPI slave read data byte0 from FIFO when CPU reads this register.

7.21.3.14 Rx FIFO Readout Data Byte1 (RxFRDRB1)

Address Offset: 0Dh

Bit	R/W	Default	Description
7-0	R	00h	**Rx FIFO Data Out Byte1** This register indicates the SPI slave read data byte1 from FIFO when CPU reads this register.

7.21.3.15 Rx FIFO Readout Data Byte2 (RxFRDRB2)

Address Offset: 0Eh

Bit	R/W	Default	Description
7-0	R	00h	**Rx FIFO Data Out Byte2** This register indicates the SPI slave read data byte2 from FIFO when CPU reads this register.

7.21.3.16 Rx FIFO Readout Data Byte3 (RxFRDRB3)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	R	00h	**Rx FIFO Data Out Byte3** This register indicates the SPI slave read data byte3 from FIFO when CPU reads this register.

7.21.3.17 Rx FIFO Count Monitor Byte0 (RxFCMB0)

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R	00h	**Rx FIFO Count Monitor Byte0 (RxFCMB0)** These registers {FCMB1R, FCMB0R} indicate the current transfer byte number of the Rx FIFO.

7.21.3.18 Rx FIFO Count Monitor Byte1 (RxFCMB1)

Address Offset: 15h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R	0h	**Rx FIFO Count Monitor Byte1 (RxFCMB1)** These registers {FCMB1R, FCMB0R} indicate the current transfer byte number of the Rx FIFO.

7.21.3.19 Tx FIFO Count Monitor Byte0 (TxFCMB0)

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R	00h	**Tx FIFO Count Monitor Byte0 (TxFCMB0)** These registers {FCMB1R, FCMB0R} indicate the current transfer byte number of the Tx FIFO.

7.21.3.20 Tx FIFO Count Monitor Byte1 (TxFCMB1)

Address Offset: 17h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R	0h	**Tx FIFO Count Monitor Byte1 (TxFCMB1)** These registers {FCMB1R, FCMB0R} indicate the current transfer byte number of the Tx FIFO.

7.21.3.21 FIFO Target Count Byte0 Register (FTCB0R)

Address Offset: 18h

Bit	R/W	Default	Description
7-0	R/W	08h	**FIFO Target Count Byte0 Register (FTCB0R)** These registers {FTCB1R, FTCB0R} indicate the target transfer byte count of the FIFO to inform the CPU.

7.21.3.22 FIFO Target Count Byte1 Register (FTCB1R)

Address Offset: 19h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0h	**FIFO Target Count Byte1 Register (FTCB1R)** These registers {FTCB1R, FTCB0R} indicate the target transfer byte count of the FIFO to inform the CPU.

7.21.3.23 Target Count Capture Byte0 (TCCB0)

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R/W	06h	**Target Count Capture Byte0 (TCCB0)** Set **{TCCB1, TCCB0}** to readout **CB0** and **CB1**.

7.21.3.24 Target Count Capture Byte1 (TCCB1)

Address Offset: 1Bh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0	**Target Count Capture Byte1 (TCCB1)** Set **{TCCB1, TCCB0}** to readout **CB0** and **CB1**.

7.21.3.25 Hardware Parsing Register1 (HPR1)

Address Offset: 1Ch

Bit	R/W	Default	Description
7-0	R/W	11h	**Hardware Parsing Register1 (HPR1)** The SPI slave parses the SPI data. If the data is the same as that of the **HPR1**, the SPI slave will start to read Tx FIFO and then send out data after 3-bytes. Ex: [Read_Cmd] [Dummy] [Dummy] [Dummy] [Data] [Data] … **Note:** Only valid in hardware mode.

7.21.3.26 Hardware Parsing Register2 (HPR2)

Address Offset: 1Eh

Bit	R/W	Default	Description
7-0	R/W	13h	**Hardware Parsing Register2 (HPR2)** The SPI slave parses the SPI data. If the data is the same as that of the **HPR2**, Rx FIFO will not store it. Usually we set this register to prevent Rx FIFO from storing the master read SPI status byte. **Note:** Valid in both hardware mode and software mode.

7.21.3.27 eMMC Boot Mode Register (eMMCBMR)

Address Offset: 21h

Bit	R/W	Default	Description
7-2	R/W	-	**Reserved**
1	R/W	0	**eMMC Alternative Boot Mode (eMMCABM)** Set this bit to operate in eMMC Alternative Boot Mode.
0	R/W	0	**eMMC Boot Mode (eMMCBM)** Set this bit to operate in eMMC Boot Mode.

7.21.3.28 UART1 Pin Mux Register (UART1PMR)

Address Offset: 23h

Bit	R/W	Default	Description
7-1	R/W	00h	**Reserved**
0	R/W	0	**UART1 Pin Select (UART1PSEL)** Set this bit to switch UART1 from GPH1/GPH2 to GPH5/GPH6.

7.21.3.29 Capture Byte0 (CB0)

Address Offset: 24h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Capture Byte0 (CB0)** **{TCCB1, TCCB0}** result will be readout here.

7.21.3.30 Capture Byte1 (CB1)

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	00h	**Capture Byte1 (CB1)** **{TCCB1, TCCB0} + 12’d1** result will be readout here.

7.21.3.31 Rx Valid Length Interrupt Status Mask Register (RxVLISMR)

Address Offset: 26h

Bit	R/W	Default	Description
7-1	R/W	00h	**Reserved**
0	R/W	1	**Rx Valid Length Interrupt Mask** 0: Rx Valid Length interrupt enabled. 1: Rx Valid Length interrupt masked.

7.21.3.32 Rx Valid Length Interrupt Status Register (RxVLISR)

Address Offset: 27h

Bit	R/W	Default	Description
7-1	R/W	00h	**Reserved**
0	R/WC	0	**Rx Valid Length Interrupt** When this bit is set indicates that **{FTCB1R, FTCB0R} + {3'd0, CB1[0] CB0[7:0]}** reaches. Write one to clear this status.

7.22 Debugger (DBGR)

7.22.1 Overview

This DBGR module provides the ability to access the instruction SRAM, data SRAM and EC side peripheral modules. More than that, the DBGR interface can be converted to N801's JTAG debug interface as well through the JTAG bridge to achive CPU core related debug such as setting break-point, setting watch-point, and stepping exeute, etc. It is called In-system Debugging (ISD). The DBGR module also provides a path to download or program the embedded flash, called In-system Programming (ISP).

DBGR can be performed by either of the two interfaces below.

- DBGR/EPP
- DBGR/SMB

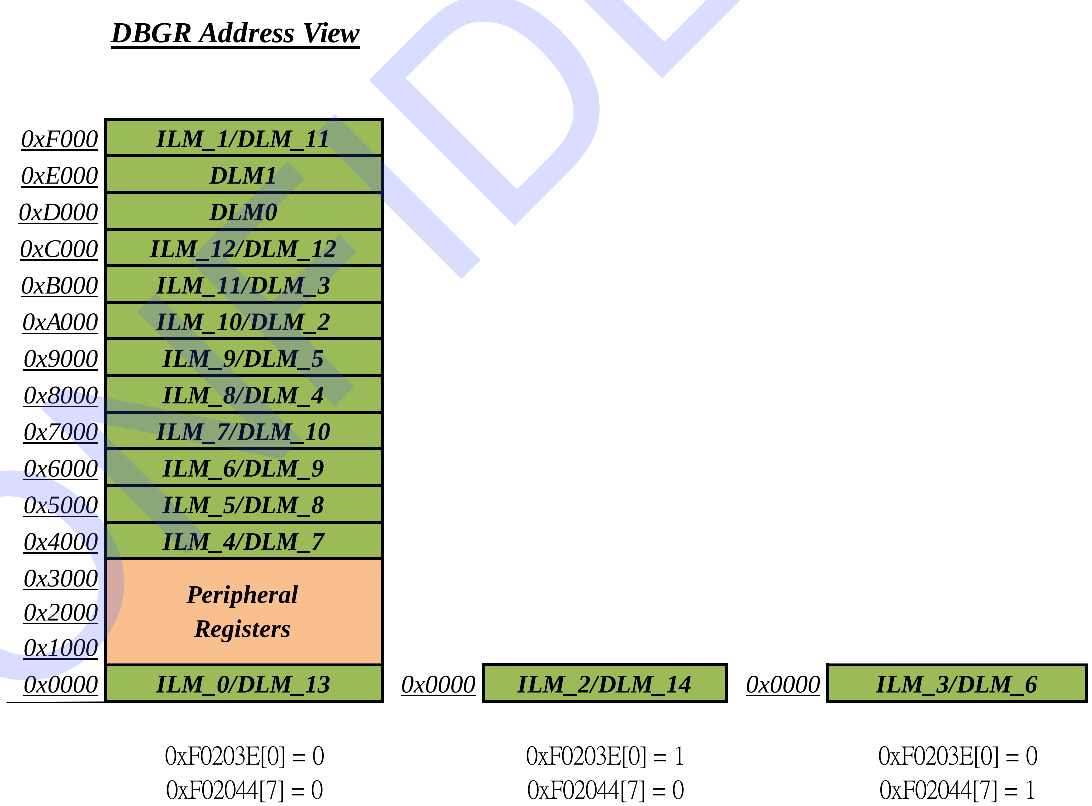
Both ISP and ISD can be performed by either DBGR/EPP or DBGR/SMB.

7.22.2 Features

- ISP and ISD
- EC Memory Snoop (ECMS = I2EC + D2EC)
- Convert to N801's JTAG interface

7.22.3 DBGR Memory Map

Figure 7-32. DBGR Memory Map



7.22.4 Functional Description

7.22.4.1 DBGR/EPP

Refer to section 7.23 Parallel Port (PP).
It can be disabled by OVRPPK bit in the KSICTRLR register.
Hot-plug is available.

7.22.4.2 DBGR/SMB

Refer to section 7.8.3.2 SMBus Slave Interface.
There is another dedicated SMBus slave for this function.
It can be disabled by OVRSMDBG bit in SLVISELR register.
Hot-plug is available, but can not exit DBGR mode after being detected.

7.22.4.3 In-system Programming Operation

It provides flash read and program function.

7.22.4.4 In-system Debugging Operation

It's performed by the utility provided by ITE and contains two features below.
1. D2EC described in section 7.22.4.5 EC Memory Snoop (ECMS).
2. Breakpoints, stepping, etc. and reset functions supported.

7.22.4.5 EC Memory Snoop (ECMS)

ECMS is available through one of the two ways:

1. I2EC (I-bus to EC Memory)
Local machine snoops EC memory through the LPC I/O cycle.

Here are two registers to provide the way to perform the I2EC access.

- I2EC_ADDR_H/I2EC_ADDR_L/I2EC_DATA register, defined in section 6.3.1.10 Depth 2 I/O Address (D2ADR) on page 78.
- I2EC_XADDR_H/ I2EC_XADDR_L/I2EC_XDATA register, with programmable address and defined in section 7.15.4.19 Port I2EC High-Byte Register (PI2ECH) on page 434.

Figure 7-33. I2EC through 2Eh/2Fh I/O Port Operation Flow

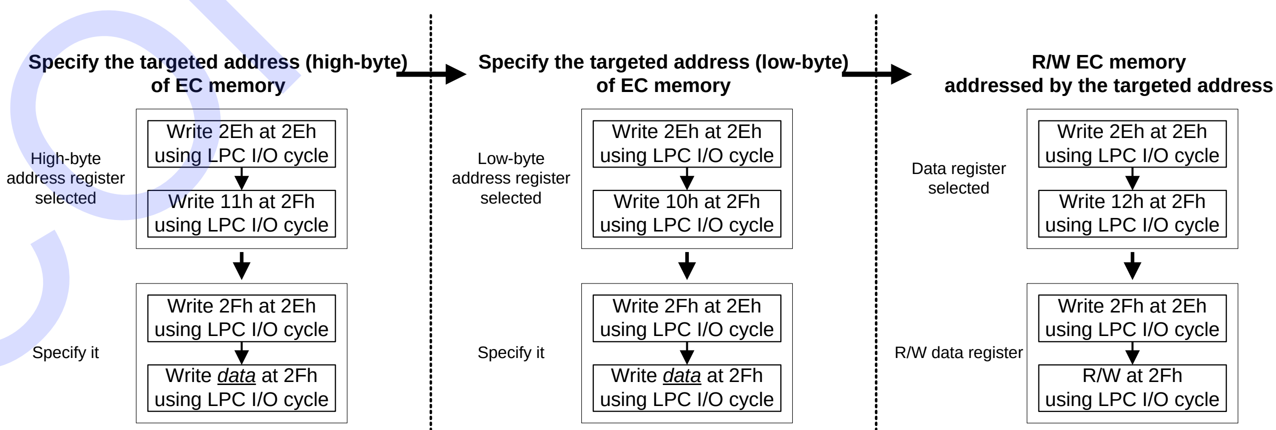
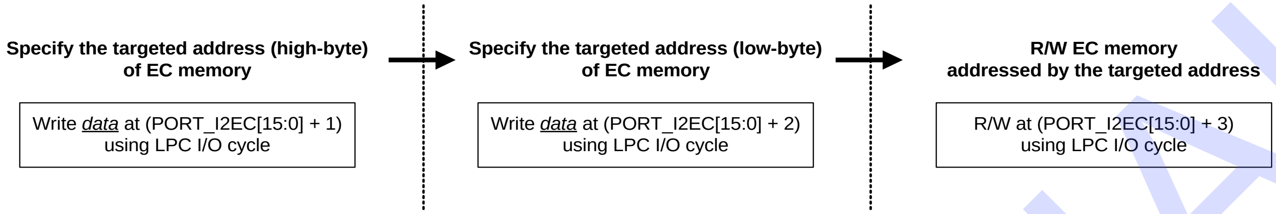


Figure 7-34. I2EC through Dedicated I/O Port Operation Flow



2. D2EC (DBGR to EC Memory)
Remote machine snoops EC memory through EPP cycle.

I2EC/D2EC utility is provided by ITE.
I2EC is not enabled until its controlled register in the EC side register is written.
I2EC can be configured as read-only for all targets.
I2EC and D2EC can work at the same time.
I2EC/D2EC will not affect any register content of read-clear registers.

The writing action of I2EC/D2EC to F/F based register is okay; however, the result of writing to non-F/F based register is not expected. Such registers may be write-clear, or writing to start internal state-machine, etc.
If D2EC is enabled, PLL will not be powered down in the Sleep mode.

Table 7-39. I2EC/D2EC Accessible Target

	I2EC	**D2EC**
uC SFR (except ACC/IE reg.)	R	R
uC SFR – ACC/IE reg.	R	R/W
uC External Memory (except DMM)	R/W controlled by I2ECCTRL field in SPCTRL1 reg.	R/W
uC External Memory – DMM	Not Accessible	R

Note: DMM denotes double-mapping module.

7.22.4.6 Other Debug Topics

Here are some debug features not covered in this DBGR section but may be useful for users.
1. Section 6.2.4 Debug Port Function on page 71.
2. Section 6.2.4 Debug Port Function on page 71. Hardware output signals to latch port 80h data on LAD[3:0].
3. Section 7.16.4 P80L on page 458.

7.23 Parallel Port (PP)

7.23.1 Overview

IT81202 supports IEEE 1284 parallel port interface to allow in-system programming (ISP) or in-system debugging (ISD) regardless of running firmware code.

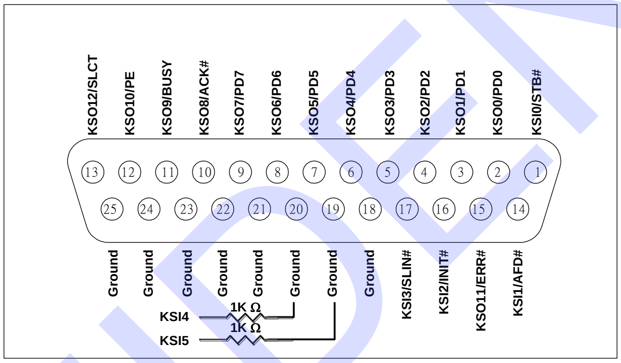
7.23.2 Features

- ISP/ISD via parallel port interface on existed KBS connector
- Fast flash programming with software provided by ITE
- Programming software supports EPP/SPP mode

7.23.3 Functional Description

7.23.3.1 KBS Connection with Parallel Port Connector

Figure 7-35. Parallel Port Female 25-Pin Connector



If Parallel Port cable is detected by internal hardware strap, the following functions will be disabled.
1. ROM Address Match Interrupt
2. Internal/External Watchdog

The DBGR/EPP debug mode takes place when VSTBY is supplied (other types of power are don't-care) and both EC chip and the flash are soldered on PCB. Parallel port interface occupies pins with the same interface as that of KBS using the existing KBS connector.

7.24 JTAG Bridge (JTAG)

7.24.1 Overview

The JTAG bridge module connects the JTAG interface and DBGR controller for CPU debug. .

7.24.2 Features

- Supports 5-wire JTAG standard interface.
- Supports JTAG clock up to 48MHz

7.24.3 Register Description

The following table lists all of the Interrupt Controller registers. Each register can be accessed by byte access only. The base address is **0x2DC0**.

Table 7-40. EC View Register Map, JTAG Bridge

Register Name	R/W	Address	Default
Control Register	R/W	0x00	81h
Instruction Register	R/W	0x01	00h
Transmit Data Register	R/W	0x03	00h
Receive Data Register	R	0x04	00h
Debug Interrupt Maximum Interval Register	R/W	0x06	90h
BRAM FIFO Status Register	R	0x08	00h

7.24.3.1 Control Register

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	1	**dbgi_n Control** When random dbgi_n is disabled, users can set this bit to control dbgi_n 1: Debug interrupt de-asserted. 0: Debug interrupt asserted.
6	R/W	0	**Random dbgi_n Enable** When this bit is set, the dbgi_n will be asserted automatically.
5-1	-	0	**Reserved**
0	R/W	1	**TRST Control (Active Low)** 1: Trst de-asserted. 0: Trst asserted.

7.24.3.2 Instruction Register

Address Offset: 01h

Bit	R/W	Default	Description
7-4	-	0	**Reserved**
3-0	R/W	0h	**JTAG Instruction setting** The main instruction value and related shift-DR length are as the following: BYPASS: 4’b1111. 64-bit length.

Bit	R/W	Default	Description
			IDCODE: 4'b1001. 32-bit length EXECUTE: 4'b1000. 0-bit length GET_DBG_EVENT: 4'b0111. 5-bit length FAST_ACCESS_MEM: 4'b0110. 33-bit length ACCESS_MISC_REG: 4'b0101. 38-bit length ACCESS_MEM_B: 4'b1011. 42-bit length ACCESS_MEM_H: 4'b1010. 49-bit length ACCESS_MEM_W: 4'b0100. 64-bit length ACCSS_DTR: 4'b0011. 34-bit length ACCSS_EDM_SR: 4'b0010. 41-bit length ACCSS_DIM: 4'b0001. 34-bit length BSCAN: 4'b1110.

7.24.3.3 Transmit Data Register

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	00h	**Transmit Data Register** Set the transmit data according to different instructions.

7.24.3.4 Receice Data Register

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R	00h	**Receive Data Register** The register receives data from CPU TDO signal.

7.24.3.5 Debug Interrupt Maximum Interval Register

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	90h	**Debug Interrupt Maximum Interval** When random dbgi_n is enabled, the value is set for interrupt maximum interval.

7.24.3.6 BRAM FIFO Status Register

Address Offset: 08h

Bit	R/W	Default	Description
7	R	0b	**FIFO Data Available** 0: FIFO is empty. 1: Data is available.
6	R	-	**FIFO Full** 0: FIFO is not full. 1: FIFO is full.
5-0	R	-	**FIFO Data Count** Theses bits indicate the number of data left in FIFO.

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8. Register List

The base addresses are 0x3680 for channel D.

The base address for USBPD Port1 is 3700h.

7.20 USBPD Controller 492

The base address for USBPD Port2 is 3800h.

9. DC Characteristics

Operating Conditions

VSTBY………….. .... 3.3V±0.15V
VFSPI(3.3V)…………............................. 3.3V±0.15V
VFSPI(1.8V)…………............................. 1.8V±0.09V
VCC(3.3V)………….................................. 3.3V±0.15V
VCC(1.8V)………….................................. 1.8V±0.09V
AVCC………….. .... 3.3V±0.05V
VBAT……….. 2.3V to 3.3V
Operating Temperature (Ta) …………..-25°C to +85°C

Absolute Maximum Ratings

Applied Voltage of VFSPI(1.8V), VCC(1.8V) …………..
.... -0.3V to +2.1V
Applied Voltage of VSTBY, VFSPI(3.3V), VCC(3.3V),
AVCC ….. .... -0.3V to +3.6V
Input Voltage of 1.8V Interface.... -0.3V to VSUP+0.3V
Input Voltage of 3.3V Interface.... -0.3V to VSUP+0.3V
Input Voltage of 5.0V Interface.............. -0.3V to +5.8V
Input Voltage of 1.8V/3.3V ....
Optional Interface .... -0.3V to +3.6V
Storage Temperature ....-40°C to +125°C

Note: VSUP is VCC, VSTBY, VFSPI or AVCC.

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Conditions
3.3V CMOS Interface					
V_{IL}	Input Low Voltage	—	—	0.8V	—
V_{IH}	Input High Voltage	2.0V	—	—	—
V_{IH}	Input High Voltage (5V tolerant pad)	2.0V	—	—	—
V_{OL}	Output Low Voltage	—	—	0.4V	—
V_{OH}	Output High Voltage	2.4V	—	—	—
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	0.8V	1.1V	—	—
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage	—	1.6V	2.0V	—
I_{IL}	Input leakage Current	-10µA	±1µA	10µA	No pull-up or pull-down
I_{OZ}	Tri-state Leakage Current	-10µA	±1µA	10µA	No pull-up or pull-down
R_{pu}	Input Pull-Up Resistance	40KΩ	75KΩ	190KΩ	V_I= 0V
R_{pd}	Input Pull-Down resistance	40KΩ	75KΩ	190KΩ	V_I= VSUP
Cin	Input Capacitance	—	2.8pF	—	—
C_L	Load Capacitance	—	—	10pF	For FSPI signals only
Cout	Output Capacitance	2.7pF	—	4.9pF	—
Cbld	Bi-directional Buffer	2.7pF	—	4.9pF	—

Note: VSUP is VCC (3.3V), VSTBY, VFSPI (3.3V) or AVCC.

Symbol	Parameter	Min.	Typ.	Max.	Conditions
1.8V CMOS Interface					
V_{IL}	Input Low Voltage	—	—	0.25*VSUP	—
V_{IH}	Input High Voltage	0.75*VSUP	—	—	—
V_{IH}	Input High Voltage (5V tolerant pad)	0.75*VSUP	—	—	—
V_{OL}	Output Low Voltage	—	—	0.4V	—
V_{OH}	Output High Voltage	0.75*VSUP	—	—	—
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	0.25*VSUP	—	—	—
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage	—	—	0.75*VSUP	—
I_{IL}	Input Leakage Current	-10µA	±1µA	10µA	No pull-up or pull-down
I_{OZ}	Tri-state Leakage Current	-10µA	±1µA	10µA	No pull-up or pull-down
R_{pu}	Input Pull-Up Resistance	80KΩ	200KΩ	510KΩ	V_I= 0V
R_{pd}	Input Pull-Down resistance	80KΩ	200KΩ	510KΩ	V_I= VSUP
Cin	Input Capacitance	—	2.8pF	—	—
C_L	Load Capacitance	—	—	10pF	For FSPI signals only
Cout	Output Capacitance	2.7pF	—	4.9pF	—
Cbld	Bi-directional Buffer	2.7pF	—	4.9pF	—

Note: VSUP is VCC (1.8V) or VFSPI (1.8V).

Table 9-1. Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Conditions
3.3V CMOS Interface					
I_{SLEEP1}	VSTBY supply current if Crystal-Free	—	TBD µA	—	Internal pull is disabled. VIL = GND VIH = VSTBY No load
I_{BAT}	VBAT supply current	—	TBD µA	TBD µA	VSTBY and VCC are not supplied.

10. AC Characteristics

Figure 10-1. VSTBY Power-on Reset Timing

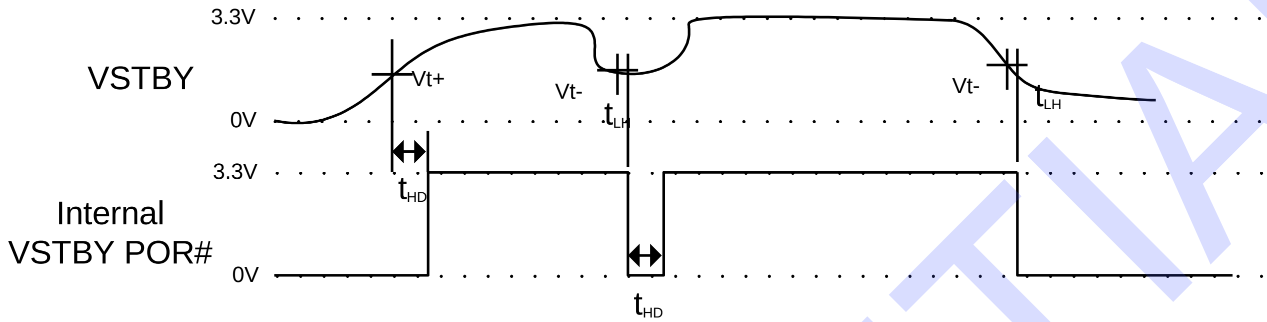


Table 10-1. VSTBY Power-on Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vt+	Level detection positive going threshold voltage	—	2.6	—	V
Vt-	Level detection negative going threshold voltage	—	(Vt+)-0.2	—	V
t_{HD}	Internal VSTBY POR going high delay	—	500	—	µs
t_{LH}	Minimum hold time after VSTBY < Vt- and before internal VSTBY POR going low	—	10	—	µs

Figure 10-2. Reset Timing

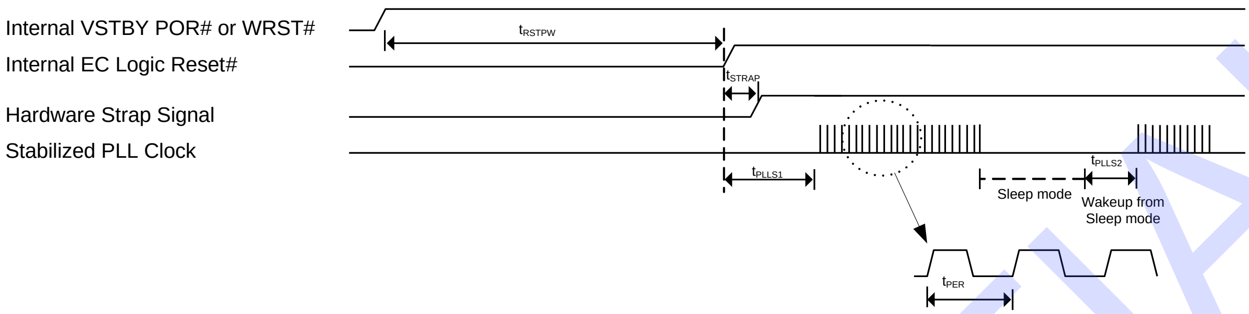


Table 10-2. Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RSTPW}	Internal EC logic reset after VSTBY POR or WRST#	—	1650	—	Tick (by 32.768 kHz)
t_{STRAP}	Strap sampling time	0	—	—	ns
t_{PLLS1}	PLL stabilization time hardware	—	5	—	ms
t_{PLLS2}	PLL stabilization time after waking up from Sleep mode	—	5	—	ms
t_{PER}	PLL clock period	—	$1/_{FreqPLL}$	—	ns
FreqPLL	PLL clock frequency if PLLFREQ = 0100b	—	48	—	MHz
FreqFND	Embedded flash clock frequency if CLK_FND_DIV_SEL = 010b	—	FreqPLL/3	—	MHz
FreqEC	EC clock frequency if CLK_EC_DIV_SEL = 0001b	—	FreqFND/2	—	MHz
E_{cf2}	"Crystal-Free": Center frequency of FreqPLL/FreqEC Temperature: -25 ~ 85℃	—	—	±2.3	%

Figure 10-3. Warm Reset Timing

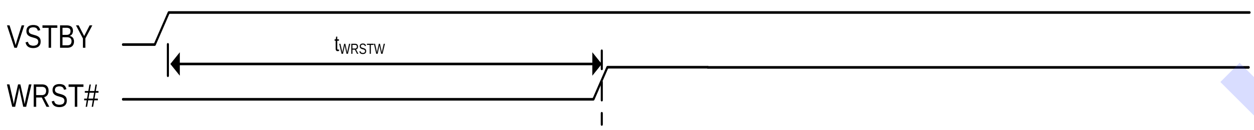


Table 10-3. Warm Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WRSTW}	Warm reset width	10	—	—	µs

Figure 10-4. Wakeup from Doze Mode Timing

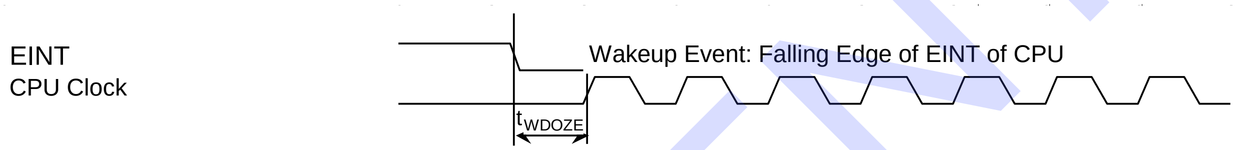


Table 10-4. Wakeup from Doze Mode AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WDOZE}	Doze wakeup time from falling edge of EINT to rising edge of first CPU clock.	—	—	2 / (EC Clock Freq)	—

Figure 10-5. Wake Up from Sleep Mode Timing

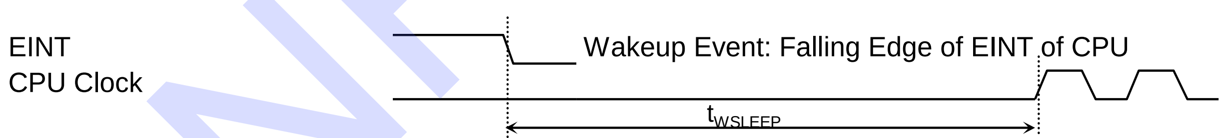


Table 10-5. Wake Up from Sleep Mode AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WSLEEP}	Sleep wakeup time from falling edge of EINT to rising edge of first CPU clock.	—	5	—	ms

Figure 10-6. Asynchronous External Wakeup/Interrupt Source Edge Detected Timing

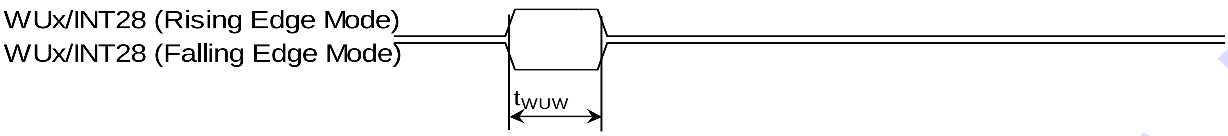


Table 10-6. Asynchronous External Wakeup/Interrupt Source Edge Detected AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WUW}	Wakeup source pulse width	—	1	—	ns

Figure 10-7. LPC and SERIRQ Timing

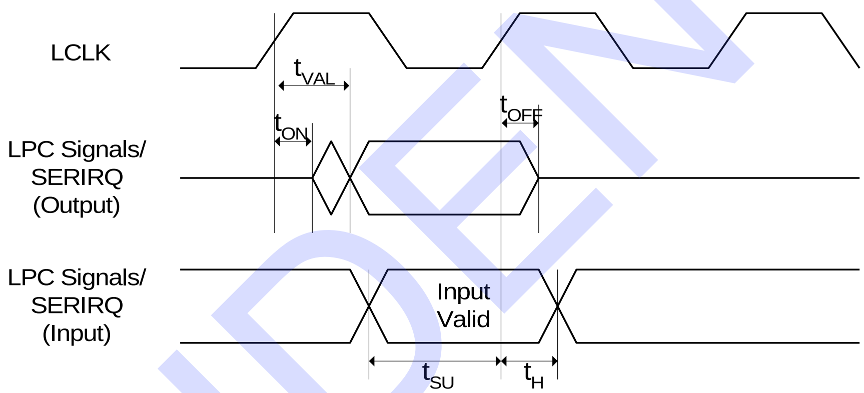
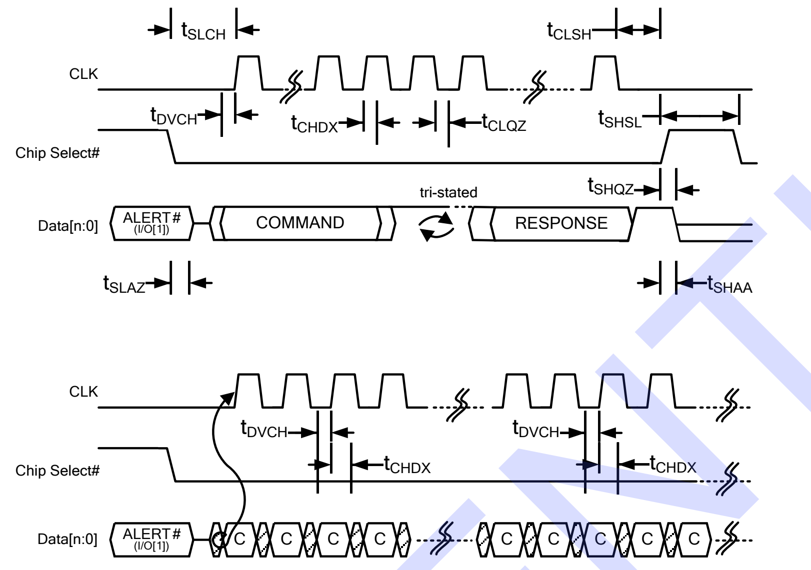


Table 10-7. LPC and SERIRQ AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ON}	Float to active delay	3	—	—	ns
t_{VAL}	Output valid delay	—	—	12	ns
t_{OFF}	Active to float delay	—	—	20	ns
t_{SU}	Input setup time	7	—	—	ns
t_H	Input hold time	0	—	—	ns

Figure 10-8. eSPI Timing

Input Timing Diagram



Output Timing Diagram

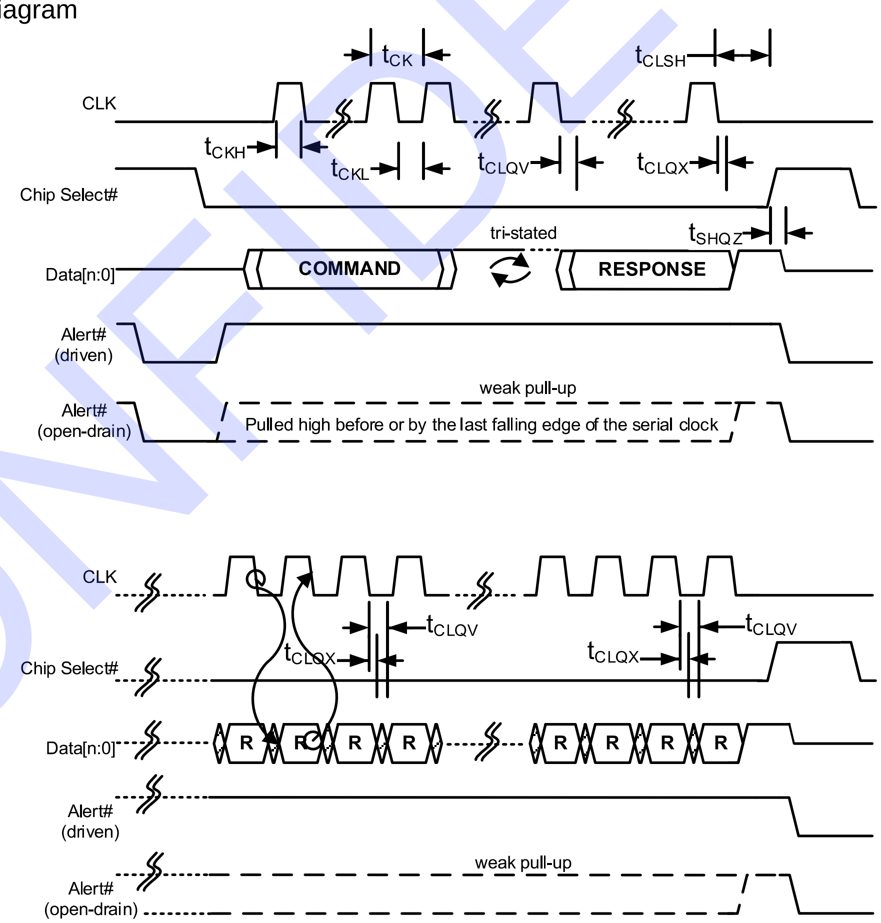


Table 10-8. eSPI AC Table

Symbol	Parameter
t_{CK}	Clock Period
t_{CKH}	Clock High Time
t_{CKL}	Clock Low Time
t_{SLCH}	Chip Select# Setup Time
t_{CLSH}	Chip Select# Hold Time
t_{SHSL}	Chip Select# Deassertion Time
t_{DVCH}	Data In Setup Time
t_{CHDX}	Data In Hold Time
t_{CLQZ}	Output Disable Time during Turn-Around
t_{CLQV}	Output Data Valid Time
t_{CLQX}	Output Data Hold Time
t_{SHQZ}	Output Disable Time after Chip Select# Deassertion
t_{SLAZ}	Chip Select# Assertion to I/O[1] Tri-stated
t_{SHAA}	Chip Select# Deassertion to I/O[1] Assertion
t_{INIT}	eSPI Reset# Deassertion to First Transaction (GET_CONFIGURATION)
$t_{INIT-FREQ}$	Initial Bus Frequency upon eSPI Reset# Deassertion

Table 10-9. eSPI AC Table 2

Symbol	20MHz		25MHz		33MHz		50MHz		66MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CK}	50	—	40	—	30	—	20	—	15	—	ns
t_{CKH}	0.4	—	0.4	—	0.4	—	0.4	—	0.4	—	t_{CK}
t_{CKL}	0.4	—	0.4	—	0.4	—	0.4	—	0.4	—	t_{CK}
t_{SLCH}	75	—	60	—	45	—	30	—	22	—	ns
t_{CLSH}	50	—	40	—	30	—	20	—	15	—	ns
t_{SHSL}	50	—	40	—	30	—	20	—	15	—	ns
t_{DVCH}	12	—	10	—	7	—	5	—	3	—	ns
t_{CHDX}	12	—	10	—	7	—	5	—	3	—	ns
t_{CLQZ}	—	15	—	12	—	9	—	8	—	6	ns
t_{CLQV}	—	20	—	15	—	10	—	8	—	6	ns
t_{CLQX}	2	—	2	—	2	—	2	—	2	—	ns
t_{SHQZ}	—	15	—	12	—	9	—	8	—	6	ns
t_{SLAZ}	—	15	—	12	—	9	—	8	—	6	ns
t_{SHAA}	15	—	12	—	9	—	8	—	6	—	ns
t_{INIT}	1	—	1	—	1	—	1	—	1	—	ns
$t_{INIT\text{-}FREQ}$	—	20	—	20	—	20	—	20	—	20	MHz

Note: Load capacitance CL = 10pF.

Figure 10-9. SWUC Wake Up Timing

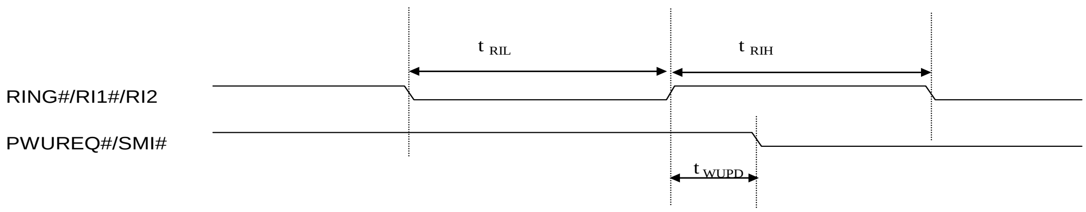


Table 10-10. SWUC Wake Up AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RIL}	RING#, RI1# , RI2# low time	10	—	—	ns
t_{RIh}	RING#, RI1# , RI2# high time	10	—	—	ns
t_{WUPD}	Wake up propagation delay time	—	20	—	ns

Figure 10-10. PWM Output Timing

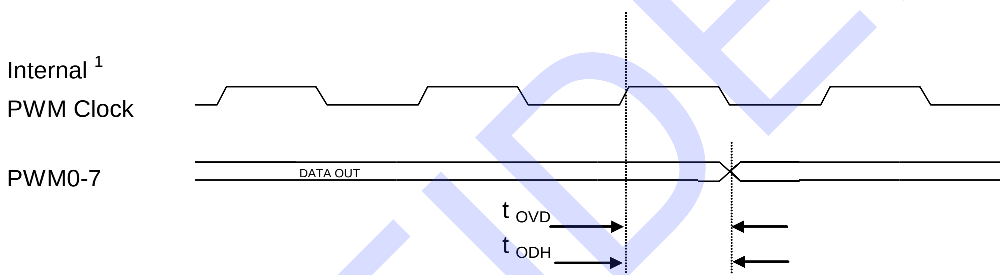


Table 10-11. PWM Output AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{OVD}	PWM output valid delay time	—	—	0.5	T^{NOTE1}
t_{ODH}	PWM output hold time	0	—	—	ns

Note 1: T is one time unit and its length is equal to the EC clock period X C0CPRS +1 (ns) for CH0~3, or X C4CPRS +1 (ns) for CH4~7.

Figure 10-11. Serial Flash (FSPI) Cycle Timing

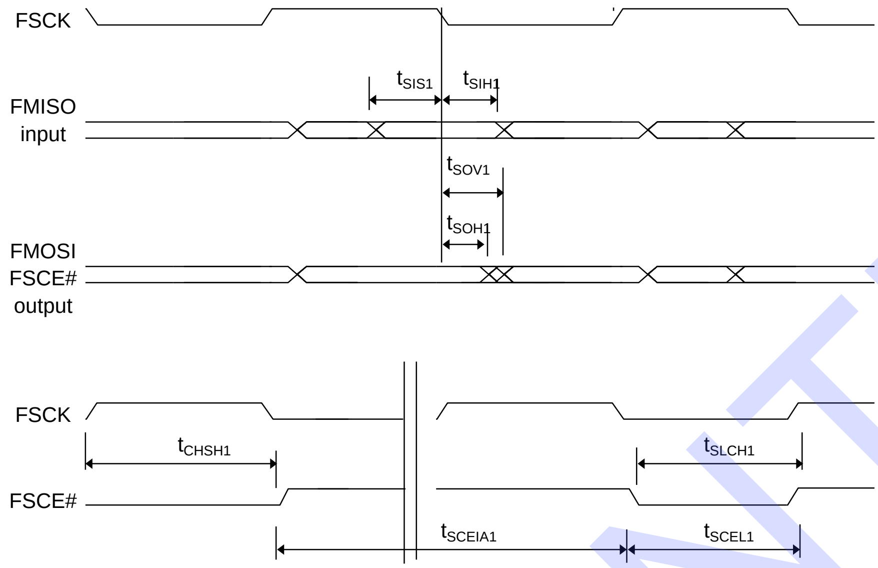


Table 10-12. Serial Flash (FSPI) Cycle AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCK}	FSCK period	—	62.5	—	ns
t_{CLH} t_{CLL}	FSCK high time NOTE1 FSCK low time NOTE1	25 Note2	—	—	ns
t_{SIS1}	Input setup time	3	—	—	ns
t_{SIH1}	Input hold time	0	—	—	ns
t_{SOV1}	Clock low to output valid	—	—	5	ns
t_{SOH1}	Output hold time	0	—	—	ns
t_{SCEL1}	FSCE# Active time	28	—	—	ns
t_{SCEIA1}	FSCE# high time	(SCEMINHW + 1) * t_{SCK}	—	—	ns
t_{SLCH1}	FSCE# Active Setup Time relative to FSCK rising edge	28	—	—	ns
t_{CHSH1}	FSCE# Active Hold Time relative to FSCK rising	28	—	—	ns

Note 1: Measurement point for low time and high time is taken at VSTBY*0.5.
Note 2: Characterized only.

Figure 10-12. PMC SMI#/SCI# Timing

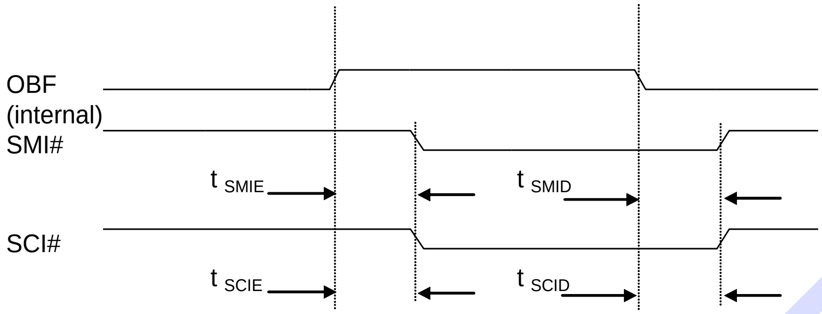


Table 10-13. PMC SMI#/SCI# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SMIE}	OBF asserted to SMI# asserted time	—	10	—	ns
t_{SMID}	OBF de-asserted to SMI# de-asserted time	—	5	—	ns
t_{SCIE}	OBF asserted to SCI# asserted time	—	10	—	ns
t_{SCID}	OBF de-asserted to SCI# de-asserted time	—	5	—	ns

Figure 10-13. PMC IBF/SCI# Timing

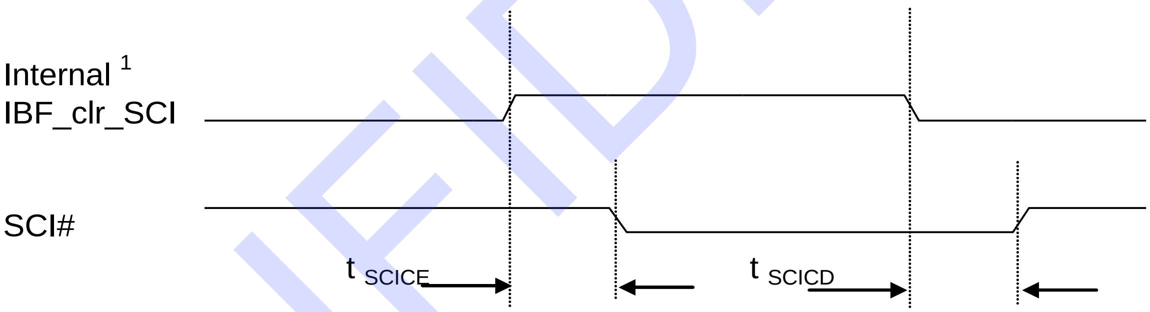


Table 10-14. PMC IBF/SCI# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCICE}	IBF_clr_SCI# asserted to SCI# asserted time	—	70	—	ns
t_{SCICD}	IBF_clr_SCI# de-asserted to SCI# de-asserted time	—	40	—	ns

Note 1: IBF_clr_SCI# means the invert signal of IBF, IBF_clr_SCI# set to one when EC read PMDI or PMDISCI.

Figure 10-14. SMBus Timing

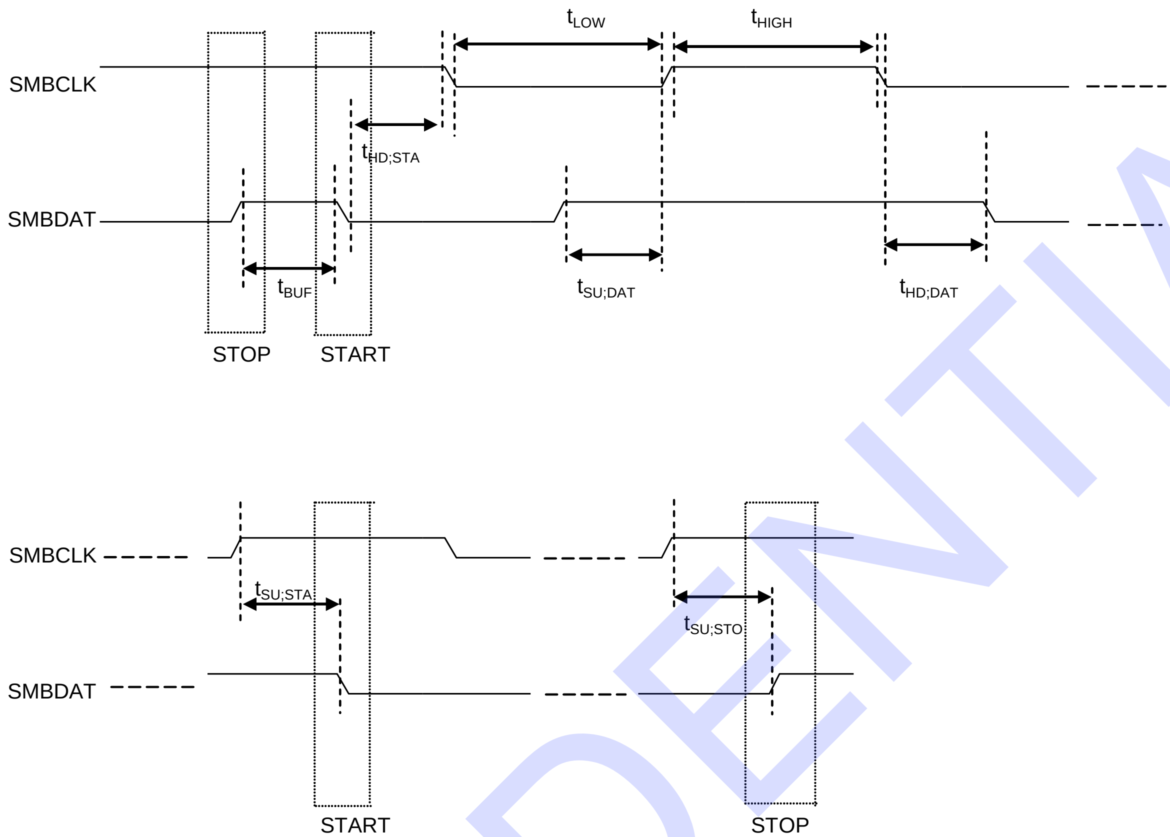


Table 10-15. SMBus AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{BUF}	Bus free time between Stop and Start condition	4.7	—	—	µs
$t_{HD;STA}$	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	4.0	—	—	µs
t_{LOW}	Clock low period	4.7	—	—	µs
t_{HIGH}	Clock high period	4.0	—	50	µs
$t_{SU;DAT}$	Data setup time	250	—	—	ns
$t_{HD;DAT}$	Data hold time	300	—	—	ns
$t_{SU;STA}$	Repeated Start condition setup time	4.7	—	—	µs
$t_{SU;STO}$	Stop condition setup time	4.0	—	—	µs

Figure 10-15. Serial Peripheral Interface (SSPI) Timing

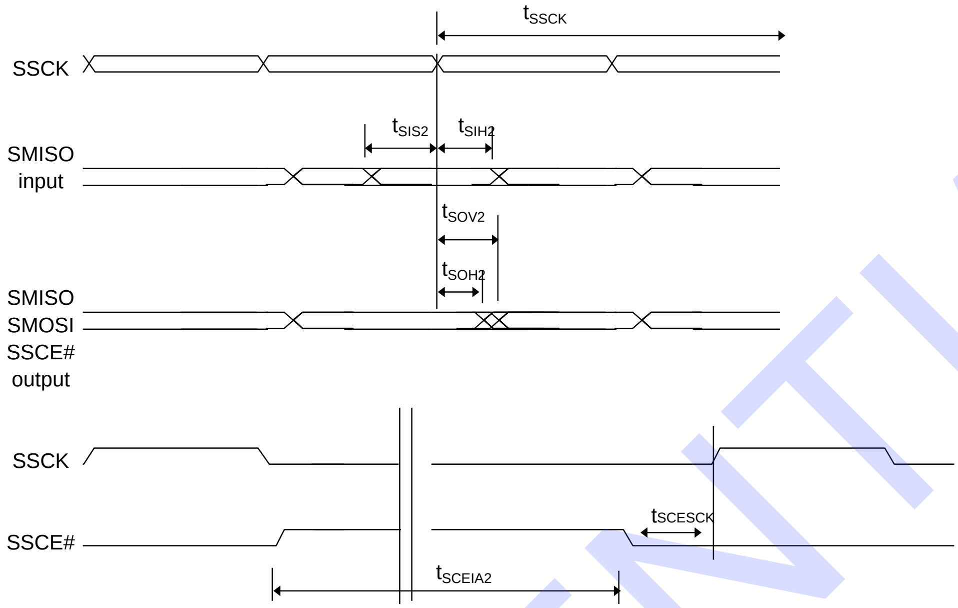


Table 10-16. Serial Peripheral Interface (SSPI) AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SSCK}	SSCK period	2/ FreqEC	—	16/ FreqEC	ns
t_{SIS2}	Input setup time	5	—	—	ns
t_{SIH2}	Input hold time	5	—	—	ns
t_{SOV2}	Clock edge to output valid	—	—	5	ns
t_{SOH2}	Output hold time	0	—	—	ns
t_{SCEIA2}	SSCE# inactive time	1/ FreqEC	—	—	ns
$t_{SCESSCK}$	From SSCE# active edge to first SSCK active edge	—	2/ FreqEC	—	ns

Figure 10-16. Serial Port (UART) Timing

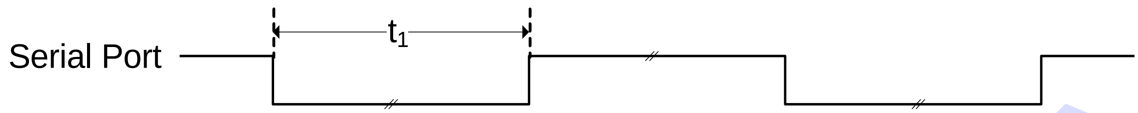


Table 10-17. Serial Port (UART) AC Table

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_1	Single bit time in UART	Transmitter	t_{BTN} – Tclk Note1	t_{BTN} + Tclk Note1	ns
		Receiver	t_{BTN} – 2%	t_{BTN} + 2%	ns

Note 1: tBTN is the nominal bit time in Serial Port (UART). It is determined by setting the Baud Rate Divisor registers. Tclk equals to 1/ FreqEC.Tclk equals to 1/ FreqEC.

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11. Analog Device Characteristics

Table 11-1. ADC Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Resolution	—	—	10	—	Bit
Integral Non-linearity Error (INL)	—	—	—	±4	LSB
Differential Non-linearity Error (DNL)	—	—	—	±4	LSB
Offset Error	—	—	—	±4	LSB
Gain Error	—	—	—	±4	LSB
External Input Accuracy	—	—	—	±4	LSB
ADC Input Voltage Range	—	0	—	AVCC/1.1 or AVCC	V
ADC Input Leakage Current	ADC0-x: 0 ≦ Vin ≦ AVCC	—	±1	—	μA
ADC Input Resistance	—	4	—	—	MΩ
ADC Input Capacitance	—	—	—	8	pF
ADC Clock Frequency	—	—	0.5	—	MHz
Voltage Conversion Time	—	—	—	100	us

Note 1: The voltage reference is AVCC/1.1 or AVCC.
Note 2: All calculated above are only within 0.25V ~ (AVCC - 0.15V) if the corresponding bit in ADCIVMFSCS1 or ADCIVMFSCS2 is set to 1b.
Note 3: All calculated above are only within 0.25V ~ 2.85V if the corresponding bit in ADCIVMFSCS1 or ADCIVMFSCS2 is set to 0b.
Note 4: After calibration is performed, INL is the difference between the actual transition curve and the end-point line.

Table 11-2. USB PD Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Unit
$I_{H\_CC\_USB}$	Source current through each C_CC pin when in a disconnected state and configured as a DFP advertising default USB current to a peripheral device.	—	73.6	80	86.4	μA
$I_{H\_CC\_1P5}$	Source current through each C_CC pin when configured as a DFP advertising 1.5A to a UFP.	—	165.6	180	194.4	μA
$I_{H\_CC\_3P0}$	Source current through each C_CC pin when in a disconnected state and configured as a DFP advertising 3.0A to a UFP.	VIN_3V3 ≧ 3.135V, V_{CC}＜2.6V	303.6	330	356.4	μA
$V_{D\_CCH\_USB}$	Voltage threshold for detecting a DFP attach when configured as a UFP and the DFP is advertising default USB current source capability.	—	0.15	0.2	0.25	V
$V_{D\_CCH\_1P5}$	Voltage threshold for detecting a DFP advertising 1.5A source capability when configured as a UFP.	—	0.61	0.66	0.7	V

Parameter		Conditions	Min.	Typ.	Max.	Unit
$V_{D\_CCH\_3P0}$	Voltage threshold for detecting a DFP advertising 3A source capability when configured as a UFP.	—	1.16	1.23	1.31	V
$V_{H\_CCD\_USB}$	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising default USB current source capability.	IH_CC=IH_CC_USB	1.5	1.55	1.65	V
$V_{H\_CCD\_1P5}$	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising 1.5A source capability.	IH_CC=IH_CC_1P5	1.5	1.55	1.65	V
$V_{H\_CCD\_3P0}$	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising 3.0A source capability.	IH_CC=IH_CC_3P0 VIN_3V3≧3.135V	2.45	2.55	2.6	V
$V_{H\_CCA\_USB}$	Voltage threshold for detecting and active cable attach when configured as a DFP and advertising default USB current capability.	—	0.15	0.2	0.25	V
$V_{H\_CCA\_1P5}$	Voltage threshold for detecting active cables attach when configured as a DFP and advertising 1.5A capability.	—	0.35	0.4	0.45	V
$V_{H\_CCA\_3P0}$	Voltage threshold for detecting active cables attach when configured as a DFP and advertising 3A capability.	—	0.76	0.8	0.84	V
R_{D_CC}	Pulldown resistance through each C_CC pin when in a disconnected state and configured as a UFP. VIN powered.	V = 1V, 1.5V	4.59	5.1	5.61	KΩ
$R_{D\_CC\_OPEN}$	Pulldown resistance through each C_CC pin when in a disconnected state and configured as a UFP. VIN powered.	V = 0V to VIN	500	—	—	KΩ
R_{D_DB}	Pulldown resistance through each C_CC pin when in a disconnected state and configured as a UFP. VIN unpowered. (IT8851 only)	V = 1.5V, 2.0V	4.08	5.1	6.12	KΩ
$R_{D\_DB\_OPEN}$	Pulldown resistance through each C_CC pin when in a disconnected state and configured as a UFP. VIN unpowered.	V = 1.5V, 2.0V	500	—	—	KΩ
V_{TH_DB}	Voltage threshold of the pull-down FET in series with RD during dead battery. (IT8851 only)	I_CC = 80 μA	0.5	0.9	1.2	V
R_{FRSWAP}	Fast role swap signal pull down.	—	—	—	5	Ω
V_{TH_FRS}	Fast role swap request detection voltage threshold.	—	490	520	550	mV
VCONN Switch						
R_{ON}	On resistance of the VCONN power FET	—	—	1.2	—	Ω

Parameter		Conditions	Min.	Typ.	Max.	Unit
$V_{(pass)}$	Voltage to pass through VCONN power FET	—	2.7	5	5.5	V
$I_{(VCONN)}$	VCONN current limit	—	—	—	500	mA

Table 11-3. USB PD Signal Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Unit
COMMON						
PD_BITRATE	PD data bit rate	—	270	300	330	Kbps
UI 1	Unit interval (1/PD_BITRATE)	—	3.03	3.33	3.7	µs
CCBLPLUG 2	Capacitance for a cable plug (each plug on a cable may be up to this value)	—	—	—	25	pF
ZCABLE	Cable characteristics impedance	—	32	—	65	Ω
CRECEIVER 3	Receiver capacitance. Capacitance looking into C_CCn pin when in receiver mode.	—	70	—	120	pF
TRANSMITTER						
ZDRIVER	TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750kHz) while the source is driving the C_CCn line.	—	33	—	75	Ω
T_{RISE}	Rise time; 10% to 90% amplitude points; minimum under an unloaded condition; maximum set by TX mask.	—	300	—	—	ns
T_{FALL}	Fall time; 90% to 10% amplitude points; minimum under an unloaded condition; maximum set by TX mask.	—	300	—	—	ns
V_{TX}	Transmit high voltage.	—	1.05	1.125	1.2	V

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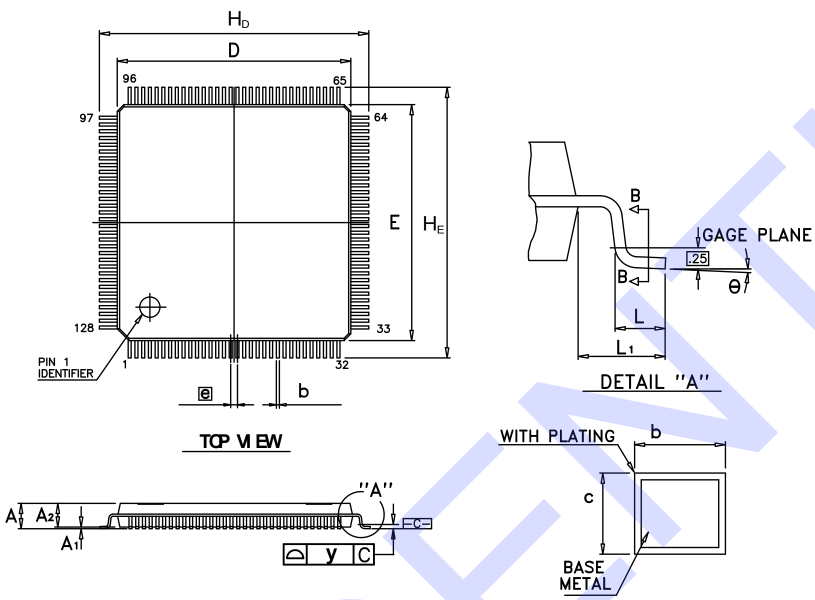
12. Package Information

LQFP 128(14*14) Outline Dimensions

unit: inches/mm



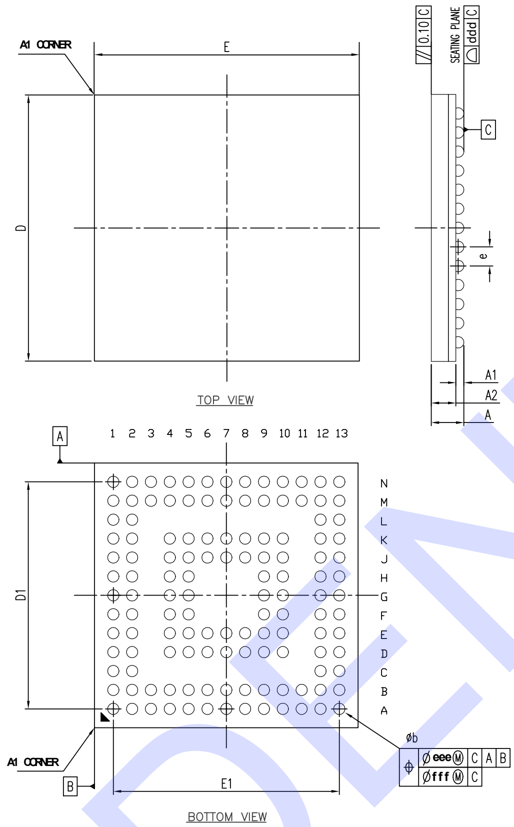
Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A1	0.002	-	-	0.05	-	-
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.007	0.009	0.13	0.18	0.23
c	0.004	-	0.008	0.09	-	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.547	0.551	0.555	13.90	14.00	14.10
e	0.016 BSC			0.40 BSC		
H_D	0.624	0.630	0.636	15.85	16.00	16.15
H_E	0.624	0.630	0.636	15.85	16.00	16.15
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:

1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
   Total in excess of the b dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.
3. Controlling dimensions: Millimeter
4. Reference document: JEDEC MS-026

DI-LQFP128(14*14)v5

VFBGA 128(7*7) Outline Dimensions unit: inches/mm



<table>
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<tr><th>Min.</th><th>Nom.</th><th>Max.</th><th>Min.</th><th>Nom.</th><th>Max.</th></tr>
<tr><td>A</td><td>---</td><td>---</td><td>0.038</td><td>---</td><td>---</td><td>0.97</td></tr>
<tr><td>A1</td><td>0.006</td><td>0.008</td><td>0.010</td><td>0.16</td><td>0.21</td><td>0.26</td></tr>
<tr><td>A2</td><td>0.024</td><td>0.026</td><td>0.028</td><td>0.61</td><td>0.66</td><td>0.71</td></tr>
<tr><td>D / E</td><td>0.272</td><td>0.276</td><td>0.280</td><td>6.90</td><td>7.00</td><td>7.10</td></tr>
<tr><td>D1 / E1</td><td colspan="3">0.236 BSC</td><td colspan="3">6 BSC</td></tr>
<tr><td>e</td><td colspan="3">0.02 BSC</td><td colspan="3">0.5 BSC</td></tr>
<tr><td>b</td><td>0.010</td><td>0.012</td><td>0.014</td><td>0.25</td><td>0.30</td><td>0.35</td></tr>
<tr><td>ddd</td><td colspan="3">0.003</td><td colspan="3">0.08</td></tr>
<tr><td>eee</td><td colspan="3">0.006</td><td colspan="3">0.15</td></tr>
<tr><td>fff</td><td colspan="3">0.003</td><td colspan="3">0.08</td></tr>
<tr><td>MD / ME</td><td colspan="3">13/13</td><td colspan="3">13/13</td></tr>
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Notes:
1. Controlling dimensions: Millimeter
2. Reference document: JEDEC MO-225

DI-VFBGA128(7*7)v4

13. Ordering Information

Part No.	Package	E-Flash Size
IT81202E-000/BX	LQFP 128	N/A
IT81202E-256/BX	LQFP 128	256KB
IT81202E-512/BX	LQFP 128	512KB
IT81202E-1024/BX	LQFP 128	1024KB
IT81202VG-000/BX	VFBGA 128	N/A
IT81202VG-256/BX	VFBGA 128	256KB
IT81202VG-512/BX	VFBGA 128	512KB
IT81202VG-1024/BX	VFBGA 128	1024KB

All green components provided are in compliance with RoHS, and Halogen-Free.

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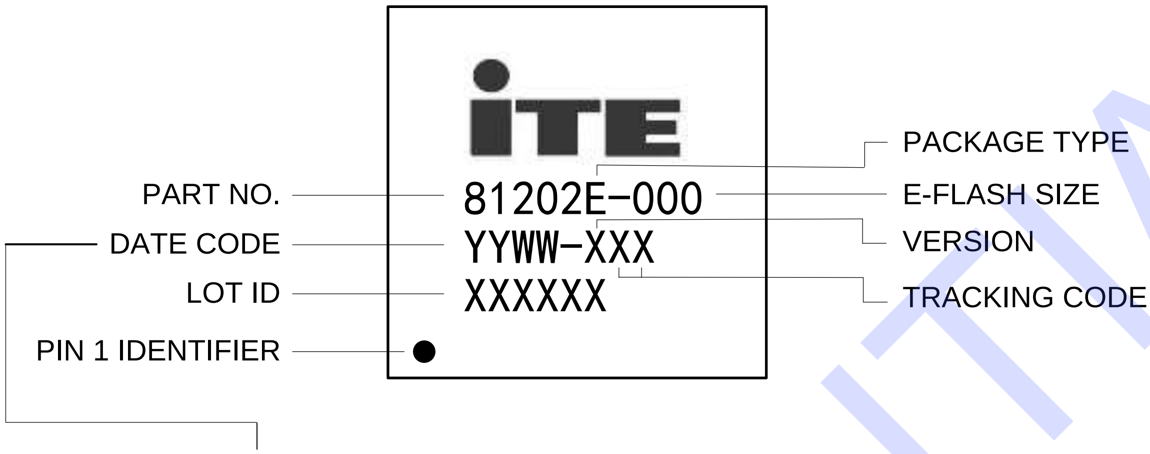
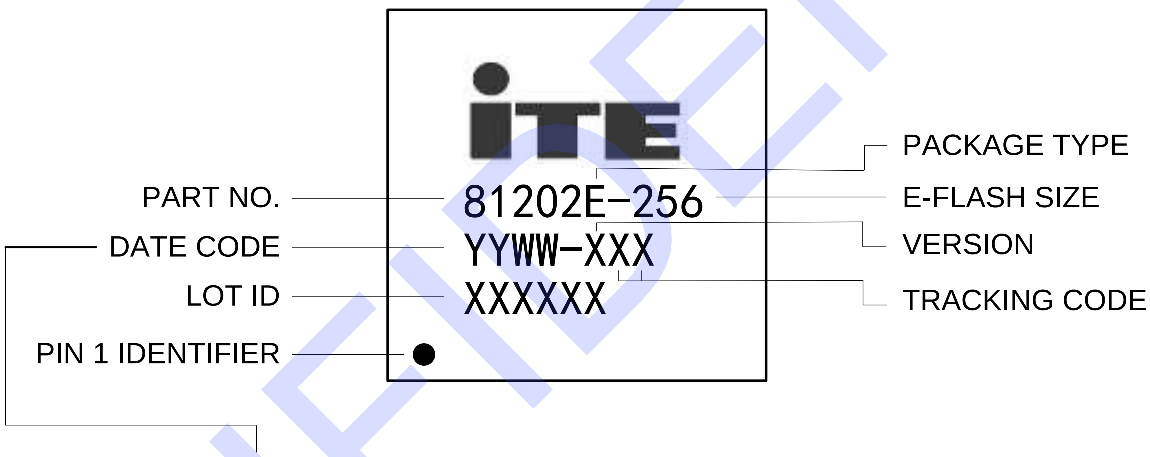
14. Top Marking Information

IT81202E-000



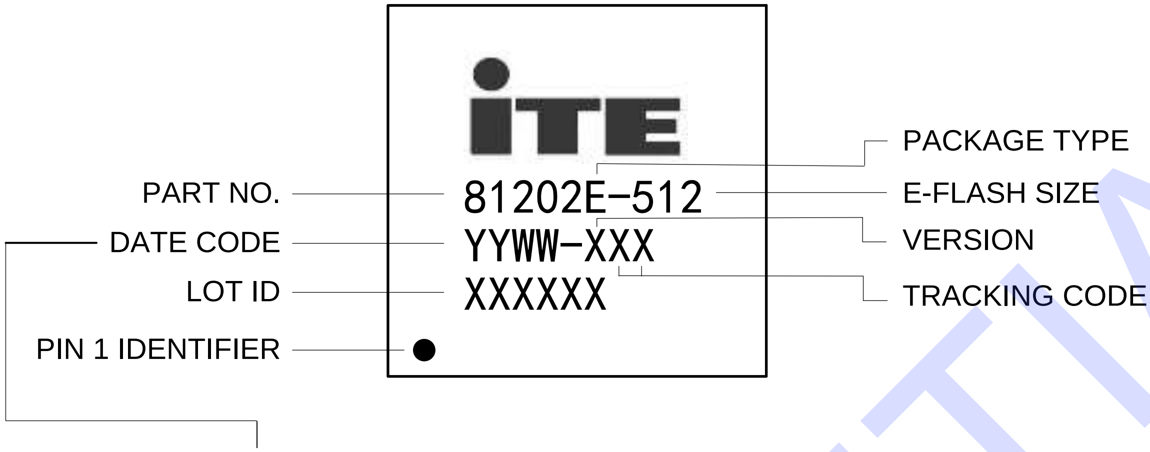
(YY: Year WW: Week)
e.g. YYWW = 2007 → The seventh week of the year 2020

IT81202E-256



(YY: Year WW: Week)
e.g. YYWW = 2007 → The seventh week of the year 2020

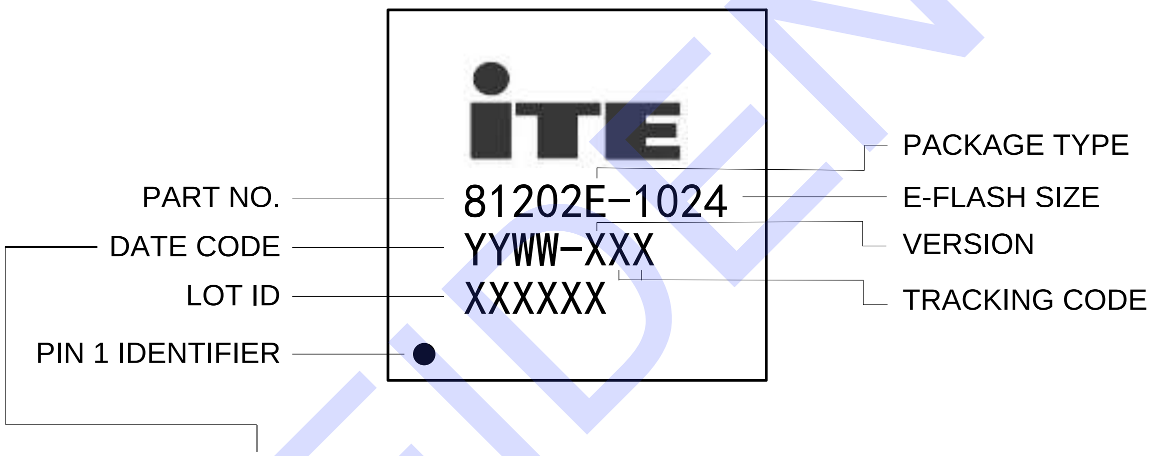
IT81202E-512



(YY: Year WW: Week)

e.g. YYWW = 2007 → The seventh week of the year 2020

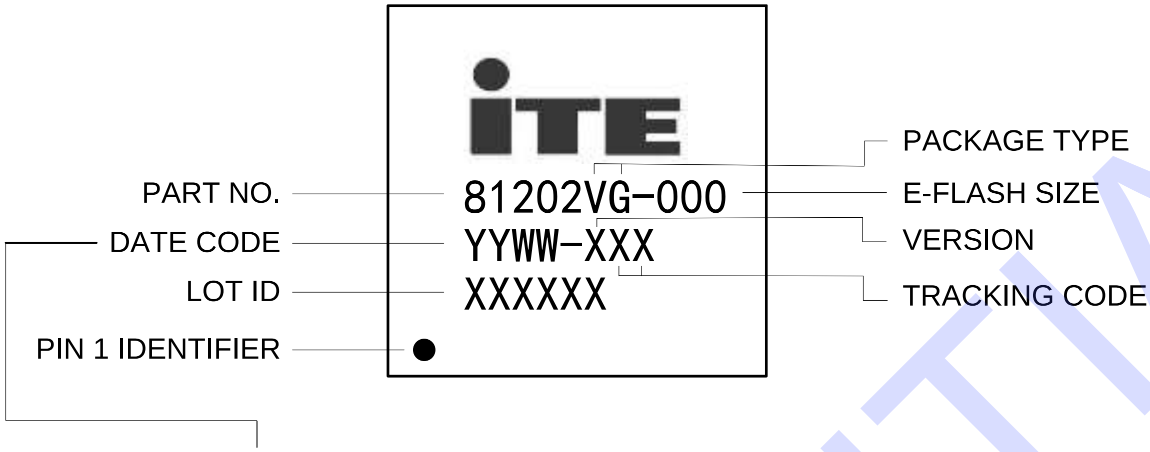
IT81202E-1024



(YY: Year WW: Week)

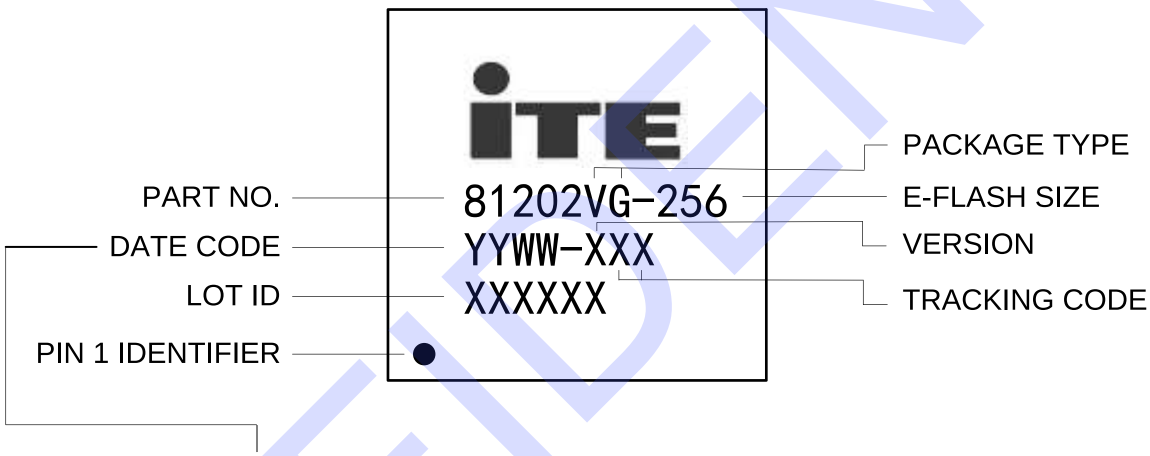
e.g. YYWW = 2007 → The seventh week of the year 2020

IT81202VG-000



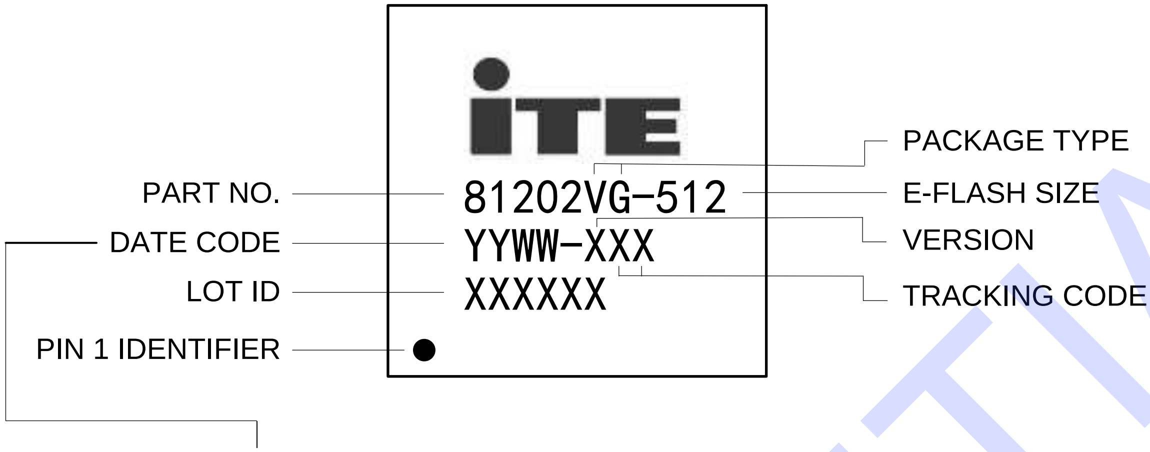
(YY: Year WW: Week)
e.g. YYWW = 2007 → The seventh week of the year 2020

IT81202VG-256



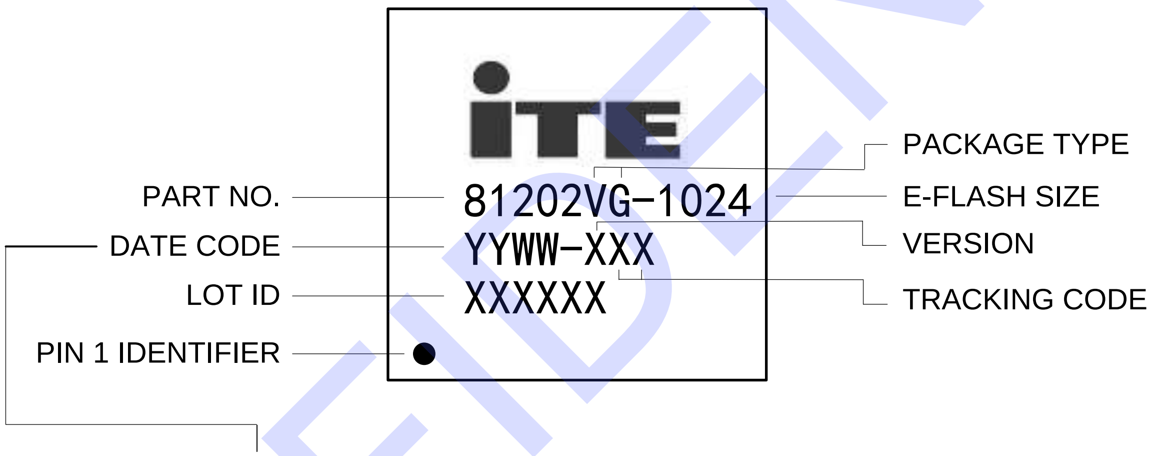
(YY: Year WW: Week)
e.g. YYWW = 2007 → The seventh week of the year 2020

IT81202VG-512



(YY: Year WW: Week)
e.g. YYWW = 2007 → The seventh week of the year 2020

IT81202VG-1024



(YY: Year WW: Week)
e.g. YYWW = 2007 → The seventh week of the year 2020

ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2013)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc.

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Otherwise specified in the order agreed by Seller, delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and by its conditions Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.